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Balance Winding Scheme to Reduce Common-Mode Noise in Flyback Transformers

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Abstract

The flyback topology is being widely used in power adapters. The coupling capacitance between primary and secondary windings of a flyback transformer is the main path for common-mode (CM) noise conduction. A Y-cap is usually used to effectively suppress EMI noise. However, this results in problems in space, cost, and the danger of safety leakage current. In this paper, the CM noise behaviors due to the electric field coupling of the transformer windings in a flyback adapter with synchronous rectification are analyzed. Then a scheme with balance winding is proposed to reduce the CM noise with a transformer winding design that eliminates the Y-cap. The planar transformer has advantages in terms of its low profile, good heat dissipation and good stray parameter consistency. Based on the proposed scheme, with the help of a full-wave simulation tool, the key parameter influences of the transformer PCB winding design on CM noise are further analyzed. Finally, a PCB transformer for an 18W adapter is designed and tested to verify the effectiveness of the balance winding scheme.

Key words: Balance winding, common-mode (CM) noise, EMI, Flyback, PCB transformer

I. INTRODUCTION

In switched-mode power supplies (SMPS), the electromagnetic interference (EMI) problem is a challenge, especially when it comes to CM noise. The methods for reducing CM noise can be categorized into three main types. The first type uses EMI filters [1]-[4], which results in large size and cost. Adding a Y-cap across the transformer static points of primary and secondary windings is very effective to reduce the CM noise through the transformer. However, due to safety leakage current regulations, the capacitance of a Y-cap is limited, and in some applications, the use of a Y-cap is not allowed. In addition, the inductors in EMI filters are easily influenced by electric and magnetic near-field coupling due to their compact space [5], which may degrade the filtering effect. The second type involves electrical considerations, such as frequency jitter [6], capacitors paralleled in switches, RCD or RC snubbers, spike killers, PCB layout design, etc. The third type reduces the CM noise flowing through the transformer path by partial shielding, noise cancelation [7]-[20] or by compensation techniques through transformer winding design. They consider the electric field behaviors in the transformer winding window, which means considering the transformer as a CM EMI filter. In addition, they also have functions in voltage transform and insulation. In other words, to integrate the voltage transform function (more related to magnetic fields) and the CM EMI filter function (more related to electric fields) in the transformer. The transformer in a flyback adapter is critical due to its efficiency and power density. It is also very important in terms of EMI noise, especially CM noise. Voltage pulsations due to switch or diode operations act on the primary and secondary windings of the transformer. This builds the voltage potential distribution along each turn of the windings and makes the displacement currents or electric charges flow through the transformer to form CM noise. The CM noise flows to the LISN through the parasitic capacitance between the secondary and the ground for the two-wire (L and N lines) type or through the grounding line directly for the three-wire (L, N and GND lines) type. By connecting the heatsinks of switches and shielding the transformer core to the primary DC bus point or the static point, the CM noises by the heatsink and core can largely avoid flowing to the LISN. As a result, the transformer becomes the main path of CM noise, which is very important for total conductive EMI

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noise. This attracts the attention of many scholars looking to reduce CM noise in view of the transformer.

A lot of scholars are focused on methods to reduce CM noise by transformer winding design [7]-[15]. For planar transformers, the concept of paired layers was proposed and applied in a flyback planar transformer with an interleaved structure, which means the adjacent primary and secondary winding layers have the same turns and the same dv/dt between the adjacent primary and secondary sides, so that their overlapping does not generate CM noise [7]. Because the turn numbers of the primary winding are always larger than those of the secondary winding, the remaining primary windings are placed between the layers of the primary side in order to hide them behind the secondary winding. However, this method can also increase the number of PCB layers and the flexible layout of the PCB winding may also be limited. This greatly increases the cost of the PCB board, which may be impractical in PCB transformers. The shielding technique is usually used to suppress CM noise by inserting copper foil between the primary and the secondary winding layers. In [13], two layers of identical single-turn copper are inserted in between the primary and secondary winding layers as shielding. The shielding layer adjacent to the primary winding layer is connected to the primary ground and the other shielding layer is connected to the secondary ground. There is no CM noise between the two shielding layers since they have the same voltage potential distributions. However, this method is not suitable in transformers with an interleaved winding structure due to problems of the core windows area and cost. Some research found that shielding with only a portion of the area between the primary and secondary windings, called partial shielding, is better than the full shielding to cancel CM noise. The size of the shielding copper in terms of the length and width of the partial shielding layer and the distance between the shielding and winding were analyzed in detail for suppressing CM noise [11]. Furthermore, Ansys Maxwell is adopted to determine the shielding foil structure size. For traditional wiring transformers, it is difficult to build a 3D model to simulate the influences of these factors, since the key structure data (such as the distance between primary and secondary windings) cannot be precisely obtained. In addition, there have been some studies suggesting that coaxial cable can be used as secondary windings [14]. It can also eliminate the displacement current between the center conductor and the outer layer grounding conductor for the same voltage distribution or the same turn numbers of the center conductor and the outer layer grounding conductor. However, this approach can also bring some challenges in terms of occupying more window height and increasing the leakage inductance when compared with enameled wire. The authors of [12] proposed a method to divide the primary windings into two portions. In addition, the primary switch is moved to the middle so that both the positive and negative voltages can be built in the primary winding to have a noise cancelation mechanics. However, difficulty is introduced to the gate driving of the primary switch.

In this paper, a noise balance winding scheme is proposed, together with its analysis and design with the help of Ansys HFSS full-wave simulation. The balance winding is inserted between the adjacent primary and secondary winding layers, and the suitable turns of the balance winding can be determined easily to reduce CM noise.

This paper is organized as follows. In Section II, the conduction paths of CM noise with traditional diode rectification and synchronous rectification are presented and compared. In section III, the origin of the CM noise flowing through the transformer is revealed to be the resultant electric charges induced in the secondary winding conductors. To cancel the CM noise flowing through the transformer path, the concept of balanced winding with anti-phase voltage potential and its basic design principle are proposed. The basic design principle simply follows that the average of the voltage potential in the balance winding is equal to that in the adjacent secondary winding. For detail consideration, some vital factors such as the gap between the PCB traces in a layer and the distance between the PCB layers are accurately analyzed with simulations. In Section IV, the traditional measurement of CM capacitance and the proposed method are introduced and compared. In Section V, an 18W PCB planar flyback converter is designed and the tested CM noise spectrums can verify the effectiveness of the noise balance winding scheme. Finally, Section VI concludes this paper.

II. CM Noise Conduction Paths and Noise Cancelation Mechanics

A. CM Current Through a Transformer with Traditional Diode Rectification

In a traditional flyback converter with a diode in the secondary, CM current is generated by voltage pulsations in both the primary MOSFET and the secondary diode. As shown in Fig. 1, the primary MOSFET generates CM current i_{ps} conducted to the secondary side through the equivalent coupling capacitance C_{ps} to the LISN, and the secondary diode generates CM current i_{sp} conducted to the primary side through the equivalent coupling capacitance C_{sp} to the LISN, where i_{ps} is determined by $V_p \cdot C_{ps}$, and i_{sp} is determined by $V_s \cdot C_{sp}$. Although the phases of CM current i_{ps} and i_{sp} are opposite, they generally cannot be fully canceled if a careful winding design is not considered. In addition, C_{ps} and C_{sp} are equivalent CM coupling capacitances produced by the primary and secondary voltage potential distributions, not just the structure capacitance between the primary and secondary windings such as the electrodes of the two capacitors. The equivalent CM coupling capacitance is also called dynamic

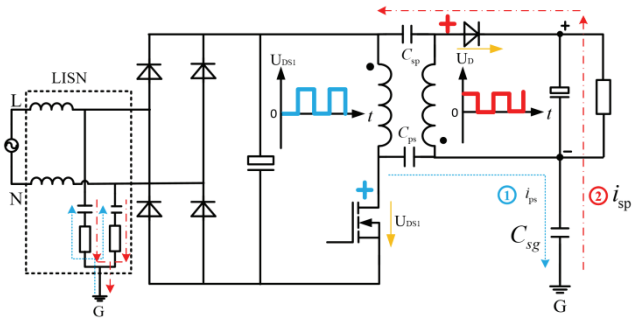


Fig. 1. CM noise conduction path of a flyback converter with diode rectification.

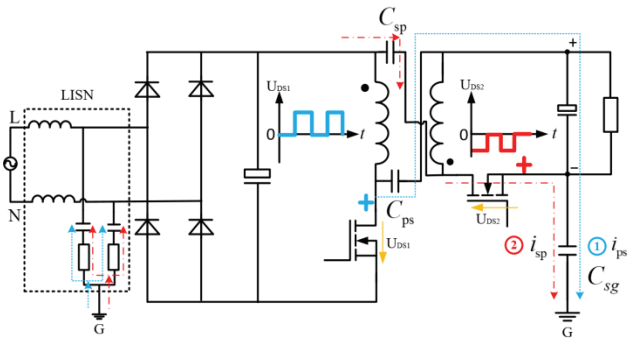


Fig. 2. CM noise conduction path of a flyback converter with synchronous rectification.

CM capacitance and the structure capacitance is just static capacitance. The detailed differences between these two kinds of capacitance will be introduced in section IV. In order to totally cancel the two CM currents, the transformer winding layout should be carefully designed and adjusted to change the winding voltage potential distributions and the values of C_{ps} and C_{sp}, so that the condition $V_P \cdot C_{ps}=V_S \cdot C_{sp}$ is satisfied to achieve zero CM noise. In this respect, the flyback transformer also acts as a CM noise filter.

B. CM Current Through a Transformer with Synchronous MOSFET Rectification

For reducing the switching loss caused by the secondary diode, the technology of synchronous rectification is applied in flyback converters. As shown in Fig. 2, a synchronous MOSFET is used in the secondary. Usually, the location is changed from the positive side to the negative (ground) for easy gate driving. However, the location change of a synchronous rectification device causes a phase inversion of the secondary CM noise source V_s, which results in the same phases of the CM current i_{sp} and i_{ps} and then their cancellation mechanics disappears. Therefore, the techniques proposed in [7] and [11] can no longer be used since they cannot generate the anti-phase CM current to cancel i_{ps} and i_{sp}. Therefore, the total CM current $i_{CM}=i_{ps}+i_{sp}$ increases. In order to build cancelation mechanics, additional winding with anti-phase potential is needed to generate the anti-phase CM noise to cancel i_{ps} and i_{sp}. The details will be described below.

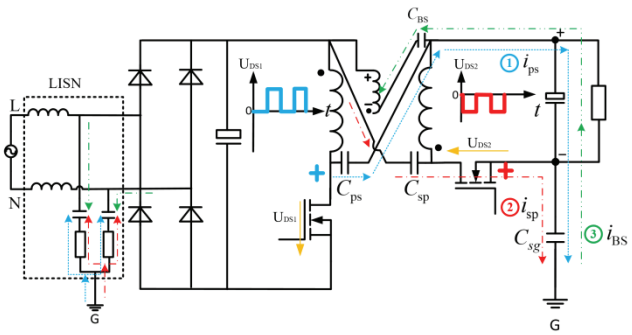


Fig. 3. CM noise conduction path of a flyback converter with dummy winding.

C. CM Current Through a Transformer with Dummy Winding

In order to achieve CM noise attenuation, an additional winding is introduced and shown in Fig. 3. One terminal of the additional winding is connected to the primary voltage static point and the other is open. In addition, the wiring direction of the additional winding should be the same as that of the secondary winding. This additional winding is also called dummy winding since it is only used to build electric fields and there is no power current flowing through it. This dummy winding introduces an equivalent coupling capacitance C_{BS} between the secondary winding and the dummy winding. Adjusting the turns of the dummy winding can change the CM current i_{BS} flowing through C_{BS}. Anti-phase CM current i_{BS} can be generated to cancel i_{ps} and i_{sp}. With proper turns of the dummy winding, the CM noise cancellation can be achieved. In addition, the displacement current between the dummy winding and the primary winding circulates internally between the dummy winding and the primary winding due to one terminal of the dummy winding being connected to the primary static point.

III. CM Current Through a Flyback Transformer

A. Origin of CM Noise

The PCB winding structure of a flyback transformer is shown in Fig. 4. It can be seen that the primary and secondary windings have a sandwich structure to reduce the winding losses and leakage inductance. The layers P1-P4 are the primary windings and layers S1-S3 are secondary windings. The point A1 is connected to primary MOSFET and a1 to secondary diode or MOSFET. They are considered to be voltage hot points. The point A5 is connected to the primary ground, and a4 is connected to the secondary ground. Thus, they are both voltage static points. Only the displacement current flowing through the LISN is detected by EMI receiver as CM noise. Therefore, displacement current flowing internally in the primary winding layers does not cause CM noise. In addition, by connecting the magnetic core to the

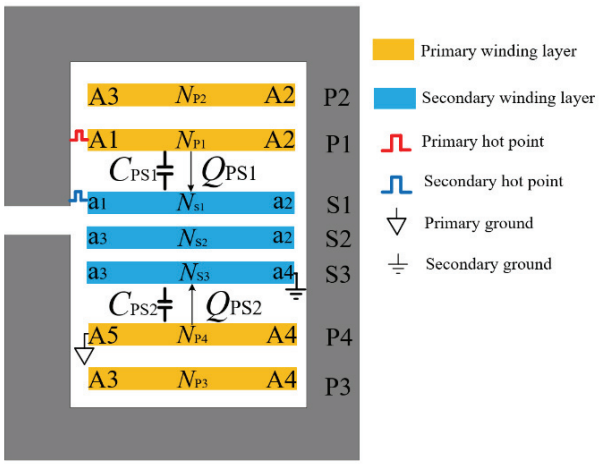


Fig. 4. Winding structure of a flyback transformer.

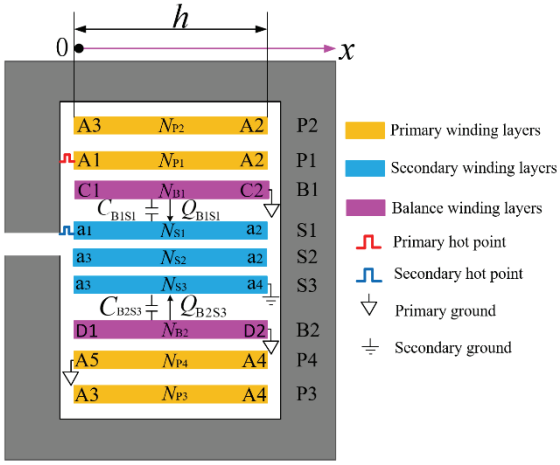


Fig. 5. Winding structure of a flyback transformer with the balance winding.

primary ground, the displacement current between the core and the primary winding does not flow to the LISN. Only the displacement current flowing through the equivalent coupling capacitances C_{PS1} and C_{PS2} in the interface of the adjacent primary and secondary winding layers, by the existence of the voltage potential distributions in each turn of the transformer winding layer, flows through the LISN via the capacitance of secondary side to the ground (for two-wires) or directly to the ground (for three-wires).

For the PCB layout, as shown in Fig. 4, there are voltage potential distributions in the layers P1 and S1, which generate the electric charges Q_{PS1} in the layer S1 and is defined as equivalent capacitance C_{PS1}. Similarly, there is a voltage potential distribution in the layers P4 and S3, and C_{PS2} is defined. Due to the existence of C_{PS1} and C_{PS2}, the primary winding layers P1 and P4 induce electric charges in the secondary layers S1 and S3, respectively.

The CM current i_{CM} flowing through the transformer can be expressed as:

$$i_{CM} = \frac{dQ_{CM}}{dt} \tag{1}$$

where Q_{CM} is the resultant electric charges in the secondary winding induced by the voltage potential distributions on each turn of windings. Therefore, for a clearer understanding, the origin of CM noise can be regarded as the resultant electric charges in all of the secondary winding layers.

B. CM Currents Through a Transformer with Balance Winding Layers

In order to reduce the resultant electric charges in the secondary winding layers to almost zero, this paper proposes a CM noise balance winding scheme in which a balance winding is inserted between adjacent primary and secondary winding layers. The transformer structure of this scheme is shown in Fig. 5. The primary winding layers are P1-P4 and the secondary winding layers are S1-S3. The balance winding B1 is inserted between the layers P1 and S1, and the balance winding B2 is inserted between the layers P4 and S3. One terminal of the balance winding B1 is connected to the primary ground and the other is open. The wiring direction is the same as that of the S1. Similarly, the B2 connection is the same as the B1 connection and the wiring direction is the same as S3. Thus, the balance windings B1 and B2 induce the electric charges Q_{B1S1} and Q_{B2S3} in the secondary layers S1 and S3, respectively. In addition, the primary winding layers P1, P2, P3 and P4 are hidden behind the balance winding, and these primary winding layers can induce small CM noise charges in the secondary winding layers. Therefore, the CM currents i_{ps} and i_{sp} shown in Fig.3 are not considered in this section tentatively.

The wires in traditional enameled winding, are always densely wound and have higher turn numbers in a layer when compared with PCB winding which has a larger trace width and fewer turn numbers in a layer. Therefore, for enameled winding, the step of the voltage potential distribution in each wire of the layer is very small and it is more reasonable to regard it as a linear distribution in theoretical calculations. Unlike traditional enameled winding transformers, PCB winding turns have a larger trace width. Therefore, the voltage potential distribution in a layer is distributed step by step. For the convenience of the theoretical calculation, it is reasonable to consider it as continuous linear distribution proximately to get the following expressions of $V_{B1}(x)$, $V_{B2}(x)$, $V_{S1}(x)$ and $V_{S3}(x)$.

$$V_{B1}(x) = \frac{V_P}{N_P} N_{B1}\left(\frac{x}{h} - 1\right) \tag{2}$$

$$V_{S1}(x) = \frac{V_P}{N_P}\left(N_{S1}\frac{x}{h} - N_S\right) \tag{3}$$

$$V_{B2}(x) = \frac{V_P}{N_P} N_{B2}\left(\frac{x}{h} - 1\right) \tag{4}$$

$$V_{S3}(x) = \frac{V_P}{N_P} N_{S3}\left(\frac{x}{h} - 1\right) \tag{5}$$

where V_P is the AC voltage across the primary MOSFET or the primary winding, and V_S is the AC voltage across the secondary MOSFET or the secondary winding. In addition, h is the width of the magnetic core window, N_{B1} is the turn numbers of the layer B1. Similarly, N_{S1}, N_{B2} and N_{S3} are the turn numbers of the layers S1, B2 and S3, respectively. Furthermore, the voltage difference between the primary ground and the secondary ground is omitted. This is due to the fact that for a flyback converter with three-wires (L, N and GND lines), the voltage difference between the primary and secondary grounds is only the voltage drop of the LISN by common-mode noise if the voltage of the rectifier bridge is ignored. Therefore, the voltage drop of the LISN is usually very small and can be omitted. For a flyback adapter with two-wires (L and N wires), the secondary ground is floating. Thus, the voltage drop between the primary ground and the secondary ground is determined by both the value of the CM current i_{CM} and the stray capacitance C_{sg} between the secondary ground and GND. This paper aims to achieve a zero CM current with proper transformer winding design. This means the transformer is designed in terms of zero CM current. Based on this assumption, the voltage difference between the primary ground and the secondary ground should be zero.

Fig. 6 and Fig. 7 show the voltage potential distribution of the layers B1, S1, B2 and S3.

From Fig. 6, the charges of Q_{B1S1} inducted in the secondary layer S1 by the balance winding B1 can be calculated as (6).

$$\begin{aligned} Q_{B1S1} &= \int_0^h \frac{C_{01}}{h}\left[V_{B1}(x) - V_{S1}(x)\right]dx \\ &= \frac{C_{01}V_P}{2N_P}\left(N_{B1} + N_{S1} - 2N_S\right) \end{aligned} \tag{6}$$

where C_{01} is the structure capacitance between the layer B1 and S1.

From (6), the charges of Q_{B1S1} are equal to zero, if (7) is satisfied.

$$N_{B1} = 2N_S - N_{S1} \tag{7}$$

In a similar way, the CM charges of Q_{B2S3} induced in the secondary winding layer S3 are calculated as (8).

$$\begin{aligned} Q_{B2S3} &= \int_0^h \frac{C_{02}}{h}\left[V_{B2}(x) - V_{S3}(x)\right]dx \\ &= \frac{C_{02}V_P}{2N_P}\left(N_{B2} - N_{S3}\right) \end{aligned} \tag{8}$$

where C_{02} is the structure capacitance between the layer B2 and S3. From (8), the charges of Q_{B2S3} are equal to zero, if (9) is satisfied.

$$N_{B2} = N_{S3} \tag{9}$$

From (7) and (9), the principle to make the resultant electric charges be zero is that the average of the voltage potential in the balance winding layer is equal to that in the adjacent secondary winding layer. In addition, if the resultant electric charges are zero, the equivalent CM noise capacitances C_{B1S1} and C_{B2S2} are also equal to zero. They are not traditional physical capacitors and they are generated by the voltage difference between the balance winding and the adjacent secondary winding. If the proper turns of N_{B1} and N_{B2} can make the resultant electric charges in all of the secondary winding layers (Q_{B1S1}+Q_{B2S3}) equal to zero, the conditions in expressions (7) and (9) are not the only solution.

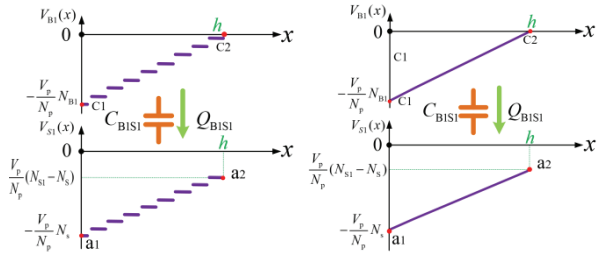


Fig. 6. Voltage potential distribution of the layers B1 and S1: (a) Step voltage potential distribution; (b) Linear voltage potential distribution.

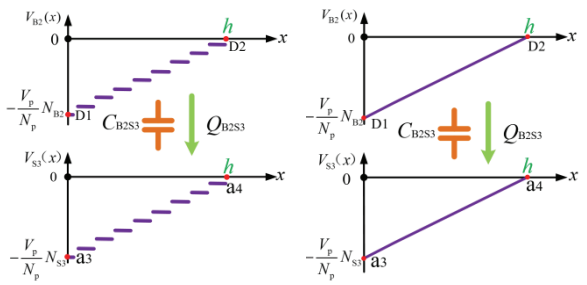


Fig. 7. Voltage potential distribution of layers B2 and S3: (a) Step voltage potential distribution; (b) Linear voltage potential distribution.

The connection scheme of the balance winding is the same as that of the convention shielding scheme. However, the principles for reducing CM noise by the proposed method and the shielding method are completely different. For the proposed balance winding method, the turn number and size of the balance winding are designed and used to adjust the electric charges to make the resultant charges in the secondary winding balanced or canceled to zero.

IV. Considering the Influence of the Gap Between PCB Winding Traces

In section III B, the calculation formulas of the balance winding turns ignore the inductive CM charges caused by the primary winding layers. In the PCB winding, there is always a minimum gap between the traces due to manufacturing limitations. Because of these gaps, the secondary winding layers induce CM charges Q_{PS} across the gaps by the primary

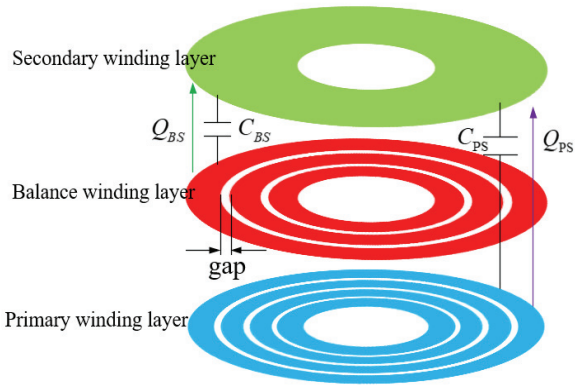


Fig. 8. Influence of the gaps between the balance winding traces.

winding layers. When the turns of the balance winding are large, the gaps occupy a larger portion area in a layer.

In order to achieve zero resultant charges in the secondary winding layers, it is necessary to consider the influence of gaps. Generally, the gap between PCB traces is 0.1-0.2mm. The high-frequency magnetic fields and electric fields exist and are coupled in the transformer. Ansys HFSS high-frequency full-wave electromagnetic field simulation software is very suitable for S parameter analysis. As mentioned above, the transformer can be regarded as a CM noise EMI filter. Therefore, the reflection parameter S_{21} or insertion loss should be extracted to evaluate the characteristics of suppressing CM noise. It should be noted that the voltage phases in the simulation excitation assignment must conform with the transformer winding terminal connections in the circuit. The lower the value of S_{21}, the lower the resultant charges in the secondary windings or CM noise current.

V. Transformer Evaluation

A. Traditional Evaluation Method

The structure capacitance in the transformer is examined in the following section. Fig. 9 shows the traditional transformer EMI characteristic evaluation method. The two terminals of the primary and secondary winding are also connected. The two ports of the LCR meter or the impedance analyzer are connected to the terminals a and b. However, this method cannot take the electrical potential distribution along the winding turns in the transformer into consideration. In this way, the voltage potential in the primary and secondary winding is a constant. Therefore, the capacitance CS measured by this method is the static physical structure capacitance, not the dynamic CM noise capacitance. The structure capacitance is referred to the static capacitance, since this capacitance is only determined by physical structure parameters such as the area, the distance and the permittivity in the space between the primary and the secondary winding layers, which have nothing to do with the transformer behaviors in real operating conditions. The dynamic capacitance, which is determined by

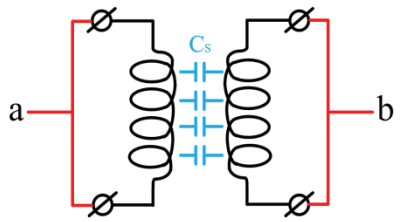


Fig. 9. Traditional transformer evaluation method by an LCR meter or impedance analyzer.

the structure parameters and the voltage potential distribution, can reflect transformer behaviors in real operating conditions.

B. C_Q Evaluation Method

Based on the concept of regarding the transformer as a CM EMI filter, the S_{21} parameters can be measured by a Network Analyzer to calculate the lumped CM noise capacitance C_Q. This method can take the influence of the transformer winding structure into consideration and synthesize the influences of C_{PS}, and C_{BS}. As analyzed in Section III A, the origin of CM current is the resultant electric charges in the secondary winding layers. The total CM noise charges contain the charges induced by the balance winding and the primary winding. Then the total resultant CM noise charges in the secondary winding layers can be defined as:

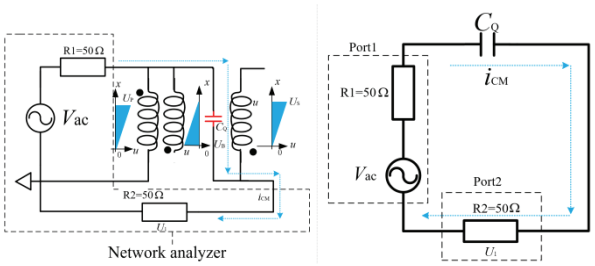
$$Q_{CM}=V_P \cdot C_Q \tag{10}$$

where Q_{CM} is determined by V_P and C_Q. V_P is the primary winding voltage that is a constant, and C_Q is the equivalent CM noise capacitance that can be determined by the winding structure. Thus, the smaller the value of C_Q, the fewer resultant CM noise charges Q_{CM}.

As shown in Fig. 10 (a), Port 1 of the network analyzer is connected to the primary winding voltage hot point with grounding to the primary winding static point. In addition, the static point of the secondary winding is connected to Port 2 with only the hot point of the secondary winding open. Port 1 outputs excitation, which builds voltage potential distributions in the primary, balance and secondary windings. The resultant charges induced in the secondary winding layers form CM current. Fig. 10(b) is the test equivalent circuit. The CM current flows through the transformer by the total equivalent CM noise capacitance C_Q and produces a voltage drop U_1 in the resistance R2. When C_Q is shorted, the voltage drop in R2 is U_2. According to the definition of S_{21}, it can be deduced as in (11).

$$S_{21}(\text{dB})=20\lg\left|\frac{U_1}{U_2}\right| \tag{11}$$

where U_1 refers to the voltage drop of the resistance R2 with the transformer as a CM filter, and U_2 refers to the voltage drop of the resistance R2 without a transformer or shorting C_Q. Then (11) can be further deduced by (12) and (13) to (14).



(a) (b)

Fig. 10. Evaluation method and equivalent circuit: (a) Proposed evaluation method; (b) Equivalent circuit.

$$U_1=\frac{50}{100+\frac{1}{j\omega C_Q}}V_{ac} \tag{12}$$

$$U_2=\frac{50}{100}V_{ac} \tag{13}$$

$$S_{21}(\text{dB})=20\lg\left|\frac{100}{100+\frac{1}{j\cdot 2\pi f\cdot C_Q}}\right| \tag{14}$$

In practice, the value of $1/2\pi fC_Q$ is far larger than 100 since the capacitance of C_Q is usually less than hundreds of pF and the frequency f is from 150kHz to 30MHz. Therefore, when f increases 10 times S_{21} (dB) increases 20dB. This means its curve slope is 20dB/Dec with the frequency axis in logarithmic. Based on (14), the expression of C_Q can be given as (15).

$$C_Q=\frac{1}{2\pi f\sqrt{10^{\frac{40-S_{21}(\text{dB})}{10}}-10^4}} \tag{15}$$

S_{21} in dB versus the frequency f can be obtained by simulation. Then the C_Q by (15) can evaluate the transformer behaviors for suppressing CM noise. Obviously, the smaller the value of C_Q, the fewer CM charges Q_{CM} according (10).

VI. Experimental Results

With the proposed balance winding scheme, the CM noise through the transformer can be greatly reduced and even to zero. As a result, the Y-cap can be removed. In order to verify this, a flyback converter with a PCB planar transformer is built and the winding structure is shown in Fig. 5. The detailed specifications are shown in Table I. The turn numbers of the two balance windings are calculated as (16) and (17) according to (7) and (9).

$$N_{B1}=2N_S-N_{S1}=5 \tag{16}$$

$$N_{B2}=N_{S3}=1 \tag{17}$$

The gap between the PCB traces in a layer is set to 0.2mm (determined by the PCB manufacturer). In addition, some other factors, such as the magnetic core, winding edge effects, etc. were also considered in the simulation.

TABLE I
Prototype Specification

Parameter		Value
Input		90-230V
Output		9V/2A
Switching Frequency		85kHz
Transformer	Core	EID22.5/12.3, PC95
	Winding Arrangement	PSP
	N_P=24, N_S=3, N_{P1}=N_{P2}=N_{P3}=N_{P4}=6, N_{S1}= N_{S2}= N_{S3}=1	

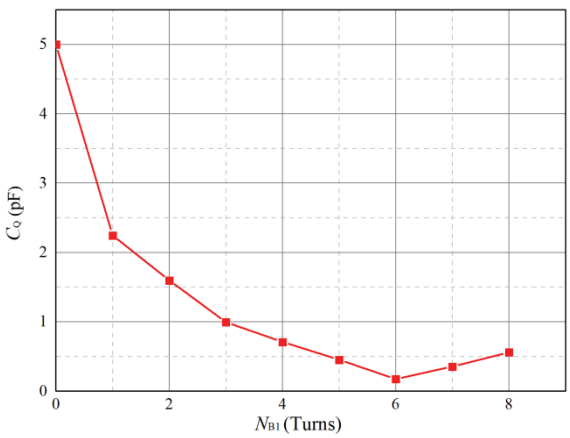


Fig. 11. Simulation result.

Several PCB windings with different turns of the balance winding layer B1 were built in the simulation to get the S_{21} parameter. Then C_Q can be calculated by (15), as shown in Fig. 11. It is clearly found that with different turns of the balance winding B1, there exists a lowest C_Q or the lowest CM noise when N_{B1} is 6 instead of 5 as calculated in (16). In addition, the influence of gaps may not be ignored in some cases.

A. Simulation Verification

To verify the validity of the proposed simulation method, Fig. 12 shows comparisons of S_{21} versus frequency with the results from the simulation, the test, and the ideal C_Q model.

For the ideal C_Q model, the transformer is regarded as an equivalent ideal capacitance to conduct CM noise and the trace of S_{21} can be calculated by (14) with a slope of 20dB/Dec when the frequency axis is logarithmic.

The S_{21} results by the simulation and test with 6 turns of the balance winding layer B1 are also shown in Fig. 12. They conform well below 2MHz. However, they do not conform well from 2MHz to 30MHz. There are many factors for this discrepancy. However, the most important reason is that the permeability of the magnetic core varies with the frequency during high frequency ranges, resulting in variations of the magnetizing inductance and leakage inductance. However,

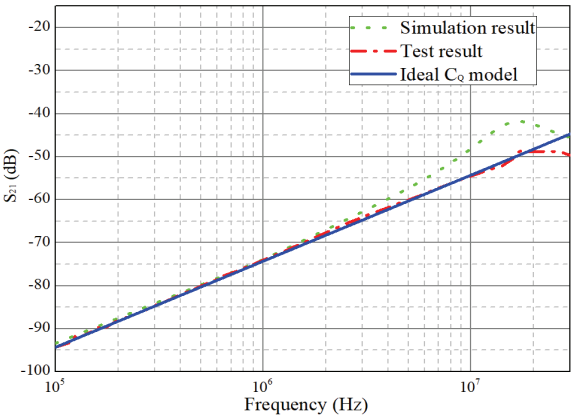


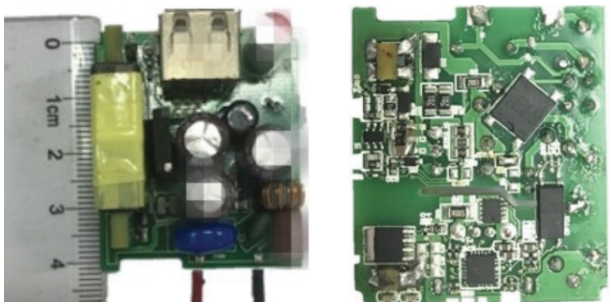
Fig. 12. Comparison result from the simulation, the test and the ideal C_Q.

the permeability of the core in the datasheet is usually given below several MHz. For the core material, PC95 is used. Only the permeability below 2MHz is given in the datasheet. Therefore, it is difficult to make the simulation and test results conform well in high-frequency ranges. In addition, the reason for the differences in high-frequencies is due to the effects of the transformer leakage inductance. Therefore, the transformer cannot be merely regarded as a capacitance in all of the frequency ranges. It is also found, by a Network Analyzer, that the phases of S_{21} are 90 deg in the lower frequencies ranges and that the phases may vary from 90 deg with increasing frequencies. That is to say, the transformer can be regarded as a capacitance below 2MHz in the designed planar transformer, and C_Q is effectively used to evaluate the CM noise behaviors of a transformer.

B. CM Noise Test

The CM noise spectrum of the designed flyback converter is measured in the electromagnetic shielding chamber. The EMI receiver is R&S ESCI, the LISN is R&S ESH2-Z5 and the RF current probe is R&S EZ-17. The directions of the CM currents flowing through the L and N lines are the same. Then CM current can be measured by an RF current probe. The adapter pictures with designed PCB planar transformer is shown in Fig. 13.

The measured CM noise spectrums of the flyback converter in three different situations are illustrated in Fig. 14. The first is the measured CM noise spectrum with 5 turns of the balance winding B1 in the designed PCB transformer shown in the blue line. The second is the measured CM noise spectrum with 6 turns of the balance winding B1 shown in the red line. Comparing these two situations, it can be seen that the measured CM noise spectrum can be reduced by 5dB. This means that the PCB transformer with 6 turns of balance winding is better than that with 5 turns of balance winding in suppressing CM noise. The third is the measured CM noise spectrum by shorting the static points of the primary and secondary windings and the transformer is that with 6 turns of



(a) (b)

Fig. 13. Flyback adapter with the proposed balance winding: (a) Top view of the prototype; (b) Bottom view of the prototype.

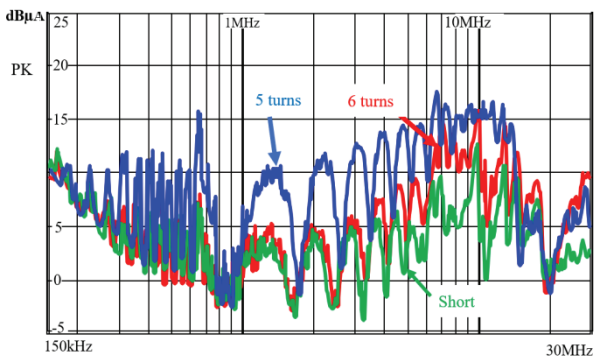


Fig. 14. Test results.

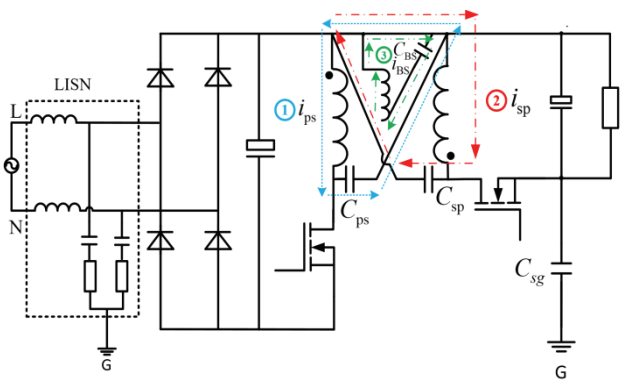


Fig. 15. Shorting the static points of the primary and secondary windings.

the balance winding B1. The third situation is only used for verifying whether the CM noise flowing transformer path has been eliminated. As a result, this action can make the CM current circulate internally in the transformer instead of being detected by the LISN as shown in Fig. 15. When compared with the second and third situations, it can be seen that the CM noise spectrums are the same below 4 MHz. This can reasonably prove that the CM current in the transformer path has been completely attenuated. It also verifies the effectiveness of the proposed simulation method. However, there are some problems in the high-frequency ranges when the CM spectrum have behaviors that are not as good as those in lower frequencies ranges.

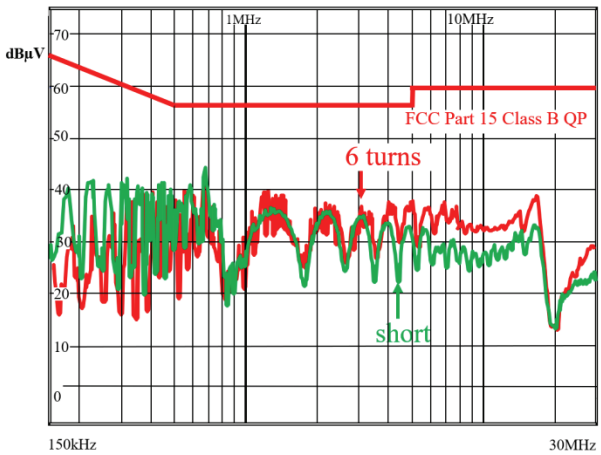
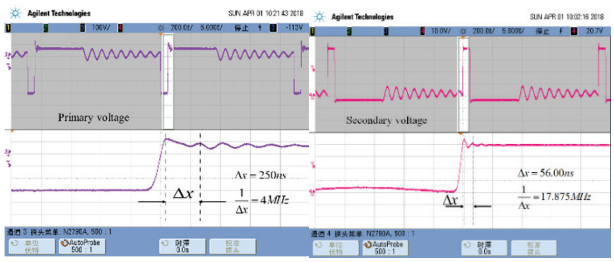


Fig. 16. Test EMI noise spectrums.



(a) (b)

Fig. 17. Voltage waveforms: (a) Primary voltage waveform; (b) Secondary voltage waveform.

Fig. 16 shows test EMI noise spectrums and the EMI test standard is the FCC (Federal Communications Commission) Part 15 class B. It can be seen that the test EMI noise spectrum with 6 turns of the balance winding B1 can have good EMI performance and that it is much lower than the EMI test standard limit line (above the 10 dB margin). In addition, the EMI noise spectrum with balance winding can have almost the same EMI noise attenuation effect when compared with that with shorting the static points of the primary and secondary winding. Therefore, the Y-cap can be removed and the sensation of numbness can be eliminated.

To further analyze the reason that the CM spectrum has behaviors that are not as good as those in the lower frequency ranges, the primary and secondary voltages are probed as shown in Fig. 17. It can be seen that high-frequency voltage spike oscillations exist in the primary and secondary winding voltages and that their corresponding frequencies are about 4 MHz and 17.875 MHz, respectively. The spike oscillations are caused by transformer leakage inductances in the primary and secondary windings. Therefore, the CM noise cancelation mechanics are no longer possible due to their different frequencies. The cancelation mechanics can be moved to higher frequency ranges if stronger RCD and RC snubbers are used in the circuit. In addition, for EMI designers, a reduction of the low-frequency is a lot more important. The EMI filter design is mainly depended on low-frequency EMI noise. The less low-frequency EMI noise, the less the cost and size of the EMI filter. Then the high-frequency EMI noise can be filtered by an EMI filter.

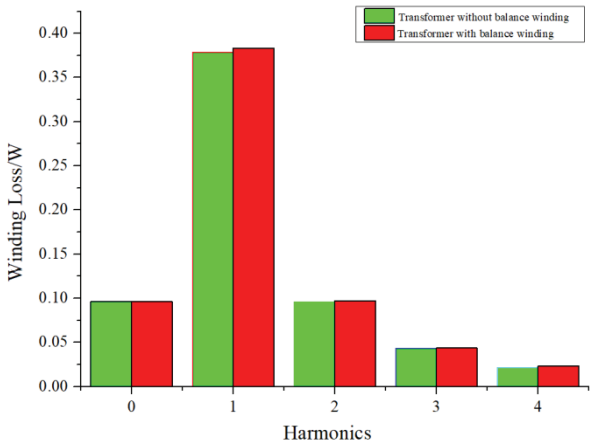


Fig. 18. Winding loss with harmonics.

C. *Winding loss Analysis*

Due to the existence of a high-frequency magnetic field between the adjacent primary and secondary winding layers, additional winding losses may be caused by the balance winding layers. To estimate the winding losses with the proposed balance winding, Finite Element Analysis (FEA) simulation results by Ansys Maxwell are shown in Fig. 18. The winding losses are simulated from DC to the fourth order harmonics.

When compared to a transformer without balance winding, the losses by the proposed noise balance winding are negligible. Therefore, the proposed balance winding scheme maintain the benefits of CM noise attenuation without a Y-cap and maintain a higher efficiency.

VII. Conclusions

For a flyback circuit using synchronous rectification, there is no inherent noise cancellation mechanism by the primary and secondary windings or partial shielding foil since the location change of the synchronous device in the secondary from the positive side to the negative (ground) side causes the phase of secondary CM noise source inversion.

The root cause of CM noise through the transformer is regarded as the resultant electric charges in the secondary winding conductors, which is induced by the electric field in winding window due to the voltage potential distributions in each turn of the transformer windings. To reduce the CM noise through the transformer, the induced resultant electric charges in the secondary winding conductors should be reduced.

The design guidelines of the balance winding scheme for the proposed method are very simple to implement whether in theoretical or simulation analysis. It is effective for greatly

reduce CM noise by the transformer coupling path so that the Y-cap can be removed. This scheme is also very easy to realize by simply inserting a balance winding layer in the adjacent primary and secondary winding layers and with suitable turn numbers by the principle that the average of voltage potential in the balance winding layer is equal to those of the adjacent secondary winding layer. For achieving the lowest CM noise, other factors such as the magnetic core, winding edge effects, the gap between the PCB traces in a layer and the distance between PCB layers should be considered in simulations.

Equivalent CM capacitance or dynamic capacitance between the primary and secondary windings C_Q is proposed to effectively evaluate the CM noise behaviors of a transformer. C_Q can be obtained by the reflection parameter S_{21} by a network analyzer or by simulation.

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