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Self-Feeder Driver for Voltage Balance in Series-Connected IGBT Associations

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Abstract

The emergence of high voltage conversion applications has resulted in a trend of using semiconductor device series associations. Series associations allow for operation at blocking voltages, which are higher than the nominal voltage for each of the semiconductor devices. The main challenge with these topologies is finding a way to guarantee the voltage balance between devices in both blocking and switching transients. Most of the methods that have been proposed to mitigate static and dynamic voltage unbalances result in increased losses within the device. This paper introduces a new series stack topology, where the voltage unbalances are reduced. This in turn, mitigates the switching losses. The proposed topology consists of a circuit that ensures the soft switching of each device, and one auxiliary circuit that allows for switching energy recovery. The principle for the topology operation is presented and experimental tests are performed for two modules. The topology performs excellently for switching transients on each of the devices. The voltage static unbalances were limited to 10%, while the activation/deactivation delay introduced by the lower module IGBT driver takes place in the dynamic unbalances. Thus, the switching losses are reduced by 40%, when compared to hard switching configurations.

Key words: Energy storage, IGBT, Power supplies, Snubber circuit, Soft switching circuits, Switching transients

I. INTRODUCTION

Series-connected MOSFET or IGBT associations have become a valid solution for high-voltage applications [1], [2]. Railway traction (>3 kV) [3], high-voltage direct current transmission (>100 kV) [4], and biological applications through electroporation [5], [6] are their most relevant current applications. The use of these topologies allows for total control of the switching position. Additionally, they are a low-cost alternative to silicon carbide devices.

The main drawbacks with these topologies are the static and dynamic voltage unbalances between devices [7], [8]. These unbalances produce uneven transistor wear, resulting in a decreased lifespan for the equivalent switching position [9]. When voltage unbalances are high, one or more of the devices in the arrangement may experience voltage magnitudes that are greater than their maximum operating rates, which can result in a breakdown [10]. The breakdown of a transistor results in an immediate failure of the entire arrangement [11].

Several methodologies have been proposed to achieve voltage unbalance reductions. These methodologies can be classified into two main groups: (a) compensation from the high-voltage side and (b) compensation from the gate side [12]. On the high-voltage side, both active and passive snubber networks are implemented [13]. These implementations increase the component switching time and result in considerable losses of the added passive elements. The addition, these elements increases the circuit size. Another alternative is to implement clamped voltage circuits by means of Zener diodes connected between the collector and the emitter or between the collector and the gate [14]. This alternative is limited to one voltage level, which is given by the breakdown voltage of the employed Zener diode. However, several compensation techniques have been developed from the gate side. Among the most effective of these techniques are the quasi-active gate control technique [15], the reference slope voltage control

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technique, and the master-slave control technique [16]. With these techniques, the collector-emitter voltages are measured by means of acquisition circuits. Through a comparison of these voltages, control signals are generated. This, in turn, gives rise to current injection into the gate of the transistor with the highest voltage level. The main inconvenience of these techniques lies in the fact that the devices operate in their linear zone, which increases the losses and wear. In addition, oscillations, which give rise to undesired transistor activation, may be generated in the control circuits.

Many of the techniques presented above, increase the switching losses. These losses are directly proportional to the switching frequency. Switching losses are notorious in high-frequency operations [17] and they have become the practical limitation for semiconductor device operation [18]. In addition to diminishing the performance of the transistor, switching losses become a major problem due to equipment temperature increases. As a result, either the size of the heat sinks must be increased, or very expensive cooling systems must be implemented [19]. Among the solutions for the switching losses problem are active and passive soft-switching circuits [20]. Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) in the transistor can be achieved with these circuits. Thus, the losses are quite low, which allows for operation at frequencies that are greater than those obtained with hard switching, which contributes to a power density increase [19].

Considering the above information, this paper presents a new topology for the association of series-connected IGBTs. This topology allows for: (a) adjustment of static and dynamic voltage unbalances, (b) reductions of switching losses by means of a soft-switching technique, and (c) recovery of the switching energy of all the transistors. The latter is achieved by means of a non-dissipative snubber network of the voltage balance on the high-voltage side. The energy accumulated in this network is sent back to the IGBT driver source. The working principle of the topology is described and compared to a hard-switching configuration via simulation. The association of the two devices has been experimentally validated.

The remainder of this paper is organized as follows. The working principle of the proposed topology is described in Section II. Prototype specifications are introduced in Section III, and the experimental validation is explained in Section IV. Finally, some conclusions are presented in Section V.

II. Operating Principle for the Topology Proposed for Series-connected IGBT Associations

Fig. 1 shows the general outline of the proposed topology. This outline is composed of *n* modules connected in series, where the modules are controlled by a single signal. In this topology, all of the modules work together synchronously, as an equivalent "switch".

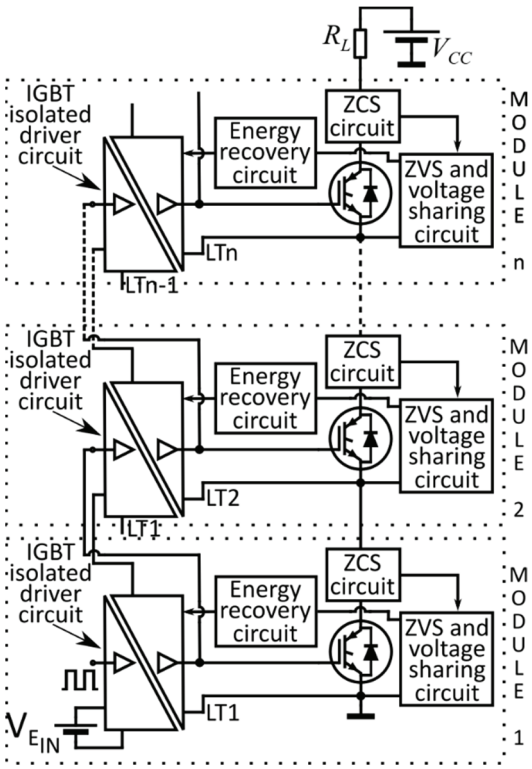

Fig. 1. Topology outline with *n* modules.

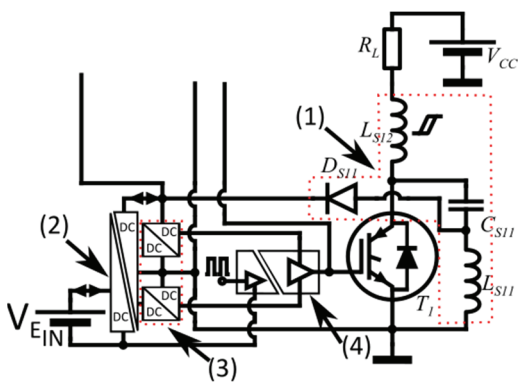

Fig. 2. Lower module of the proposed topology.

1) Switching aid circuit with an energy recovery system.
2) Bi-directional isolated dc-dc converter circuit.
3) Dc-dc converters.
4) IGBT driver circuit.

Fig. 2 shows the details of one of the modules. Each of the modules consists of the following circuits:

The switching aid circuit consists of three passive elements: L_{SI1} and C_{SI1} that make up the ZVS and voltage sharing circuit and the L_{SI2} saturable inductor that makes up the ZCS circuit. The interaction of these elements provides soft switching in both the 'on' and 'off' states of the IGBT. The saturation current element L_{SI2} is less than that of V_{CC}/R_L. This guarantees a maximum value of the inductance in switching to on, and a

very low inductance value during conduction. There is a power return from the high voltage side to the bidirectional dc-dc converter when the diode D_{SI1} is conducting.

The bi-directional dc-dc converter generates output voltages from two secondary windings. The two output voltages have equal magnitudes but different polarities. This converter supplies power to the those that feed the IGBT driver, and returns the energy accumulated in the switching aid circuit to its primary source, V_{EIN}. The output voltage of the bi-directional converter rises momentarily when energy is returned. This rise in voltage may result in damage to the driver or the IGBT gate if the maximum operating voltage rates are exceeded. Thus, two dc-dc converters are connected: one for each of the bi-directional converter outputs. This guarantees a constant input voltage for the IGBT driver.

In the proposed topology, each of the modules supplies the control signal and power supply voltage to the isolated IGBT driver circuit's upper neighboring module. This configuration ensures a similar value for the insulation voltage between the control and high voltage signals of each module. Under these conditions, all of the optocoupler modules of the topology driver are readily available on the market, and the level of the flyback converter insulation voltage is equal in all cases, which reduces the size of the control circuit. In the lower module, the control signal and the power supply voltage are provided from external sources.

In order to analyze the operating principle of the topology, the module shown in Fig. 2 is simplified, as shown in the circuit in Fig. 3. The activation switching slope v_{CE} of T_1 is approached by a straight line, and D_{SI1} is assumed to be ideal. The analysis is performed for two state transitions: conduction to blocking and blocking to conduction.

A. Switching on

$t < t_o$: T_1 and D_{SI1} are blocked, the capacitor C_{SI1} is loaded with a voltage value equal to V_{CC} ($v_{CSI1}(t_o)=V_{CC}$). Fig. 3 shows the initial stage of the circuit.

$t_o \le t < t_1$: When the activation command is given, T_1 conducts, and the circuit reaches Stage 2. The preloaded C_{SI1} capacitor transfers energy to the L_{SI1} inductor. The equations describing the L_{SI1} and L_{SI2} inductor current and voltage in the C_{SI1} capacitor are given in (1), (2) and (3):

$$i_{L_{S11}}(t) = \frac{V_{CC}}{\sqrt{L_{S11}/C_{S11}}} sin((\sqrt{1/L_{S11}C_{S11}})t) \quad (1)$$

$$i_{L_{S12}}(t) = \frac{V_{CC}}{R_L}\left(1 - e^{\frac{-R_L}{L_{S12}}t}\right) \quad (2)$$

$$v_{C_{S11}}(t) = V_{CC} cos((\sqrt{1/L_{S11}C_{S11}})t) \quad (3)$$

The current in the transistor evolves in accordance with the below equation:

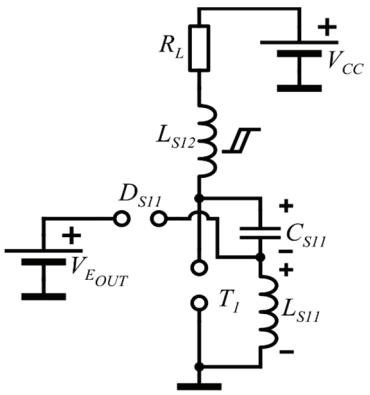

Fig. 3. Stage 1: T_1 and D_{SI1} are blocked.

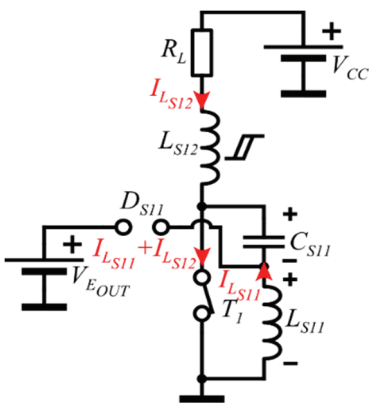

Fig. 4. Stage 2: T_1 is conducting and D_{SI1} is blocked.

$$i_{T_1}(t) = i_{L_{S11}}(t) + i_{L_{S12}}(t) \quad (4)$$

Fig. 4 shows the position of D_{SI1} and T_1 in circuit Stage 2. In this interval, D_{SI1} is blocked, while T_1 conducts.

$t_1 \le t < t_2$: Equations (1), (2), (3) and (4) are valid until $v_{CSI1}(t)=-V_{EOUT}$. From this point on, the D_{SI1} diode conducts and yields new equations that describe the circuit behavior:

$$i_{L_{S11}}(t) = \frac{-V_{EOUT}}{L_{S11}}(t - t_1) + i_{L_{S11}}(t_1) \quad (5)$$

$$i_{L_{S12}}(t) = \frac{V_{CC}}{R_L} \quad (6)$$

$$v_{C_{S11}}(t) = -V_{EOUT} \quad (7)$$

$$i_{T_1}(t) = i_{L_{S12}}(t) \quad (8)$$

In this interval, the energy accumulated in the L_{SI1} inductor is delivered to the V_{EOUT} source. This energy is approximately equal to:

$$W_1 = \frac{1}{2} i_{L_{S11}}(t_1) * (t_2 - t_1) * V_{EOUT} \quad (9)$$

Fig. 5 shows this stage of the circuit. In this case, the D_{SI1} diode and the T_1 transistor are in conduction.

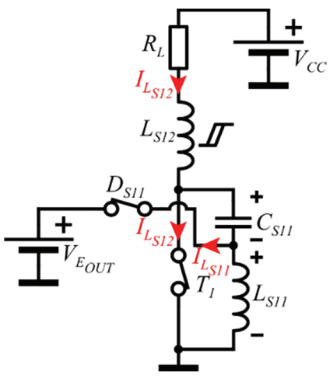

Fig. 5. Stage 3: T_1 and D_{S11} are in conduction.

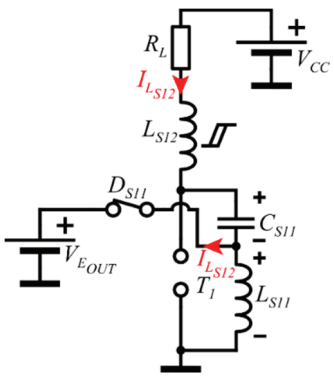

Fig. 6. Stage 5: Blocking of the T_1 transistor.

B. Switching off

$t_2 \le t < t_3$: The T_1 opening command can only be given if L_{S11} has been fully discharged into the V_{EOUT} voltage source, $i_{LS11}(t_2) = 0$. Under this condition, D_{S11} turns off yielding Stage 4. In this stage, the circuit returns to the state shown in Fig. 4. A small current circulates through L_{S11}, due to the energy accumulated in C_{S11}. The equations that describe the behavior of the system at this stage are:

$$i_{L_{S11}}(t) = \frac{V_{EOUT}}{\sqrt{L_{S11}/C_{S11}}} sin((\sqrt{1/L_{S11}C_{S11}})t) \quad (10)$$

$$i_{L_{S12}}(t) = \frac{V_{CC}}{R_L} \quad (11)$$

$$v_{C_{S11}}(t) = V_{EOUT} cos((\sqrt{1/L_{S11}C_{S11}})t) \quad (12)$$

$$i_{T_1}(t) = i_{L_{S11}}(t) + i_{L_{S12}}(t) \quad (13)$$

$t_3 \le t < t_4$: The D_{S11} diode goes into conduction when the command to open is given to T_1, $v_{LS11}(t)=V_{EOUT}$. The new state variable equations are:

$$i_{L_{S11}}(t) = 0 \quad (14)$$

$$i_{L_{S12}}(t) = B_1 e^{S_1 t} + B_2 e^{S_2 t} \quad (15)$$

$$v_{C_{S11}}(t) = V_{CC} - B_3 e^{S_1 t} - B_4 e^{S_2 t} \quad (16)$$

Where:

$$S_{1,2} = -\frac{R_L}{2L_{S12}} \pm \sqrt{\left(\frac{R_L}{2L_{S12}}\right)^2 - \frac{1}{L_{S12}C_{S11}}}$$

$$B_1 = \frac{V_{CC}}{R_L}\frac{S_2}{S_2 - S_1};\ B_2 = \frac{V_{CC}}{R_L}\frac{S_1}{S_1 - S_2}$$

$$B_3 = \frac{V_{CC}}{R_L C_{S11}}\frac{1 + R_L C_{S11} S_2}{S_2 - S_1};\ B_4 = \frac{V_{CC}}{R_L C_{S11}}\frac{1 + R_L C_{S11} S_1}{S_1 - S_2}$$

The transistor opening is adjusted to the voltage function of the C_{S11} capacitor. The energy transferred to the V_{EOUT} source in the new D_{S11} diode conduction interval is approximately equal to:

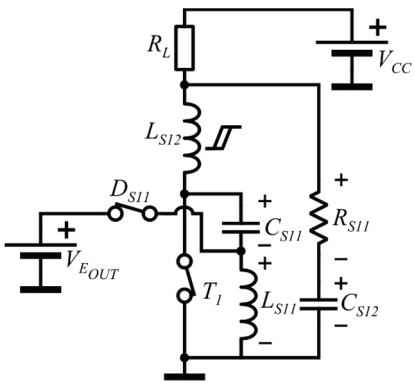

Fig. 7. Circuit with an additional *RC* snubber network.

$$W_2 = V_{EOUT} \int_{t_3}^{t_4} (i_{L_{S12}}(t) - i_{T_1}(t))dt \quad (17)$$

Fig. 6 shows the blocking stage of the T_1 transistor.

The energy transfer to V_{EOUT} is performed until C_{S11} is fully charged. Once this condition is fulfilled, the D_{S11} diode is blocked and a new switching operation cycle begins.

C. Addition of an RC Snubber Network

The gate control signal in each of the modules is delayed in receiving that signal from its lower neighboring module signal. This delay causes the transistors to enter into sequential conduction once the command to turn on is given. The difference between activation times generates a momentary rise in the v_{CE} voltage in higher module transistors. An *RC* snubber network is added in parallel on the high-voltage side of each module in order to avoid this overvoltage. Fig. 7 shows the lower module with the addition of a snubber network.

The power that dissipates in the R_{S11} snubber network resistance is given by:

$$P_{sn} = C_{S12} * V_{CC}^2 * f \quad (18)$$

The R_{S11} and C_{S12} values are adjusted so that the smallest possible amount of energy is dissipated in the resistor. Thus, these values fulfil their objective. C_{S12} is as small as possible.

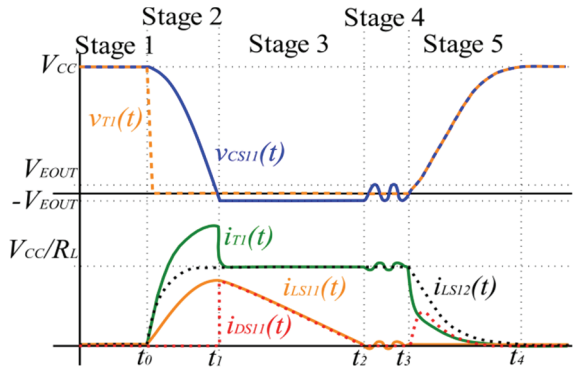

Fig. 8. Voltage signals in the C_{S11} capacitor, current in the L_{S11} and L_{S12} inductors, and voltage and current in the T_1 transistor.

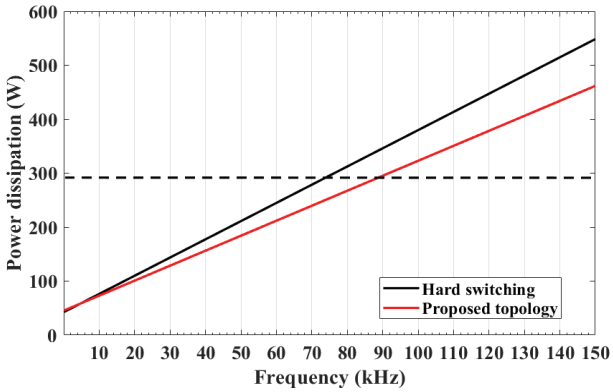

Fig. 9. Power dissipation for the IGBT vs the switching frequency.

Fig. 8 shows transistor current and voltage waveforms, as well as their state variables in the lower module of the topology.

From t_o, the i_{T1} current is displayed in a rising curve, as a function of the value of the L_{S12} saturable inductor while the v_{T1} voltage changes rapidly. This guarantees soft switching to 'on' ZC(on). In the interval between t_o and t_1 (before D_{S11} enters conduction), the non-dissipative snubber current flows through the transistor, which generates a current elevation. This elevation increases the conduction losses and becomes a fundamental parameter in the selection of the transistor and C_{S11} and L_{S11} values. From t_3, (blocking signal), the v_{T1} voltage evolves slowly as a function of C_{S11}, while the i_{T1} current changes rapidly until L_{S12} is cut off at saturation and the tail current of the IGBT appears. The C_{S11} capacitor helps to smooth the switching to blocking ZV (off).

A simulation test was carried out using the LTSpice XVII software, in order to determine the IGBT losses as a function of the switching frequency. International Rectifier provided the SPICE model for the IGBT *IRGPS60B120KD*. The proposed topology was implemented using two modules in series, as shown in Fig. 11. A second series-association topology (hard switching configuration) was simulated with a synchronized control signal in each of the IGBTs. This is done without unbalance-correction elements on the high voltage side, and without regard for the practical restrictions of voltage isolation, in order to establish a comparative framework. The supply voltage V_{CC} was 2 kV in both topologies, the load resistance was 660 Ω and the duty cycle was maintained at a constant value of 0.5. A switching frequency variation was made from 0.1 to 150 kHz, and the power dissipation was measured in each IGBT.

Fig. 9 shows a switching frequency vs power dissipation graph in an IGBT (worst case scenario) with the proposed topology (red line) and an IGBT in an idealized topology of the reference (black line).

Fig. 9 shows that IGBTs with frequencies above 10 kHz have lower losses when the proposed topology is employed. The proposed topology (equivalent "switch") form part of different conversion systems in power electronics. Considering this, and in accordance with Fig. 9, there are two operation alternatives. The first alternative is increasing the commutation frequency. This allows for an inductor and transformer size reduction in the conversion system implemented, by means of an equivalent "switch". The second alternative is for low frequency applications where it is possible to reduce the heat sink size. Either of these cases guarantee that the IGBT is in its Secure Operation Area (SOA), and that there is a contribution to increase the power density of the implemented conversion system.

Losses in the cores of the inductors and in the snubber network are very low when compared to the transistor losses. Simulation tests show greater efficiency in the proposed topology than in the hard-switching topology for switching frequencies above 10 kHz.

TABLE I
KEY EXPERIMENTAL PROTOTYPE PARAMETERS

L_{S11}/L_{S21}	L_{S12}/L_{S22}	C_{S11}/C_{S21}	C_{S12}/C_{S22}	R_{S11}/R_{S21}	R_L
15 uH	2.4 uH	4.7 nF	2.2nF	100 Ω	70 Ω

III. PROTOTYPE SPECIFICATIONS

A two-module series stack prototype was built in order to validate proposed topology.

In the development of the prototype, T_1 and T_2 are *IRGPS60B120KD* IGBTs, D_{S11} and D_{S21} are *UF4007* diodes, and the IGBT drivers are *FOD3184*. The values of the switching circuit passive components and load resistance are shown in Table I.

L_{S11} and L_{S21} were built in EE3007 cores, while L_{S12} and L_{S22} were built in E2005 cores. The inductors were built in line with the procedure developed by Tacca in [21].

The bi-directional converters are the IGBT drivers isolated power supply. The bi-directional converters are very simple and might even be flyback-type converters. The circuit used in the prototype is contained in Appendix. A Greinacher multiplier is utilized as the high voltage source [22].

TABLE II
PROTOTYPE DESIGN SPECIFICATIONS

Maximum operating voltage	2 kV
Maximum operating current	40 A
Maximum operating frequency	50 kHz
Maximum voltage in IGBT driver	15 V
Minimum pulse width	15 us

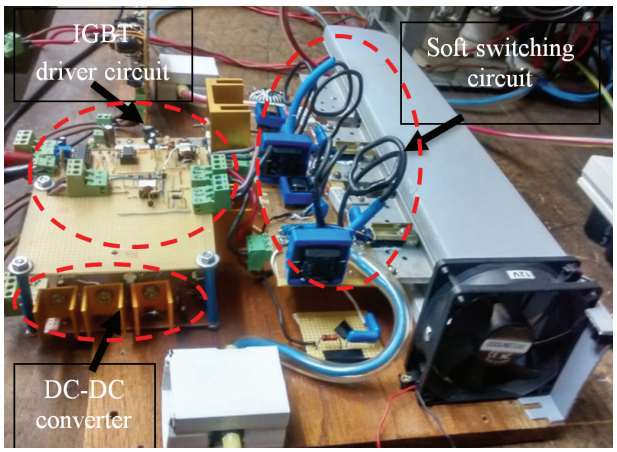

Fig. 10. Experimental prototype.

Table II shows the prototype operating ranges. Fig. 10 shows the experimental prototype.

IV. EXPERIMENTAL VALIDATION

Measurements were made using a Fluke 190 scopometer with 1 kV, 200 MHz voltage probes, and a 70 A, 1 MHz Pintek 699 current probe. Testing was performed using three different values for the V_{CC} voltage: 1 kV, 1.5 kV and 1.8 kV. Fig. 11 shows a diagram of the circuit built, including the points where the voltage and current measurements were taken.

A. Voltage Balance

The collector-emitter voltage waveforms were recorded in the first test during switching to conduction. This test was performed using the topology without the snubber network. Fig. 12 shows the $v_{CE1}(t)$ and $v_{CE2}(t)$ voltages in switching to conduction.

Voltage $v_{CE2}(t)$ shows both a peak and a delay, with respect to $v_{CE1}(t)$, during switching due to the propagation delay time to a high output level (t_{PLH}) of Module 1's IGBT gate driver in the T_2 gate signal. The momentary overvoltage is eliminated with the addition of the snubber network. Fig. 13 shows the $v_{CE1}(t)$ and $v_{CE2}(t)$ waveforms after modification.

The power at 2.2 W is dissipated in the resistance of the snubber *RC* network for each of the modules with a test switching frequency of 2 kHz. The delay between the signals is always present, and this is one of the constraints for

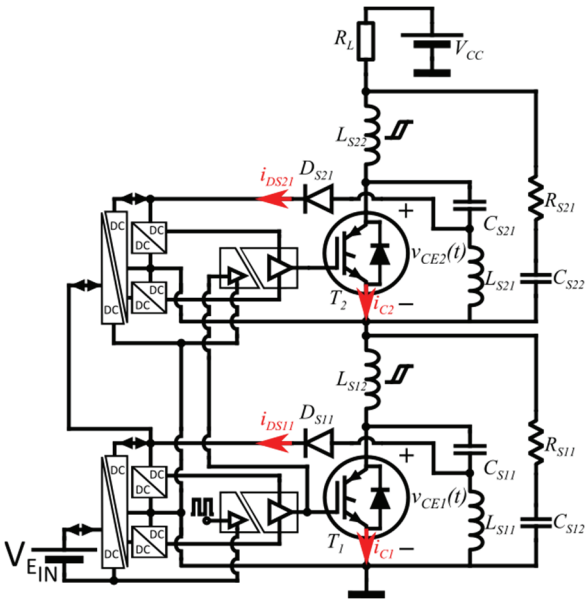

Fig. 11. Diagram of the circuit built.

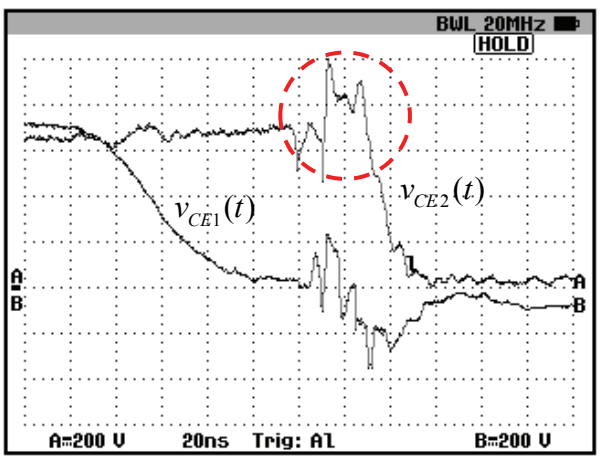

Fig. 12. Voltage in T_1 and T_2 in switching to conduction (topology without the *RC* snubber network).

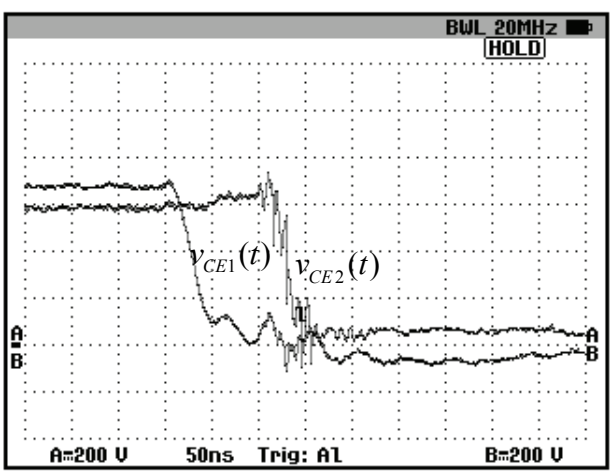

Fig. 13. $v_{CE1}(t)$ and $v_{CE2}(t)$ waveforms after addition of the *RC* snubber network.

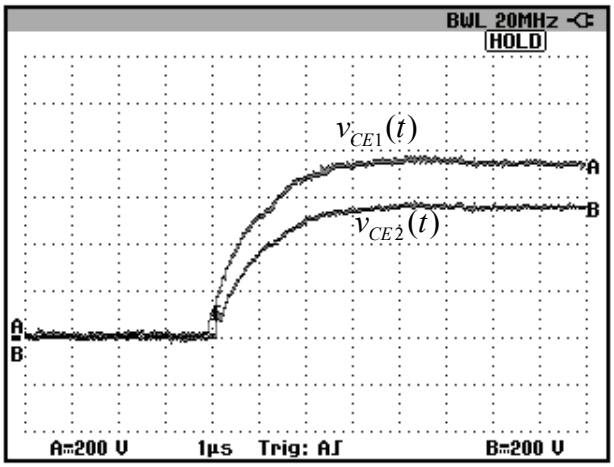

Fig. 14. Voltages $v_{CE1}(t)$ and $v_{CE2}(t)$ in switching to blocking.

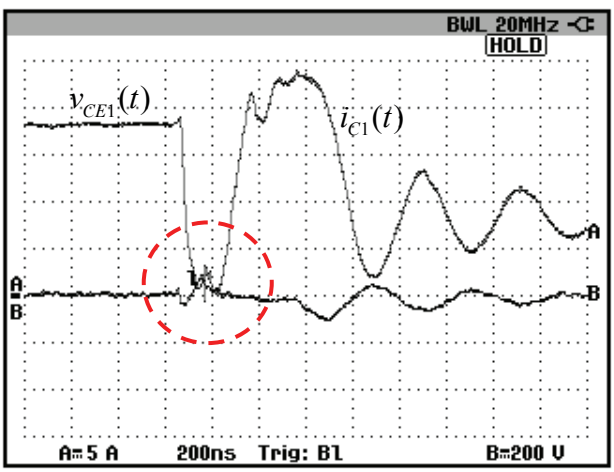

Fig. 15. T_1 voltage and current in switching to conduction.

deciding the maximum number of modules to connect, within the topology. There is a difference between the two voltage slopes during the switching to 'off'. This difference is preserved while the devices are blocked. The voltage difference never exceeds 10%. Fig. 14 shows voltage waveforms in switching to blocking.

B. Switching ZC(ON)-ZV(OFF)

Fig. 15 and Fig. 16 show voltage and current waveforms at T_1 and T_2 in switching to conduction. It should be noted that the current waveforms in each of the modules were measured on different scales.

The saturable inductor regulates the current transistor slope during switching to 'on', while the voltage decreases to zero. This effect produces switchings with very low losses in the transistors.

The $v_{CE1}(t)$ voltage increases as a function of the $v_{CS1}(t)$ voltage during the change from switching to blocking, while $i_{C1}(t)$ decreases as a function of the saturable inductor current. Fig. 17 shows $v_{CE1}(t)$ and $i_{C1}(t)$ waveforms.

$i_{C1}(t)$ decreases rapidly, due to the initial saturation

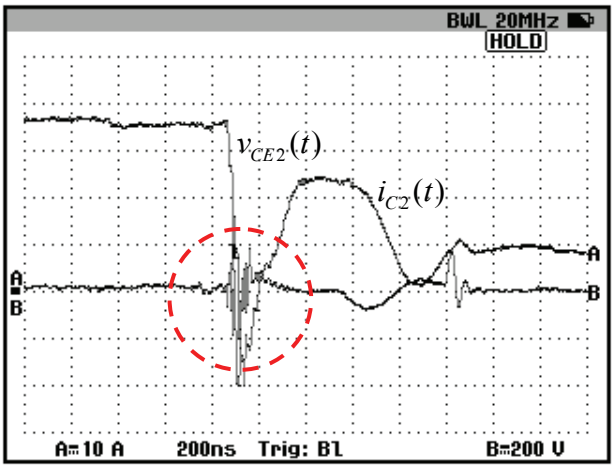

Fig. 16. Voltage and current for T_2 in switching to conduction.

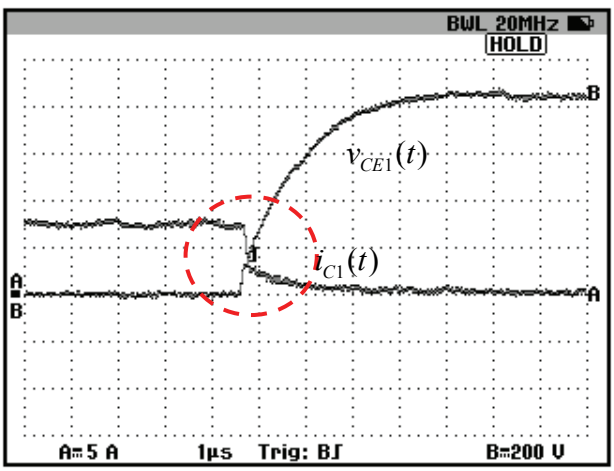

Fig. 17. Voltage and T_1 current during the change from switching to blocking.

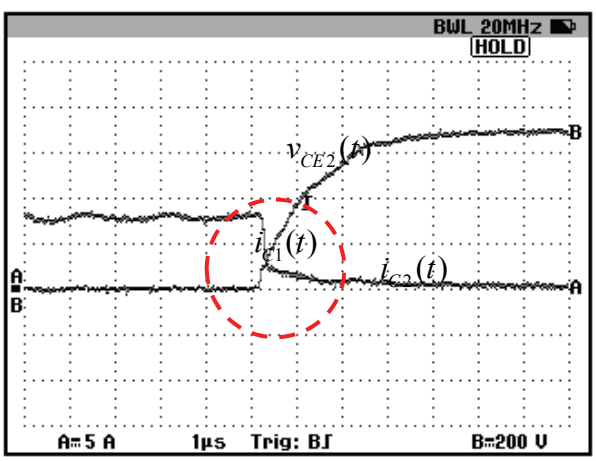

Fig. 18. T_2 voltage and current during the change from switching to blocking.

condition of the L_{S2} inductor. The L_{S2} inductor and the IGBT tail current delay the evolution of the current when it has been decreased by approximately 70% of its maximum value.

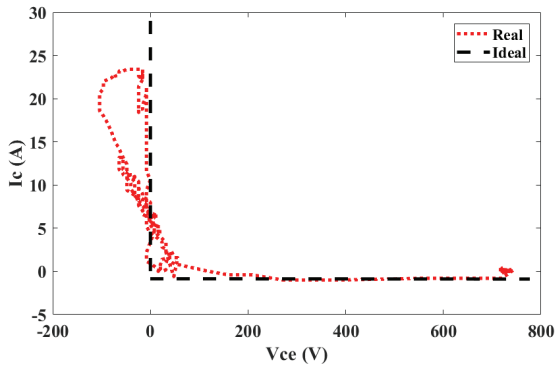

Fig. 19. Lissajous voltage and current curves in the T_1 transistor during switching to 'on'.

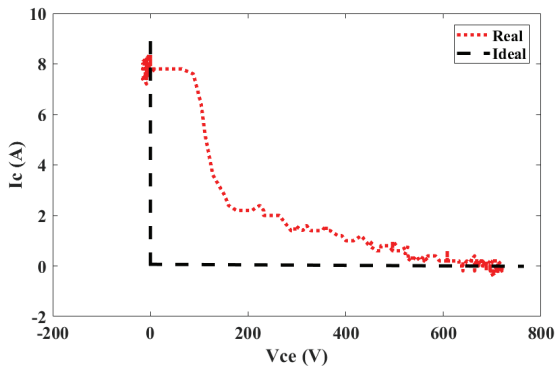

Fig. 20. Lissajous voltage and current curves in the T_1 transistor during switching to 'off'.

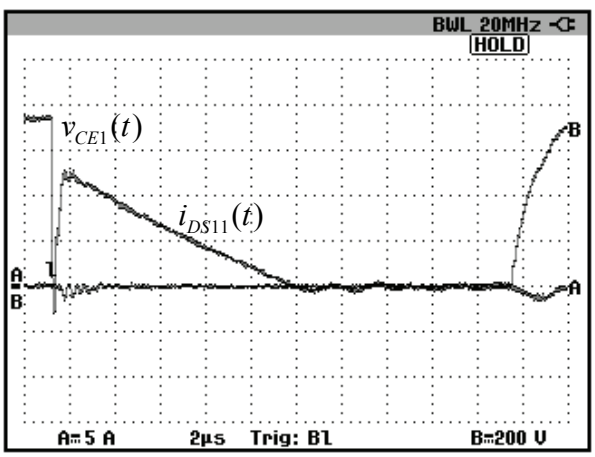

Fig. 21. Recovery of the switching energy in Module 1.

The same behavior is observed in the transistor voltage and current in Module 2. Fig. 18 shows voltage and current waveforms in the Module 2 transistor.

Voltage and current *Lissajous* curves are generated from the voltage and current in transistors. This is done in order to clearly determine the switching softness or hardness. Fig. 19 shows T_1 voltage and current curves during switching to 'on'.

In ideal soft switching, the curve is placed on the axes corresponding to the zero voltage and zero current. Fig. 19 shows nearly ideal soft switching. The losses, in this case are reduced by 76% when compared to hard switching.

The diagram in Fig. 20 shows a switch that is not completely soft during switching to 'off'. This is due to the effect of the IGBT tail current. Despite this, the losses during this switching process are reduced by 32% when compared to hard switching.

Considering the obtained switching loss reduction, the equivalent "switch" can reach switching frequencies of up to 90 kHz. This frequency is 40% higher than that achieved in similar applications that use hard switching.

C. Switching Energy Recovery

The current in the D_S diodes was measured in each of the modules in order to verify the energy recovery from the high-voltage circuit to the converters that feed the IGBT driver. Fig. 21 shows the transistor collector-emitter voltage, and the current in Module 1's D_S diode.

Fig. 21 shows that the IGBT conduction time is limited by the L_{S11} discharge time on V_{EOUT}. This limitation restricts the value of the duty cycle and/or switching frequency of the equivalent "switch".

An acceptable decrease of the static and dynamic voltage unbalances may be observed in the experimental results. This topology exhibits reduced switching losses due to the soft switching condition in all of the IGBTs. This decrease in the switching losses allows the equivalent "switch" to operate at frequencies that are higher than those achieved with hard switching configurations. The energy recovered from the switching aid circuit can be utilized to recharge a battery and to supply power to the IGBT driver circuit. Previous checks have established that the energy recovered from switching frequencies above 1 kHz exceeds the value required for IGBT driver operation. Experimental results and topology simulations using an additional storage module will be provided in a future paper.

V. Conclusions

A new topology for series stacks of power semiconductor devices was described and tested in this paper. Adequate topology performance was demonstrated through experimental testing with the implementation of two modules. The simplicity of this implementation, as well as the reduced losses of the static and dynamic voltage unbalances of the correction circuit are the two main advantages of this topology.

The conduction time for each of the IGBTs is limited by the L_{S11} inductor discharge time on the V_{EOUT} source. This behavior is generalized in each module. This time parameter determines the frequency and maximum duty cycle on the equivalent "switch". Based on the design values used in this paper, the maximum switching frequency for a 0.9 duty cycle is 90 kHz.

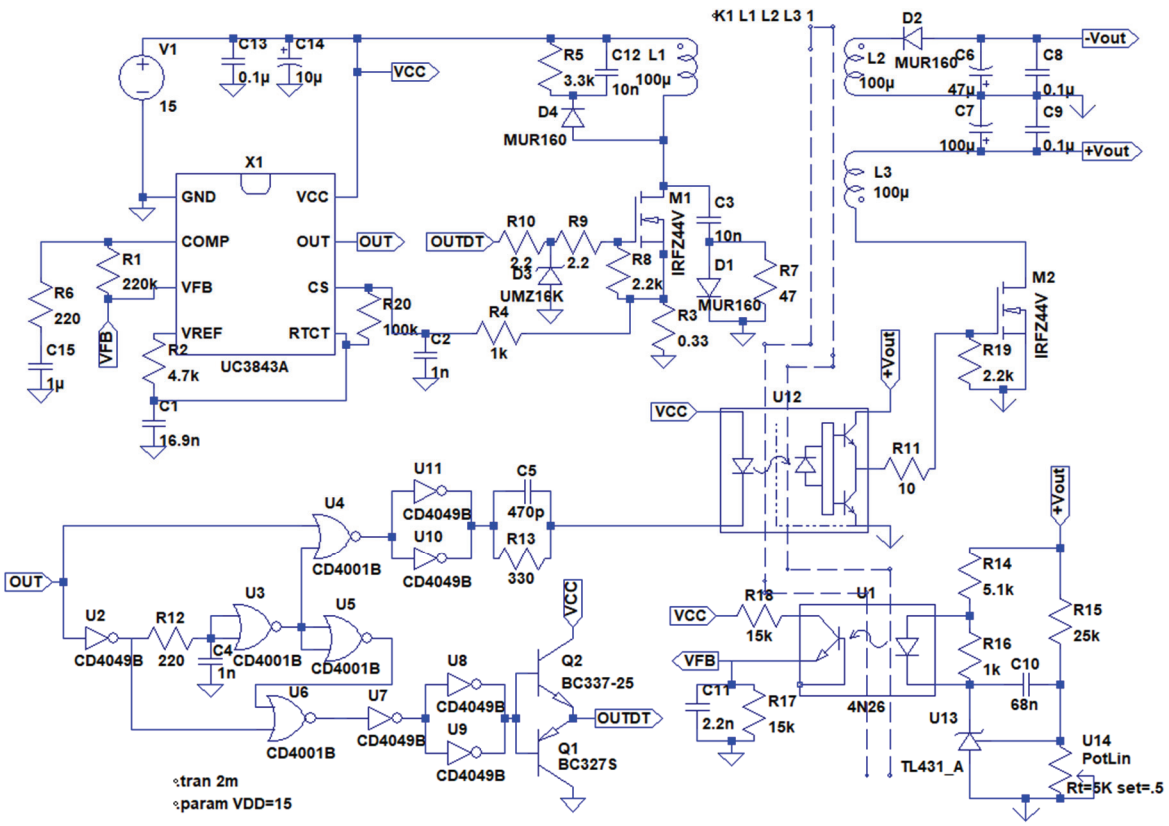

Fig. 22. Schematic of the bi-directional flyback converter.

The switching delay induced by the IGBT driver at each module results in an increase in the equivalent "switch" time. This increase must be considered as additional data for determination of the number of modules to be connected.

Part of the IGBT power switching is directed to the IGBT driver supply power circuit in each module. The switching losses are reduced when soft switching is achieved in both the IGBT 'on' and 'off' positions. In addition to reducing losses, there is a decrease in the electromagnetic interference, which can affect the control circuit and other systems external to the "switch".

APPENDIX

Fig. 22 shows the schematic of the bi-directional flyback converter used for the experimental tests. This converter is bi-directional only at the positive output ($+V_{EOUT}$). This schematic was developed by using the software LTspice XVII.

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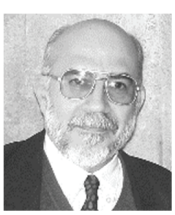

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