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# Analysis and Modeling of AC–AC Switched Capacitor Converters

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**Abstract**

A new modeling method for AC–AC switched capacitor converters (SCCs) is introduced in this study. The proposed analytical method aims to accurately describe the input–output characteristics of AC–AC SCCs and establish a mathematical model for static voltage conversion ratio and equivalent resistance, which are key performance metrics for SCCs. A quantitative analysis of converter regulation capability is addressed on the basis of the modeling method. In this analysis, the effects of the control parameters and individual components on SCCs are illustrated extensively. Component stresses, such as the peak value and transient variation of the voltage/current of the converter, are also presented. The effectiveness of the proposed method is verified by comparing it with the existing modeling method and applying it to an AC–AC SCC with a conversion ratio of three. Two 1 kW prototypes are built in a laboratory, and their experimental results exhibit good agreement with the theoretical analysis.

**Key words:** AC–AC converters, Modeling, Switched capacitor, Transient analysis

## I. INTRODUCTION

Switched capacitor converters (SCCs) have been an important research topic for many years. They present the advantages of high power density, small size, and low weight due to the absence of inductors or transformers [1]. Different circuit models have been presented for DC–DC SCCs [2], [3]. Applications that benefit from the switched capacitor (SC) principle include power supplies for mobile electronic systems, electric vehicles, and battery equalizer circuits [4]-[8]. Reference [9] extended the SC principle to AC–AC static conversion for the first time. This literature presented a brief analysis and the experimental results of a step-down/step-up converter. On the basis of [9] and by using bidirectional switches, a new SC-based bidirectional AC–AC static power converter with novel characteristics, such as the stress voltages on the components being equal to half of the high-side voltage and the use of a single SC leg, was introduced in [10]. SCCs have also been used in three-phase systems for high-power applications [11]-[13].

An SCC is characterized by a conversion ratio and an equivalent resistance [14], as shown in Fig. 1, which are determined by a selection of switching frequency, duty cycle, and other component parameters. An understanding of the basic mechanisms is crucial to achieve optimized performance. Previous studies have provided several modeling methods for DC–DC SCCs. A unified state-space averaging approach for switching mode converters, which combined the state-space and averaging methods, was presented in [15], but the derived mathematical model did not consider switching frequency. References [16] and [17] offered a behavioral average circuit model, which is valid for SCCs within all operational ranges, but is limited by the derivation assumptions that subcircuits can be described or approximated by a first-order resistor–capacitor circuit. Another modeling approach addressed in [18] analyzes an individual SC cell to derive an equivalent resistance formula for various operation modes but cannot be used to provide generic symbolic results for a complete converter. The charge-balance transient-calculation modeling method introduced in [19] and elaborated in [20] provides an accurate prediction of circuit behavior under varying duty cycle and frequency conditions; this method has been applied to obtain a steady-state model and peak current formulas. Nevertheless, modeling methods for SCCs that are implemented for static AC–AC conversion are rarely found in the literature.

Motivated by References [19], [20], the primary objective

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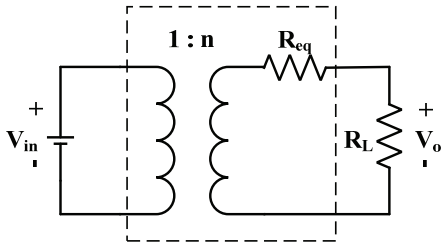



Fig. 1. Ideal model of an SCC.

of the current study is to find an appropriate modeling method for AC–AC SCCs. The input–output characteristics of AC–AC SCCs can be accurately described using the proposed method. A mathematical model is also built for calculating static voltage conversion ratio and equivalent resistance. The major characteristics and transient behavior of the converter are analyzed in detail. The impacts of the electric elements on the converter are also illustrated. Component stresses, such as the voltage variation and peak voltage value of the capacitors, are addressed in detail to enhance the understanding of SCCs. The experimental results confirm the correctness of the proposed modeling method.

## II. Modeling of an AC–AC SCC with a Conversion Ratio of Two

In this section, a typical step-up AC–AC SCC, as shown in Fig. 2(a), is analyzed using the conventional and proposed methods. The analyzed converter has a single SC cell, and complex converters that consist of multistage SC cells can be generated. The converter has four groups of bidirectional switches, and each group consists of two metal-oxide-semiconductor field-effect transistors (MOSFETs) that share a common source.

The expected low-frequency waveforms of the input–output voltages and the voltages across the capacitors are presented in Fig. 2(b), with the input voltage as the peak value. The gate drive signals and the operational high-frequency waveforms of the capacitors are shown in Figs. 2(c) and 2(d).

Three operational modes, namely, partial charge (PC), no charge, and complete charge (CC), exist for the capacitors depending on the relationship between the duration and the time constant [17]. The converter analyzed in this section operates in PC mode due to the trade-off between performance and cost.

To simplify the analysis, all MOSFETs are assumed to have the same on resistance $R_{dson}$ and all capacitors have the same capacitance $C$ and equivalent series resistance (ESR).

### A. Conventional Modeling Method

In accordance with the modeling method presented in [18] and its application example in [10], the equivalent resistance of the circuits shown in Fig. 2(a) is defined in (1) for different duty cycle values.

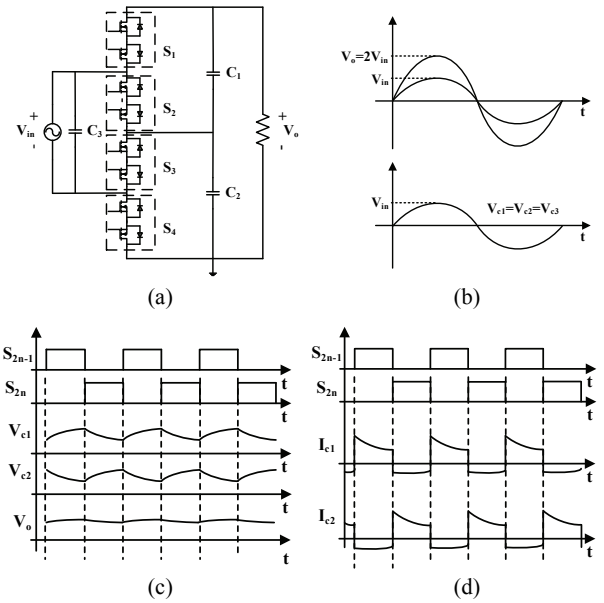



Fig. 2. Topology of the analyzed AC–AC SCC and operational high-frequency waveforms of capacitors: (a) Step-up converter; (b) Low-frequency input–output voltages and voltages across the capacitors; (c) Voltages; (d) Currents.

$$R_{eq} = \frac{1}{f_s \cdot C} \cdot \frac{(1 - e^{-1/f_s \cdot 2 \cdot R_{on} \cdot C})}{1 - (e^{-D/f_s \cdot 2 \cdot R_{on} \cdot C} + e^{-(1-D)/f_s \cdot 2 \cdot R_{on} \cdot C}) + e^{-1/f_s \cdot 2 \cdot R_{on} \cdot C}}, \quad (1)$$

where $f_s$ is the switching frequency, $R_{on}$ is the total on resistance of a bidirectional switch that is twice that of a MOSFET, and $D$ is the duty cycle.

When $D$ is fixed at 0.5, the limit value of the equivalent resistance is

$$R_{eq(D=0.5)\_\min} = \lim_{f_s \to \infty} R_{eq} = 8 \cdot R_{on}. \quad (2)$$

### B. Proposed Modeling Method

A new modeling technique for conversion ratio and equivalent resistance based on the state equations derived from Kirchhoff's current law (KCL) and Kirchhoff's voltage law can be used for the circuit in Fig. 2(a). This modeling technique for AC–AC SCCs can also be used to model its DC–DC counterpart due to the similar subcircuits and operating principle.

The converter has two operational stages. The subcircuits are presented in Fig. 3. Stage 1, as shown in Fig. 3(a), starts when switches $S_1$ and $S_3$ are turned on and capacitor $C_1$ is charged by the input voltage source throughout the stage. Accordingly,

$$V_{in} = V_{c1}(t) + (2R_{on} + r)(C\frac{dV_{c1}(t)}{dt} + I_L), \quad (3)$$

where $r$ is the ESR of the capacitor.

When the boundary condition is considered,

$$V_{c1}(0) = V_{c1\min} . \quad (4)$$

The switching frequency is relatively higher than the grid frequency; therefore, the input voltage is assumed to be constant during a switching period, and the following equation can be derived:

$$V_{c1}(t) = e^{-\frac{t}{C(2R_{on}+r)}}(2I_L R_{on} + V_{c1\min} - V_{in}) + V_{in} - 2R_L R_{on} . \quad (5)$$

The maximum voltage of $C_1$ can be derived as

$$V_{c1\max} = V_{c1}(D\,T_s) . \quad (6)$$

Given the subcircuits in Fig. 3(b), the charge stored in $C_1$ is delivered to $C_2$ during Stage 2 [$DT_s$, $T_s$]. The following equation based on charge balance can be derived:

$$C(V_{c1\max} - V_{c1\min}) = (1-D)T_s I_L . \quad (7)$$

The voltage across the load is nearly imperceptible; thus, the load current can be assumed to be a constant current source.

$$I_L = \frac{V_o}{R_L} \quad (8)$$

The analyzed converter is symmetrical; hence, the output voltage can be expressed as

$$V_o = V_{c1\max} + V_{c1\min} . \quad (9)$$

From (3)–(9), the conversion ratio of the projected converter can be derived as

$$\frac{V_{out}}{V_{in}} = \frac{4CR_L}{2C(4R_{on}+R_L) + \frac{(1-D)}{f_s}\mathrm{Coth}[\frac{D}{2f_sC(2R_{on}+r)}] + \frac{D}{f_s}\mathrm{Coth}[\frac{(1-D)}{2f_sC(2R_{on}+r)}]} . \quad (10)$$

When $R_L \to \infty$, the ideal conversion ratio of the converter can be obtained as

$$G_{ideal} = \lim_{R_L\to\infty}\frac{V_o}{V_{in}} = 2 . \quad (11)$$

From the idealized model of SCC in Fig. 1, the equivalent resistance can be derived as

$$R_{eq} = R_L(\frac{2}{G}\text{-}1) = \frac{1}{2C}[8CR_{on} + (1-D)T_s\,\mathrm{Coth}(\frac{DT_s}{2C(2R_{on}+r)}) + DT_s\,\mathrm{Coth}(\frac{(1-D)T_s}{2C(2R_{on}+r)})] . \quad (12)$$

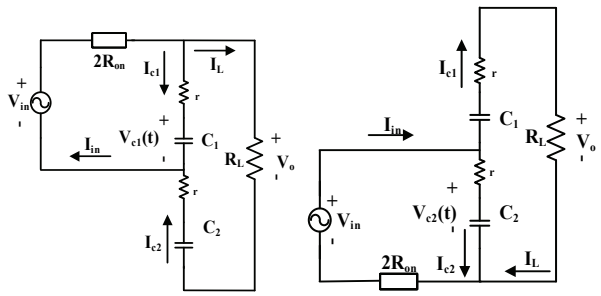



Fig. 3. Subcircuits of an SCC: (a) Stage 1; (b) Stage 2.

TABLE I
COMPONENT PARAMETERS FOR THE THEORETICAL ANALYSIS AND EXPERIMENTS

| Fig. 4 | $V_{in\_rms}$ (V) | $f$ (Hz) | $f_s$ (kHz) | $R_{on}$ (Ω) | $C$ (μF) | $D$ | $R_L$ (Ω) |
|---|---|---|---|---|---|---|---|
| (a) | 110 | 50 | 50 | 0.07 | 10 | 0.05–0.5 | 100 |
| (b) | 110 | 50 | 50 | 0.07 | 10 | 0.05–0.5 | 100 |

When $D$ is fixed at 0.5 and $f_s$ approaches infinity, the minimum limit of equivalent resistance can be derived as

$$R_{eq\min} = \lim_{f_s\to\infty} R_{eq(D=0.5)} = \lim_{T_s\to 0} R_{eq(D=0.5)} = 8R_{on} . \quad (13)$$

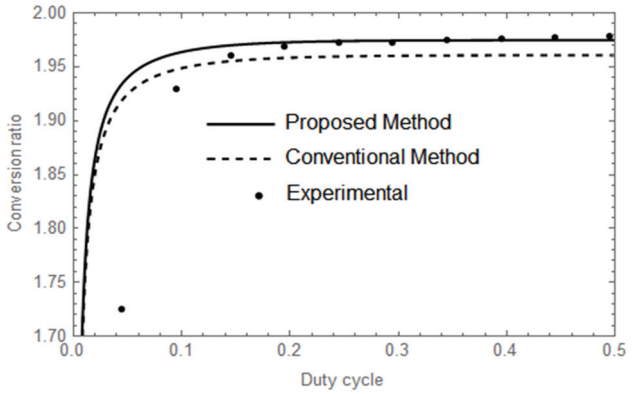
The deduced limit value of equivalent resistance presented in (13) coincides with that in (1), which is 16 times of a single MOSFET's on resistance.

The modeling method is also valid for an SCC with a step-down configuration.

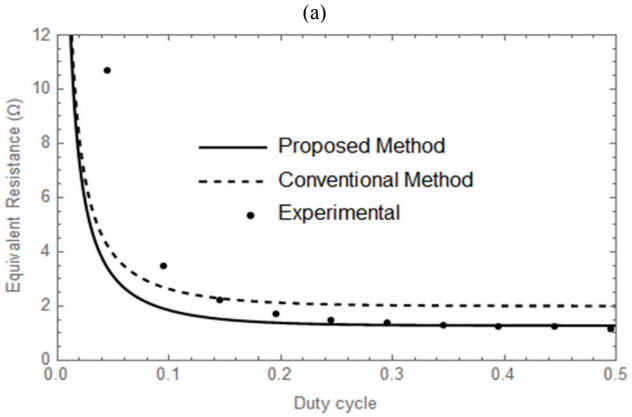
### C. Comparison Study of the Two Methods

The two modeling methods include frequency and duty cycle regulation and involve the impacts of capacitors, on resistance, duty cycle, and switching frequency. A comparison of equivalent resistance between the two modeling methods under varying duty cycle and switching frequency conditions is presented in Fig. 4 and the experimental curve. The component parameters selected for the theoretical analysis and experiments are provided in Table I.

The curves in Fig. 4 show that compared with the conventional modeling method, the proposed method tends to exhibit better agreement with the experimental results. The primary reason for the imprecision of the conventional method is that the voltage ripples in $C_2$ and $C_3$ are assumed to be constant in the modeling process, and the ESR of the capacitors is disregarded. Discrepancies in the proposed method occur when the duty cycle is between 0.05 and 0.10 because the actual value of the duty cycle deviates from the setting value as the impacts of finite dead time, rise time, and fall time become significant when $D$ tends to approach zero (or is extremely small). Nevertheless, the proposed method is suitable for the modeling of AC–AC SCCs.




(a)




(b)

Fig. 4. Behavior comparison of the two modeling methods and the experimental results: (a) Conversion ratio vs. duty cycle; (b) Equivalent resistance vs. duty cycle.

## III. Application of the Proposed Modeling Method

### *A. AC–AC SCC with a Conversion Ratio of Three*

In this section, a step-up AC–AC SCC with a conversion ratio of three is analyzed using the proposed method to demonstrate the effectiveness of this method. The converter topology is presented in Fig. 5.

The analyzed converter consists of five capacitors and six bidirectional switches and can achieve step-up and step-down configurations with minimal change in the points where the input source and the load are connected. The gate drive signals are the same as those in Section II.A. The converter has two major operation stages as shown in Figs. 6(a) and 6(b).

Stage 1 starts when switches $S_1$, $S_3$, and $S_5$ are turned on. Capacitor $C_1$ is charged by $C_4$, and $C_5$ is charged by the input voltage source through $C_2$. $C_3$ discharges and delivers energy to the load throughout the stage.

Stage 2 starts when $S_2$, $S_4$, and $S_6$ are turned on and $S_1$, $S_3$, and $S_5$ are turned off. Capacitor $C_3$ is charged by $C_5$, and $C_4$ is charged by the input voltage source through $C_2$. $C_1$ discharges and delivers energy to the load throughout the stage.

The voltage across capacitor $C_2$ is always equal to the input source during the two stages.

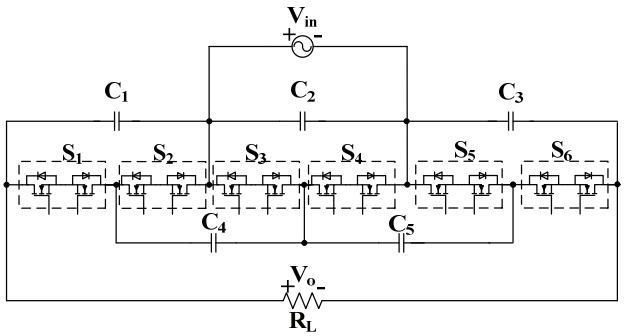



Fig. 5. Topology of an AC–AC SCC with a conversion ratio of three.

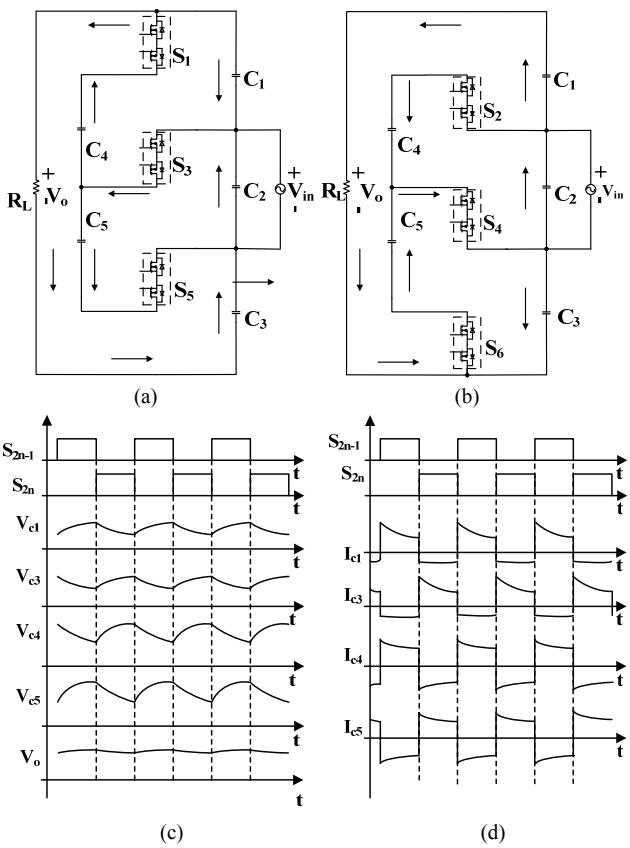
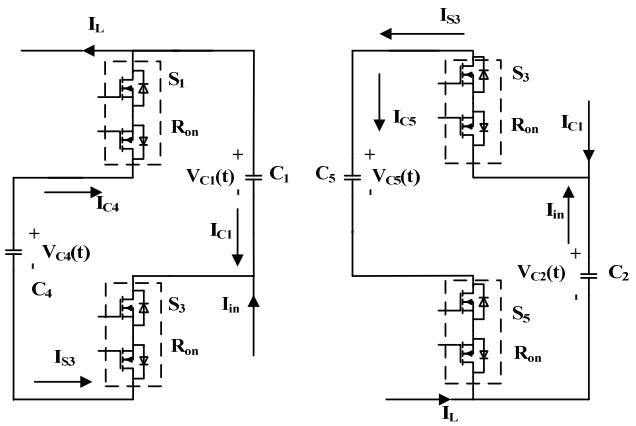



Fig. 6. Operation stages of an SCC and high-frequency waveforms of capacitors: (a) Stage 1; (b) Stage 2; (c) Voltages; (d) Currents.

The expected operation waveforms of voltages and currents are presented in Figs. 6(c) and 6(d), respectively. The converter is assumed to work in PC mode.

The current waveforms of capacitors $C_1$ and $C_3$ are nearly identical to those in Fig. 2(d) given that they all receive energy in one working stage (PC mode) and deliver energy to the load in the other. However, the waveforms in CC mode differ and are further illustrated in Section III.D. The current waveforms of capacitors $C_4$ and $C_5$ vary from those of $C_1$ because they work in PC mode throughout the charge–discharge cycle.




(a) (b)

Fig. 7. Subcircuits of an SCC: (a) Stage 1; (b) Stage 2.

### *B. Modeling of the Converter*

The subcircuits of the converter can be obtained by analyzing the operational stages and expected waveforms of the components, as shown in Figs. 7(a) and 7(b).

To simplify the analysis, all MOSFETs are assumed to have the same on resistance $R_{dson}$ and all capacitors have the same capacitance $C$. The ESR of the capacitor is disregarded.

On the basis of the subcircuits in Fig. 7(a), when t∈ [0, $DT_s$], we yield

$$\begin{aligned} V_{c1}(t) &= R_{on}C_4\frac{dV_{c4}(t)}{dt} + V_{c4}(t) \\ &+ R_{on}(C_4\frac{dV_{c4}(t)}{dt} - C_5\frac{dV_{c5}(t)}{dt}) \end{aligned} . \quad (14)$$

From KCL,

$$\frac{V_o}{R_L} + C_4\frac{dV_{c4}(t)}{dt} + C_1\frac{dV_{c1}(t)}{dt} = 0 . \quad (15)$$

For the charging loop of $C_5$ in Fig. 7(b), the following equation can be derived:

$$V_{in} = R_{on}(2C_5\frac{dV_{c5}(t)}{dt} - C_4\frac{dV_{c4}(t)}{dt}) + V_{c5}(t) . \quad (16)$$

Considering the law of charge–balance and assuming the load current to be constant due to the high frequency, the following equations can be derived:

$$C(V_{c1\max} - V_{c1\min}) = \frac{(1-D)V_oT_s}{R_L} , \quad (17)$$

$$C(V_{c4\max} - V_{c4\min}) = \frac{V_oT_s}{R_L} . \quad (18)$$

Given the symmetrical structure of the converter, the output voltage can be expressed as follows:

$$V_o = V_{c1\max} + V_{c1\min} + V_{in} . \quad (19)$$

From (14)-(19) and considering the boundary conditions, the expression of the conversion ratio is obtained as follows:

$$\begin{aligned} \frac{V_o}{V_{in}} = \frac{6CR_Le^{-\frac{2DT_s}{RC}}(1-e^{\frac{2DT_s}{RC}})(-e^{\frac{2T_s}{RC}}+e^{\frac{2DT_s}{RC}})}{[2Ce^{\frac{T_s}{RC}}(-e^{-\frac{DT_s}{RC}}+e^{\frac{DT_s}{RC}})(-e^{-\frac{T_s-DT_s}{RC}}+e^{\frac{T_s-DT_s}{RC}})(R} \\ +R_L)+T_s(-5+5e^{\frac{2T_s}{RC}}+2e^{\frac{(2-D)T_s}{RC}}-2e^{\frac{DT_s}{RC}} \\ +(-1+2D)e^{\frac{2DT_s}{RC}}+2e^{\frac{(1+D)T_s}{RC}}-2e^{\frac{(1-D)T_s}{RC}})] \end{aligned} . \quad (20)$$

The equivalent resistance can be derived as

$$\begin{aligned} R_{eq} \\ = R_L(\frac{3}{G}-1) = \frac{[2RC(e^{\frac{2T_s}{RC}}-e^{\frac{2DT_s}{RC}})(-1+e^{\frac{2DT_s}{RC}}) \\ +T_s(5e^{\frac{2(1+D)T_s}{RC}}+2e^{\frac{(2+D)T_s}{RC}}+2e^{\frac{(1+3D)T_s}{RC}})]}{2C(e^{\frac{2T_s}{RC}}-e^{\frac{2DT_s}{RC}})(1-e^{\frac{2DT_s}{RC}})} \end{aligned} . \quad (21)$$

The currents that flow through capacitors $C_4$ and $C_5$ are numerically identical due to the similar charge–discharge process. Therefore, when decoupling the subcircuits, the on resistance of $S_3$ can be equalized to $2R_{on}$, which leads to $R$=3$R_{on}$.

From (20), the ideal conversion ratio can be derived as the load approaches infinity,

$$\lim_{R_L\to\infty} G = \frac{6Ce^{-\frac{2DT_s}{RC}}(1-e^{\frac{2DT_s}{RC}})(-e^{\frac{2T_s}{RC}}+e^{\frac{2DT_s}{RC}})}{-2Ce^{-\frac{2DT_s}{RC}}(-1+e^{\frac{2DT_s}{RC}})(-e^{\frac{2T_s}{RC}}+e^{\frac{2DT_s}{RC}})} = 3 . \quad (22)$$

The minimum limit of equivalent resistance can be derived as follows (D=0.5):

$$R_{eq\min} = \lim_{T_s\to 0} R_{eq(D=0.5)} = 8R = 24R_{on} . \quad (23)$$

The obtained $R_{eq\min}$ is represented in the same form as that of the converter in Fig. 2(a).

### *C. Analysis of Control and Component Parameters*

The model derived in Section III.B can be used to provide a solid design principle for the converter in terms of modulation and selection of component parameters. Capacitance, resistance, duty cycle, switching frequency, and load will exert impacts on the conversion ratio. The selection of component parameters is provided in Table II.

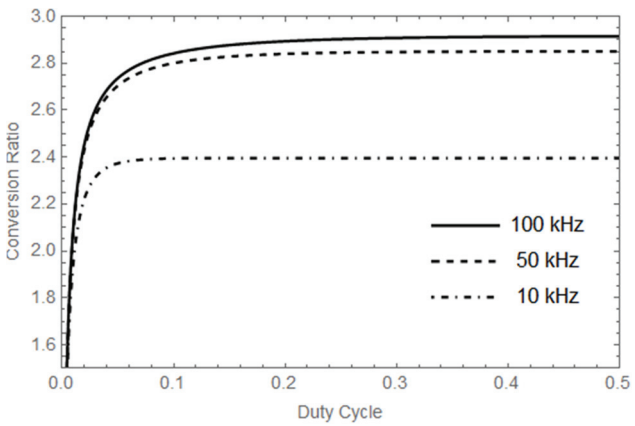
The effects of the converter parameters are illustrated in Fig. 8.

The duty cycle can be used to regulate converter output. As shown in Fig. 8(a), the conversion ratio increases with an increment in duty cycle in the “low duty-cycle” region and reaches a limit at approximately 0.3 for the 50 kHz and 100 kHz curves. The conversion ratio reaches an earlier limit for the 10 kHz curve. The duty cycle is strictly limited within 0.5 to avoid shooting through.

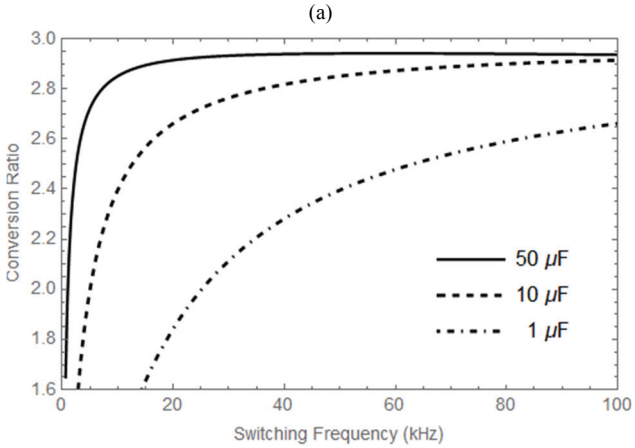
Switching frequency can also be used to regulate the conversion ratio. The modulation capability is noticeable

TABLE II
CONTROL AND COMPONENT PARAMETERS FOR THEORETICAL ANALYSIS

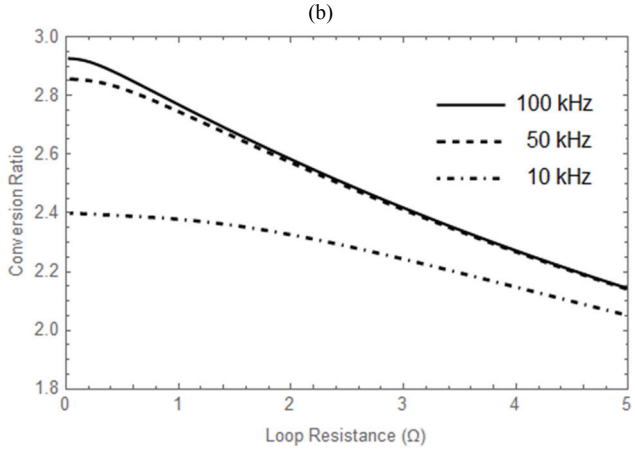
| Fig. 8 | $f$ (Hz) | $f_s$ (kHz) | $R_{on}$ (Ω) | $C$ (μF) | $D$ | $R_L$ (Ω) |
|---|---|---|---|---|---|---|
| (a) | 50 | 10–100 | 0.07 | 1,10,100 | 0.05–0.5 | 100 |
| (b) | 50 | 10,50,100 | 0.07 | 10 | 0.5 | 100 |
| (c) | 50 | 10,50,100 | 0.07 | 10 | 0.5 | 100 |




(a)




(b)




(c)

Fig. 8. Effects of control and converter components: (a) Conversion ratio vs. duty cycle; (b) Conversion ratio vs. switching frequency; (c) Conversion ratio vs. loop resistance.

within the low-frequency region. Although a high switching frequency leads to a high conversion ratio, switching losses and parasitic elements (e.g., ESR and ESL) prevent it from increasing indefinitely. As shown in Fig. 8(b), the conversion ratio remains nearly unchanged when the frequency reaches 60 kHz for the given parameters. The conversion ratio is slightly higher with a switching frequency of 100 kHz than that of 50 kHz, as shown in Figs. 8(a) and 8(c).

Frequency considerably influences capacitance modulation capability when it is relatively small (e.g., when $C$=1 μF). Increasing capacitance is another method for raising the conversion ratio. A high charging efficiency is obtained when $\Delta V$ ($=V_{cmax}-V_{cmin}$) is small, and a large capacitance leads to a small ΔV, and consequently, high efficiency [21].

Loop resistance is the total resistance in the charging and discharging circuits, and it consists of the ESR of capacitors and on resistances. A large loop resistance leads to a small charging current in the path. Loop resistance is supposed to be small for improving efficiency and decreasing conduction losses, as shown in Fig. 8(c).

### D. Component Stress Analysis

Using the proposed method, the peak stress of components, such as extreme voltage and current stresses, can be estimated for the analyzed SCC in Fig. 5. The ESR of the capacitor is disregarded to simplify the derivation. The expressions for $V_{c1}$(t) during the charging period can be derived as follows:

$$V_{c1}(t)=V_{in}\frac{\begin{array}{l}T_s(2+(-2+D)e^{a-\frac{2t}{CR}}+D\,\mathrm{Cosh}[a])\,\mathrm{Sinh}[b]\\+\mathrm{Sinh}[a](-4T_s+2(1-D)T_s\,\mathrm{Cosh}[b]\\+(-2CR+4CR_L-6t+3DT_s)\,\mathrm{Sinh}[b])\end{array}}{\begin{array}{l}2T_s(1-(-3+D)\,\mathrm{Cosh}[a])\,\mathrm{Sinh}[b]\\+2\,\mathrm{Sinh}[a](T_s+(2+D)T_s\,\mathrm{Cosh}[b]\\+2C(R+R_L)\,\mathrm{Sinh}[b])\end{array}}, \quad (24)$$

where $a=\frac{DT_s}{CR}$ and $b=\frac{(1-D)T_s}{CR}$.

The SCC operates in different modes due to the varying component parameters of the converter.

The expected operational high-frequency waveforms of the voltage across $C_1$ in different operation modes can be obtained from the theoretical analysis in Figs. 9(a) and 9(b).

Fig. 9(a) indicates that for the SCC operating in PC mode, $C_1$ charges throughout Stage 1 [0, $DTs$] and discharges throughout Stage 2 [$DT_s$, $T_s$] in a switching period. Therefore, the maximum value is reached at the end of Stage 1, whereas the minimum value is reached at the end of Stage 2.

Fig. 9(b) indicates that for the SCC operating in CC mode, unlike the converter operating in PC mode, the maximum value is reached at $\Delta t$ during interval [0, $DTs$]. The capacitor $C_1$ starts to discharge in Stage 1. The minimum value is reached at the end of Stage 2.

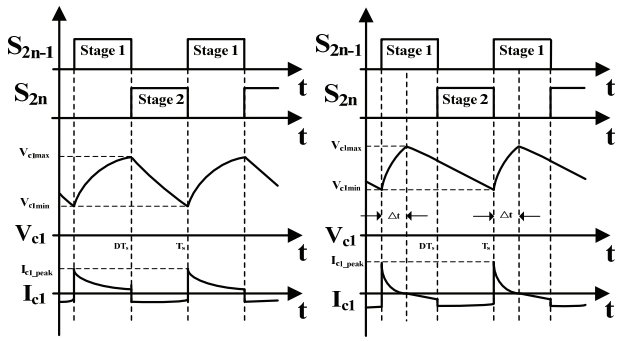



Fig. 9. Expected high-frequency waveforms of capacitor $C_1$: (a) PC mode; (b) CC mode.

Nevertheless, the high-frequency waveforms of capacitors $C_4$ and $C_5$ in CC mode remain the same as those in Figs. 6(c) and 6(d).

For the converter operating in PC mode, the maximum voltage of capacitor $C_1$ can be derived on the basis of the conversion ratio derivation process described in Section III.B as follows:

$$\begin{aligned} V_{c1\max} &= V_{c1(D=0.5)}(DT_s) \\ &= V_{in}\frac{\begin{array}{l} e^{-a}((-4T_s - e^{a}((2+e^{a})T_s \\ +2C(R-2R_L)\mathrm{Sinh}[a])) \end{array}}{\begin{array}{l} 2(5T_s\,\mathrm{Cosh}[a] \\ +2(T_s + C(R+R_L)\mathrm{Sin}[a])) \end{array}}, \end{aligned} \tag{25}$$

where $a = \dfrac{T_s}{2CR}$.

The minimum voltage of capacitor $C_1$ can be derived as

$$\begin{aligned} V_{c1\min} &= V_{c1}(0) \\ &= \frac{\begin{array}{l} V_{in}(T_s(1+(-3+2D)\mathrm{Cosh}[a])\mathrm{Sinh}[b] \\ +\mathrm{Sinh}[a](-2T_s - C(R-2R_L)\mathrm{Sinh}[b] \\ +(-1+D)T_s(\mathrm{Cosh}[b]+3\mathrm{Sinh}[b]))) \end{array}}{\begin{array}{l} T_s(1-(-3+D)\mathrm{Cosh}[a])\mathrm{Sinh}[b] \\ +\mathrm{Sinh}[a](T_s + (2+D)T_s\,\mathrm{Cosh}[b] \\ +2C(R+R_L)\mathrm{Sinh}[b]) \end{array}}. \end{aligned} \tag{26}$$

The input voltage source delivers energy to $C_4$ through Stage 1, and the peak current occurs at the start of the charging process.

The minimum voltage of $C_4$ can be derived as

$$V_{c4\min} = V_{in}\frac{\begin{array}{l} T_s(1-(-3+D)\mathrm{Cosh}[a])\mathrm{Sinh}[b] \\ +\mathrm{Sinh}[a](-2T_s + (-1+D)T_s\,\mathrm{Cosh}[b] \\ +(2C(R+R_L)-3T_s)\mathrm{Sinh}[b]) \end{array}}{\begin{array}{l} T_s(1-(-3+D)\mathrm{Cosh}[a]\mathrm{Sinh}[b] \\ +\mathrm{Sinh}[a](T_s + (2+D)T_s\,\mathrm{Cosh}[b] \\ +2C(R+R_L)\mathrm{Sinh}[b]) \end{array}}. \tag{27}$$

Therefore, $I_{c4\max}$ can be derived as follows:

$$\begin{aligned} I_{c4\max} &= \frac{V_{in} - V_{c4\min}}{2R_{on}} \\ &= \frac{9V_{in}}{2R}\cdot\frac{(1+e^{b})T_s\,\mathrm{Sinh}[a]}{\begin{array}{l} T_s(1-(-3+D)\mathrm{Cosh}[a]\mathrm{Sinh}[b] + \mathrm{Sinh}[a](T_s \\ +(2+D)T_s\,\mathrm{Cosh}[b] + 2C(R+R_L)\mathrm{Sinh}[b]) \end{array}}, \end{aligned} \tag{28}$$

where $a = \dfrac{DT_s}{CR}$ and $b = \dfrac{(1-D)T_s}{CR}$.

The derived peak currents and voltages can be useful when designing converter topology and selecting control and component parameters. The component stress of other switches and capacitors can be derived by following a similar procedure illustrated in this section.

TABLE III
CONTROL AND COMPONENT PARAMETERS FOR EXPERIMENT VERIFICATION

| Description | Value |
|---|---|
| Output power ($P_o$) | 1 kW |
| Input voltage ($V_{in}$) | 110 V (50 Hz) |
| Switching frequency ($f_s$) | 50 kHz |
| Duty cycle ($D$) | 0.5 |
| Capacitance ($C$) | 20 μF |
| Load ($R_L$) | 50 Ω |
| MOSFETs | FQA62N25C ($R_{dson}$=0.035 Ω) IRFP460 ($R_{dson}$=0.27 Ω) |

## IV. EXPERIMENTAL VERIFICATION

A series of experiments is performed with two prototypes in a laboratory to demonstrate the correctness of the proposed modeling method. Prototype 1 is an SCC with a conversion ratio of two, whereas Prototype 2 has a conversion ratio of three. The major specifications and component parameters used in the prototypes are presented in Table III.

### *A. Experimental Results of Prototype 1*

The input and output voltages are presented in Fig. 10(a). The measured output voltage is 216.88 Vrms. The experimental conversion ratio is 1.972, which is close to the ideal value of 2 $V_{in}$. The slight voltage drop results from the switching and conduction losses caused by the resistance and other parasitic elements.

The current through capacitor $C_1$ is presented in Fig. 10(b), and the waveform agrees with the theoretical analysis in Fig. 2(d). Several current spikes occur due to the distortion of the grid voltage.

The voltage across MOSFET $S_1$ is given in Fig. 10(c). As expected, the voltage stress of the switch is equal to the input voltage and half of the output voltage.

The theoretical curves of the conversion ratio and the switching modulation using the proposed modeling method

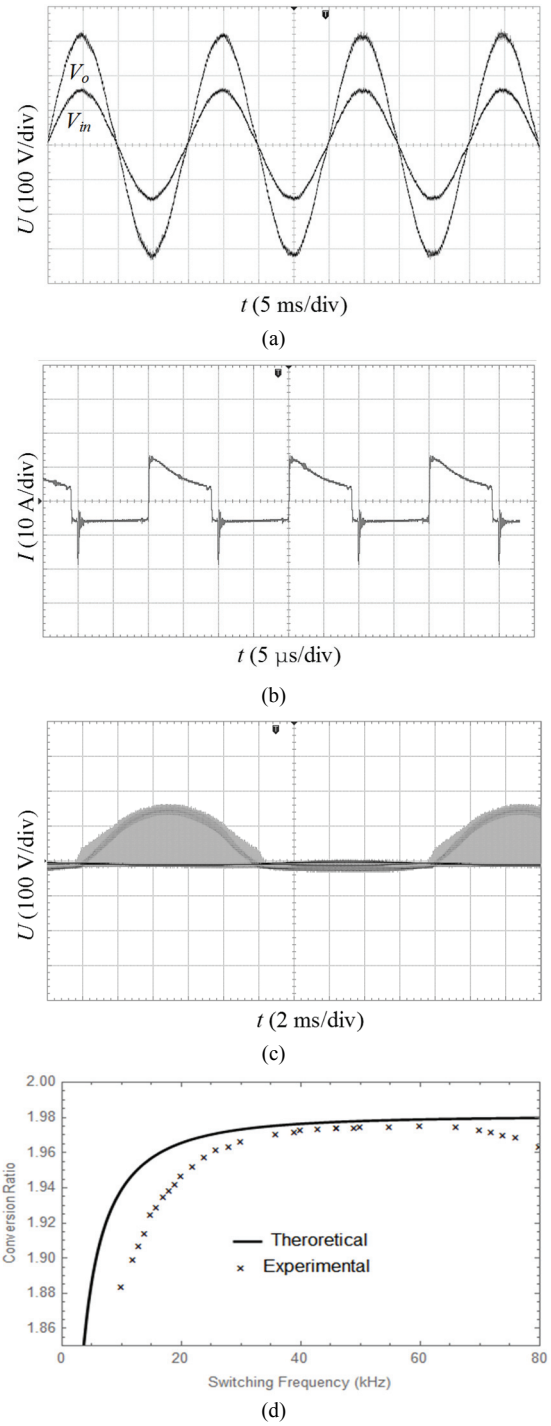



Fig. 10. Experimental results of Prototype 1: (a) Waveforms of input and output voltages; (b) Waveform of current through capacitor $C_1$; (c) Waveform of voltage across switch $S_1$; (d) Conversion ratio vs. switching frequency.

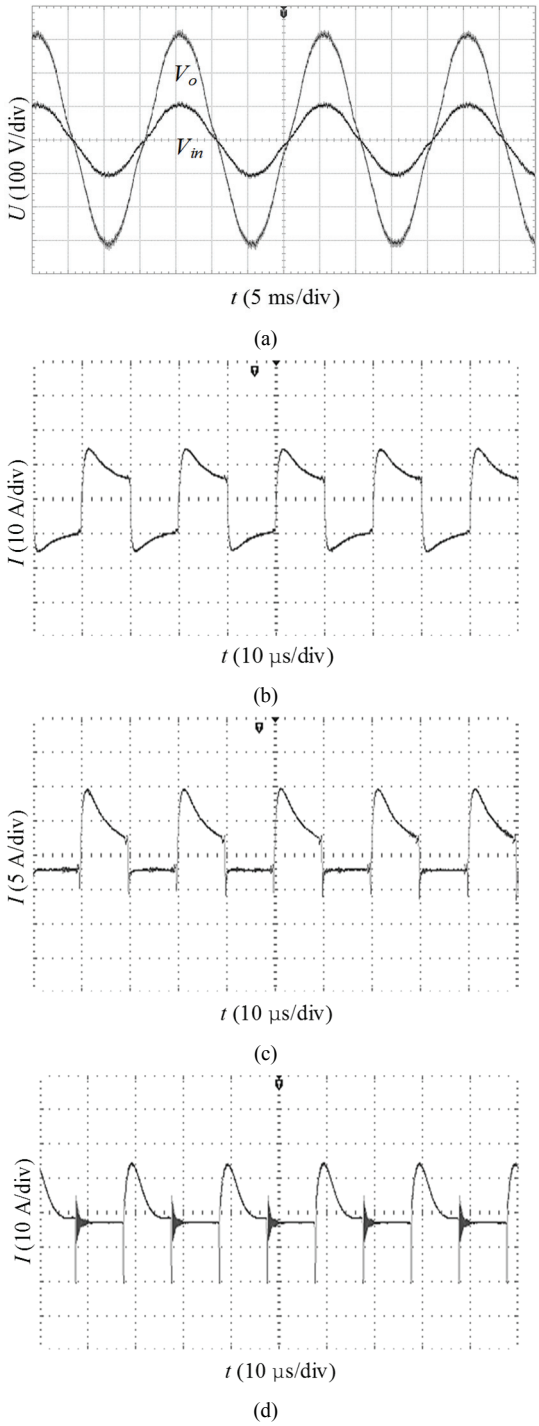
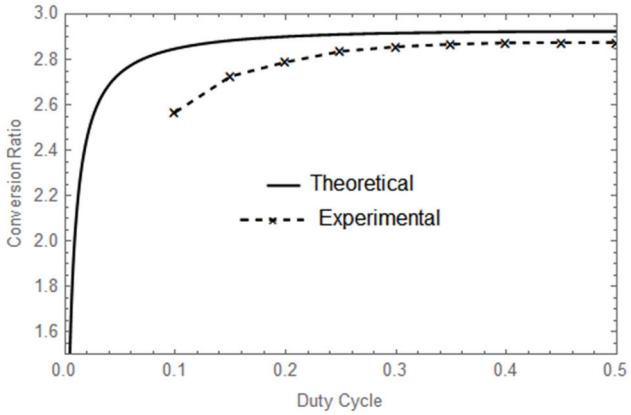



Fig. 11. Experimental results of Prototype 2: (a) Waveforms of input and output voltages; (b) Waveform of current through capacitor $C_4$; (c) Waveform of current through $C_1$ (PC mode); (d) Waveform of current through $C_1$ (CC mode).

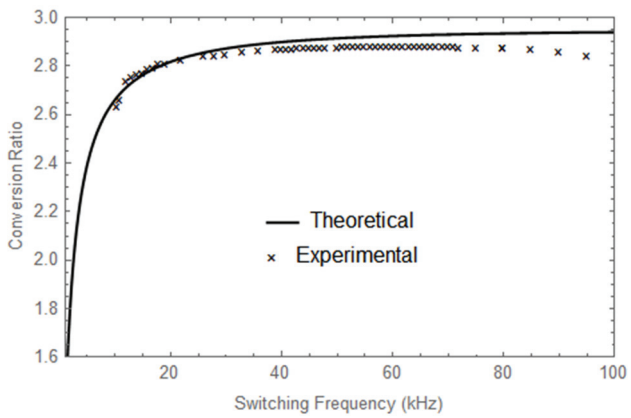
are compared with the experimental results. The duty cycle regulation curves are presented in Fig. 4(a). The frequency regulation curves are provided in Fig. 10(d). The experimental and theoretical curves exhibit good agreement when switching frequency is between 30 kHz and 60 kHz. The peak ratio for the experimental curve is reached when $f_s$=60 kHz.

### *B. Experimental Results of Prototype 2*

The input and output voltages are shown in Fig. 11(a). The input voltage is 75 $V_{rms}$, and the selection of control and other component parameters is presented in Table III. The measured output voltage is 215.65 Vrms, and the conversion ratio is 2.875.




(a)




(b)

Fig. 12. Duty cycle and frequency regulation curves: (a) Conversion ratio vs. duty cycle; (b) Conversion ratio vs. switching frequency.

The current through capacitor $C_4$ is presented in Fig. 11(b), and the waveform agrees with that in Fig. 6(d). The currents through $C_1$ in PC and CC modes are shown in Figs. 11(c) and 11(d), respectively. The experimental current waveforms agree with those of the theoretical analysis in Figs. 9(a) and 9(b).

The duty cycle regulation curves are shown in Fig. 12(a). The experimental curve matches with the theoretical curve when the duty cycle is above 0.2. The difference in the two curves is mostly attributed to the finite dead time leading to the deviation of the actual duty cycle from the setting values.

The frequency regulation curves are shown in Fig. 12(b). The curves are in good agreement when switching frequency is lower than 70 kHz. The deviations result from the effect of parasitic elements (e.g., ESL and ESR) and the increasing switching losses.

## V. Conclusion

A new modeling method for AC–AC SCCs is introduced in this study. The method provides input–output characteristics, including low-frequency and high-frequency behavior and the impacts of component parameters. The feasibility of this method is validated by comparing it with an existing modeling method for a typical SCC with a conversion ratio of two and through experimental verification.

Using the proposed method, another AC–AC SCC with a conversion ratio of three is analyzed extensively. The operational characteristics of the converter are described and analyzed. The impacts of control and component parameters on the converter are also presented. Component stress analysis for the converter operating in PC and CC modes is performed comprehensively. The effectiveness of the theoretical analysis is confirmed by the experimental results.

We will work on the development of a generalized modeling method for AC–AC SCCs with multiple ratios in the future.

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