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Channel Equalization for High-speed applications using MATLAB

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Abstract

This paper compared the performance with an overview of channel equalization techniques used in high-speed serial transceivers, including the homogeneous architecture and associated components for the GHz interconnect of backplane and cable channels. It also used the MATLAB tool to present system analysis and simulation results for continuous time equivalent structures.

In the case of conventional continuous equalization, high frequency deficits occur due to the use of a comparator that is difficult to implement as well as the low speed limit. In this paper, the channel equalization technique based on the power spectrum analysis of clocks was used to compensate for the frequency loss, and the application of the TX+Channel and TX+Equalizer filters enabled the measurement of attenuation and equivalence without comparators. The application of blender and band-pass filters at high speeds also showed significant effectiveness.

▸Keyword: Channel equalization techniques, Workload, GHZ interconnect, MATLAB simulation

I. Introduction

Look at the homogeneous architecture and associated components for this backplane and cable channel's GHz interconnect, and compare the overview and performance of channel equalization techniques used in high-speed serial transceivers.

In particular, in measuring the attenuation amount and equivalence without a receiver, the channel bandwidth limit can be compensated based on the power spectrum analysis of the clock, and a band-pass filter can be used for high-speed operation accuracy. However, clock adaptation not only reduces comparison of power for each receiver, that it also excels at fast operation, but it is complex and expensive to implement. Therefore, it is effective to apply the band-pass filter with the application of the mixer. Experimentation with all of these implementations and operations uses MATLAB tools to display system analysis and simulation results of a continuous time equivalent architecture.

II. Equalization Overview

1. Channel-Backplane

The transmission signal of a typical high-speed data communication backplane applied with channel equalization is transmitted from an IC to another IC and therefore has the characteristics to pass through many discontinuities depending on the channel. This includes chip bonding, packages, cards, connectors, and various copper trace lengths, which operate through various processes such as reflection and attenuation, which affect the information symbols transmitted throughout the channel. This results in a distortion of the information bits called the Inter-Symbol Interference (ISI). In addition, the impulse response of a typical 30" FR-4 backplane has characteristics that are distorted by a pass with a low transmission bit. These long impulses responses will have a detrimental effect that transmitted information-bit has to the next bit by channel, and the higher the data rate, the greater the number errors.[1]

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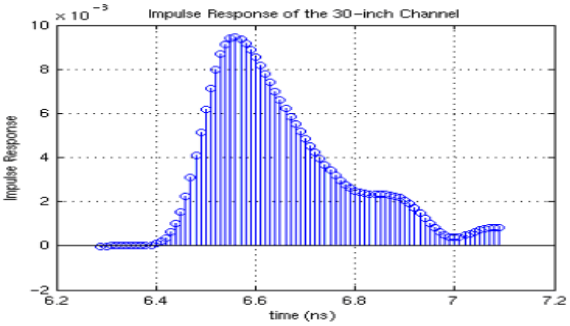


Fig. 1. Normalized impulse response of a 30 inch FR-4 backplane channel[1]

1.1 Cross-talk

Another major obstacle found in the backplane environment is Cross-talk. In this case, there are traces of copper along the backplane from connectors and packages, which cause a lot of capacitance, such as proximity and length in which the bits of information are coupled to adjacent traces. This type can be categorized as Far End Cross-talk (FEXT) and Cross-work (NEXT). FEXT occurs because the transmission symbol is coupled from one channel to a parallel channel connected to a separate receiver and is at the end of the same position as the receiver. This occurs along the length of the channel and can be seen as noise to the following receivers: NEXT occurs when the receiver is coupled on a channel connected to the end of the same position as the opening transmitter. Because the transmitter and receiver are close, the amplitude of the unwanted symbol may be greater than the desired symbol. The information received can then be completely removed. The effects and locations of the topology are shown in Figure 2.[1]

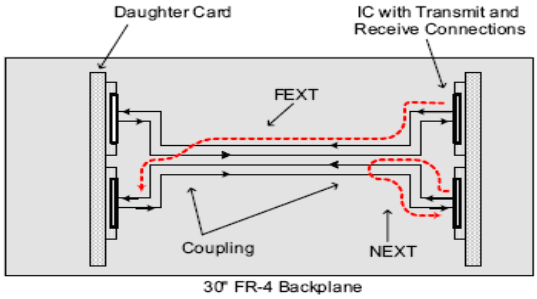


Fig. 2. Channel-Backplane

2. Comparison of Signaling Schemes

Some of the signaling schemes applicable for backplane communications include Non-return-to-Zero(NRZ), Duo-Binary(DB) and Partial Response(PR4) schemes. A detailed comparison of performance of these signaling schemes was recently presented in [2]. Based on this study, NRZ is the best solution for the backplane application at the speed up to 12Gbps. It has advantages such as the backward compatibility, better performance, less complexity and lower power consumption. But any system which has 10dB of loss difference between the 2-PAM and 4-PAM Nyquist fundamental frequencies would be likely to benefit from 4-PAM signaling. Figure 3 shows the Signal to noise ratio for different signaling schemes.

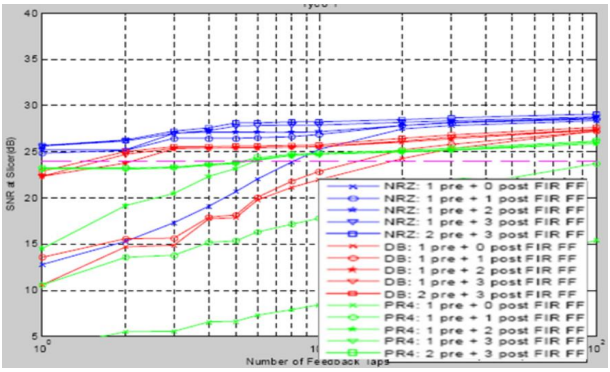


Fig. 3. Performance comparison of NRZ, DB, and PR4 signaling over Tyco channel #1 with data rate of 10.3Gb/s with the worst case NEXT[2]

Table 1. System Environment

Item	Value
CPU Clock Speed	100 ~ 500 MIPS

3. Comparison of Equalization Schemes

3.1 Equalization

In the meantime, several equalization techniques have been proposed to compensate for the low-pass characteristics of the transmission channels. Equivalence technologies, applied in appropriate circuit configurations and architectures with increased speed and interference, apply when there is no interference through linear and nonlinear algorithms, but amplifies high-frequency noise, and when noise rejection and high-frequency signal energy can be increased. An important element of this equalization technology is how the coefficients are set up and that is adaption level.

3.2 TX Equalization / RX - Equalization

To enable system-independent calibration of the transmission pre-emphasis, there is a signal-signal LMS adaptive algorithm that allows a common mode back channel to be included in the link to enable update communication in the reverse direction of the fast data flow.[3] Two-way links are required to implement a

minimum mean square(LMS) adaptation algorithm that is not acceptable in one-way applications, and Figure 4 shows a typical TX pre-emphasis plan.[4][5]

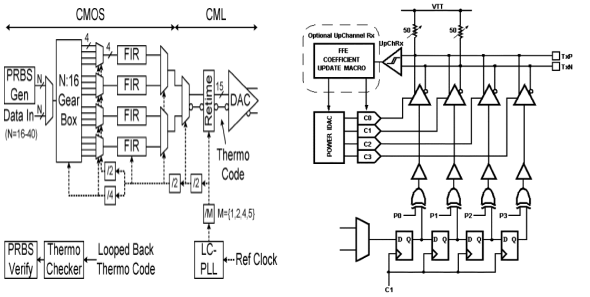


Fig. 4. Typical TX pre-emphasis schemes

There are two serious limitations to this technique: maximum allowable amplitude, high frequency content and increased power. In the first case, this equivalence technique would still not be appropriate without the necessary high power levels. This means that pre-emphasis on transmitters can partially compensate for channel loss, but offset the dynamic range cost. This means that the pre-emphasis on the transmitter may partially compensate for the loss of the channel, but also offsets the dynamic range cost. A supply voltage of 2.5V is required to accept large amplification elements or pre-emphasize 12dB without being affected by low frequency fluctuations.[6] Therefore, if low supply voltage and channel loss up to 25dB indicate that the receiver should perform the most uniformity. The second, even more important limits are the result of high-frequency content and increased power. These factors reduce the performance of the system by strengthening the NEXT connection of the transmitted symbol to the adjacent channel.

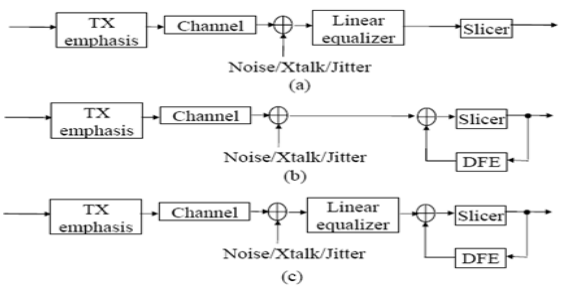


Fig. 5. Different Equalization Schemes: (a) LE; (b) DFE; (c) LE+DFE.[2]

The best way to set up the complex equalizer required to run at 5+ Gb/s with very low bit error rates is the <Browse Table Set and Forgetting> and <Adaptive Once> techniques. The <Browse Table Set amp; Forget> method measures the channel on the test bench and sets the best set of equalization coefficients. Initializing the live system loads the coefficients from the lookup table regardless of the variation of this particular system due to manufacturing or environmental conditions. Therefore, a dedicated pin is not required to set up the equivalence tab, so it is the simplest method, but some serious limitations may arise. First, it does not take into account the extensive laboratory characteristics for each channel and, second, manufacturing changes (including impedance tolerances) seen in the board combinations of individual systems.[7]

The adaptive once technique is used to measure channel margins and optimize equalizer settings. This method has the advantage of minimizing the impact of manufacturing deviations, but does not take into account environmental deviations when the system is operating. The most practical of these changes is temperature and humidity, and one of the other ways to consider Continuous Adaptation. This technique has hardware to perform continuous updates on the equivalence tab while real-time data is running, and provides optimal equivalence settings for all manufacturing systems and operating environments. However, there is a need for the complexity of hardware to monitor and update tabs without disrupting real-time data streams.[8]

4.1 Adaptation Criterion

Most widely used adaptation criterion is the mean-square error (MSE) calculated between the recovered signal and the training data in the time domain at sampling points. The typical equalizer structures using this criterion are feedforward transversal equalizers (FFE) and decision-feedback equalizer (DFE) using the least-mean square (LMS) algorithm or its variations.

The second method obtains error signal by sampling the equalizer output and then analyzing its characteristics in the time domain [9], [10]. This methods need a clock with accurate sampling phase to obtain time-domain information required for error calculation.[11]

Another way to generate an error signal is to use statistical frequency information. Looking at the benefits, (a) because the information is a time average result, the speed requirements for tuning circuits are mitigated. (b) by using continuous time analogue circuits to compare

frequency domain signals other than time zones, the sampling clock of correct phase is not necessary, (c) the desired frequency is statistical information and does not need to have an training sequence.[12]

III. A basic study

1. Z-domain Equalization comparisons

The design of a high-speed cross-sectional equalizer, shown in Figure 6 of the CMOS 1Gb/s 5 tab, based on Inductor-Less Third Order Delay Cells[13], requires the implementation of a broadband delay line. Based on the third linear phase filter presented in this study, the delay line has two different phases for the broadband SUM node that can place a parasitic pole on the output of a cross-section equalizer exceeding 650MHz. The results showed that programmable frequency responses could compensate for losses of up to 25dB at 500MHz for 1Gb/s binary data streams.

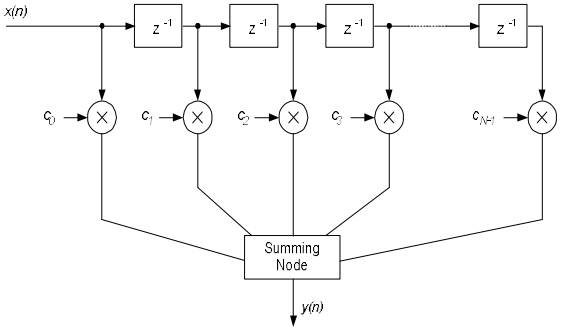


Fig. 6. 5-tap transversal equalizer structures

The proposed 3rd-order delay cell to implement each z^-1 block is depicted in Figure 7. Derived from the L_C ladder prototype shown in the same figure, the OTA-C realization incorporates active inductor emulation(L_2 = $C_2/(g_{m1}g_{m3})$) as well as active terminations(RS,L = $1/g_{m2}$) at ports A and B that are implemented by using NMOS loads(transistors M_2 in Figure 7) at the output of 2 of the amplifiers in the inductive emulation. The operating point at the input and output ports is fixed by the delay cell terminations (M_2); we can knows that hence only one common-mode feedback (CMFB) circuit is required for the entire structure.

Similarly, g_{m0} is a single-stage OTA that does not require a large gain since it is connected to a low-impedance at port A. These features lead to a compact low-power realization of the 3rd order delay cell. Current Ibias1 controls the gain while Ibias2 sets the group delay, that providing a tuning range from 420ps to 590ps with <10% ripple within 500MHz. Simulations over process corners and temperatures of -20°C to 100°C show variations in the low frequency group delay within 15%. Designed in a standard 0.35μm CMOS process, the delay cell consumes 16.8mW(Supply = ±1.5V) when tuned for a nominal delay of 500ps at 27°C room temperature.

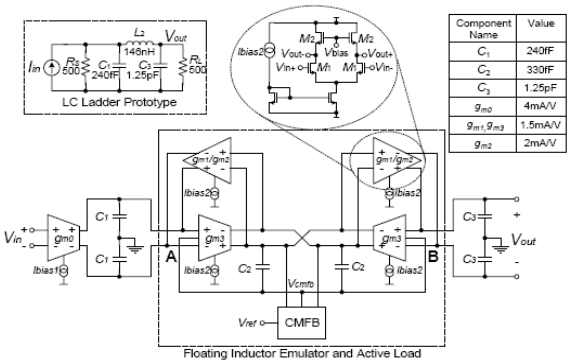


Fig. 7. 3rdorder delay Cell

To further improve the bandwidth of the summing circuit and I/V converter, a transimpedance load is proposed, as shown in Figure 8. The load, composed of a TIA implemented by M_3 and R_1, leads to a transimpedance gain of TGain = $-R_1$, assuming $R_2>>R_1>>1/g_{m3}$(g_{m3} denoting the transconductance of M_3). Resistors R_2 bias the gates of M_4, and M_5(which provides the bias current for the Gilbert cells) to avoid the use of additional CMFB circuits, therefore reducing power consumption. The circuit effectively introduces a low resistance at both, the summing and the output nodes, leading to 2 high-frequency poles approximately given by ω1 = $g_{m3}/(Cp + Cgs,3)$ and ω2 = g_{m3}/C_L, where Cp is the total parasitic capacitance of the 5 multipliers, Cgs,3 is the parasitic capacitance added by M_3, and C_L is the load capacitance due to the next stage, typically a limiting amplifier. This circuit provides a wider bandwidth compared to the resistive and cascode approaches even with the additional capacitance Cgs,3(~200fF). Using this technique, the 3dB bandwidth of the summing circuit is increased to 1GHz(R_L = 1kΩ, g_{m3} = 7mA/V), while the cascade approach leads to a bandwidth of only 520MHz, which would result in larger deterministic jitter. The total power consumption of the 5 multipliers(Gilbert cells) is 22.5mW; the TIA will doing consumes an additional 6mW.

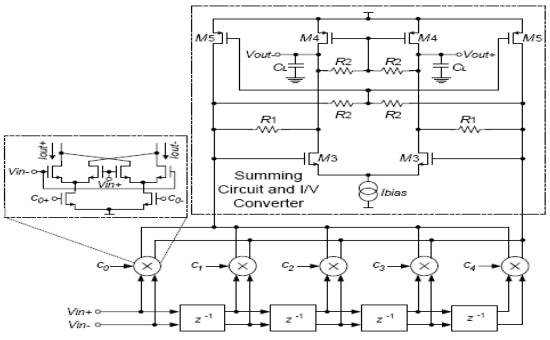


Fig. 8. Summing Circuit and I/V Converter

2. Classifications of Receiver Equalizers and comparisons

The equalizer is used to compensate for the frequency-dependent loss in CAT5e twisted-pair cable. In Figure 9, that shows classifications of Receiver Equalizer and in this section focus on comparison between S-domain active continuous time equalization and Z-domain equalization.

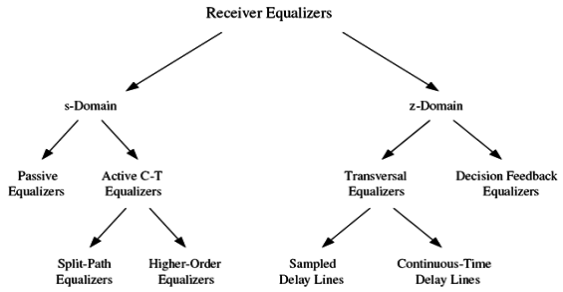


Fig. 9. Classifications of Receiver Equalizers

A recent study of equalizer is as follows: [4], [5], [6] Incorporates nonlinear equivalents, such as decision feedback, to accommodate sharp sounds in the channel due to impedance interruption and to prevent amplification. The transceiver core that uses adaptive reception equalization with tab 1 DFE and linear equalizer emits 150mW at 6.25Gb/s.

Recent equalizer characteristics are preferred when cross talk and impedance discontinuities, that due to connectors and biases become important.

An analog adaptive equalizer can compensate for loss in up to 30 inches of FR4 transmission line, dissipates only 25mW.[14] Discrete-time analog finite-impulse-response equalizers can achieve low-power operation and take advantage of various digital adaptive algorithm but receiver front-end, a cross-dependence exists between the equalizer adaptation loop and the timing recovery loop. The adaptation loop only works well if a recovered clock is available. Meanwhile, as the data rate increases, the power consumption grows drastically owing to the large number of taps needed in this type of equalizer.

Low-power, high-speed applications performed well in continuous time analog equalizer studies. A typical approach compares to low frequencies by adjusting the frequency response of an active high-pass filter, and that achieves uniformity by increasing the high-frequency component of the data signal.[15]

IV. Matlab Simulation

The MATLAB tool was used to establish a homogeneous architecture and operational experiment for the GHz interconnects of backplane and cable channels, and to present system analysis and simulation results for sequential time equivalent structures for the channel being used by high-speed serial transceiver. The experimental method is to compare each of the low-pass filters that may have ideal gain values, high-frequency bandwidth-pass filters, and mixer+filters according to clock-driven channel equalization-based behavior, and to demonstrate that the technology proposed in this paper is effective through simulation based on implementation.

1. The Continuous Time Equalization Matlab Simulation

The received input signal first goes through an equalizing filter, which has to signal paths: the unity-gain path and the high-frequency-boosting path. The high frequency-boosting path compensates for the high-frequency loss of the channel so that the overall loss becomes equal for all frequencies. The output of the equalizing filter is then fed into a comparator with a regulated output swing (regulating comparator), which then transforms it into a signal with predefined edge rate and amplitude. The rest of the circuits comprise the servo loop that adaptively adjusts the high-frequency gain of the equalizing filter. The servo loop determines the need for more boosting by comparing the high-frequency contents of the comparator's input and output signals. Two pairs of high-pass filter and rectifier extract the high-frequency power of these signals, and an error amplifier calculates their difference. After being filtered by a loop capacitor C, this difference controls the high-frequency gain, which effectively adjusts

the zero frequency of the equalizing filter. Unfortunately, this conventional adaptive equalizer suffers from two main bottlenecks. One is the low operating frequency of the equalizing filter and the other is the degradation of adaptation accuracy.

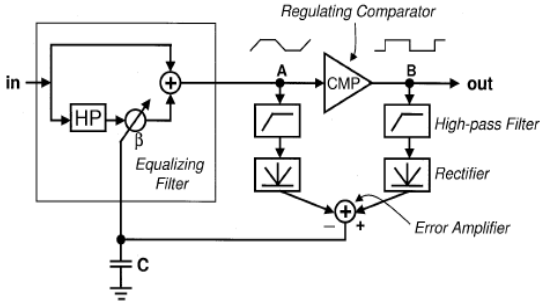


Fig. 10. Block Diagram of conventional Continuous-time adaptive Cable equalizer[15]

Figure 10 shows the block diagram of the conventional CMOS continuous-time adaptive cable equalizer, and that shows the existing the sequence of operations is as follows.

- The received input signals are first passed through the equivalence filter, which signals the integration-gain path and the high frequency boost path. The high frequency boost path compensates for the channel's high frequency loss so that the total loss is equal at all frequencies.
- The output of the equivalence filter is supplied to the regulated output regulation comparator, which converts it into a signal with predefined edge speeds and amplitudes. Servo loops, which adaptively adjust the high frequency gain of equivalence filters, compare the high frequency components of the input and output signals of the comparator to determine the need for more climb.
- This means that two pairs of high-pass filters and rectifiers extract the high-frequency power of these signals and the error amplifier calculates the difference.
- After filtered by the roof capacitor C, this difference effectively adjusts the zero frequency of the equalizing filter by controlling the high frequency gain. However, the conventional adaptive equalizer has two major bottlenecks: the low frequency of equalization filters and the poor adaptation accuracy.

1.1 Equalizer Filter

Copper marks, which are designed as transmission lines on the FR4 substrate, experience both skin effects and genetic loss (for an Ex. 30 inch trace, represent losses of 5GHz: about 21dB, 10GHz: 34dB). Therefore, equalizer filters should provide adequate benefits around 5GHz to equalize the signal spectrum, with the following requirements for gain pitch circuit design:

- Enough boost at high frequencies.
- Matching the reverse loss profile of the channel with the appropriate tolerances.
- Minimum low frequency loss low jitter acquisition is important, with sufficient noise accumulation minimised and linearity at the cascaded stage.
- Small input capacitance.

These requirements also created common problems in designing low-voltage broadband amplifiers, such as bandwidth constraints or functions running.

2. Simulation Results and Consideration

Based on several techniques, the results of the MATLAB simulation using the continuous time equalization technique are as follows:

In simulation, the channel was 1storder low-pass filter with the cutoff frequency equal to Pc, and the total transfer function including the channel and the equalization filter is obtained as

$$H_T(S) = H_C(S) * H_E(S) = \frac{P_C}{S+P_C} * \frac{S(A+1)+P_H}{S+P_H}$$

Hc(s) is the channel transfer function, He(s) is the transfer function of the equalization filter, Pc is the channel pole, A is the variable gain amplifier (VGA) gain, and Ph is the pole of a HPF in the equalization. The optimal VGA gain, A that makes the zero of the equalization filter equal to the channel pole is obtained as

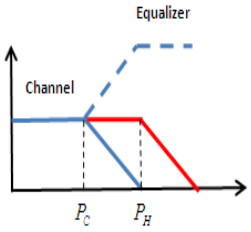
$$A = -1 + \frac{P_H}{P_C}$$

Ex:

$NRZ\,rate = 1Gbps$
$Require\,BW = 500MHZ\ \text{for}\ channel$

$P_c = 50MHZ,\ Theerefore$
$P_c = 50MHZ\ \text{and}\ Equalizer\,P_h = 500MHZ$

$ideal\,A = 9$



2.1 Demonstrate Poor adaptation

In Figure 11, the comparator output is not band-limited, however input of comparator is band-limited by channel+equalizer filter. Therefore, the comparator output power will be always higher than input, so equalizer filter will be over-boosting.

$$A = -1 + \frac{P_H}{P_C}$$

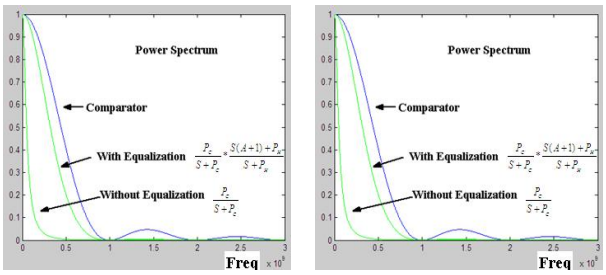


Fig. 11. Power vs Frequency

2.2 Design Consideration: Power detecting Filter

As shows like follow Table 1, the VGA gain value A seriously depends on type of power detecting filter and their cut off frequency when is more than ideal A = 9.

Table 2. Value A that depends on type of power detecting filter and their frequency

Power detecting Filter	Fc=100MHz	Fc=400MHz
Low pass	A=9.6	A=10
High Pass	A=12	A=13.5
Band Pass	Fc=500MHz 450MHz~550MHz A=12.8	Fc=500MHz 400MHz~600MHz A=12.4

As we can see in Table 1, the low-pass filter allows having ideal gain value, however, in practice, the DC offset significantly distorts the power comparison. Therefore, high-pass or band-pass filters are utilized in most systems.

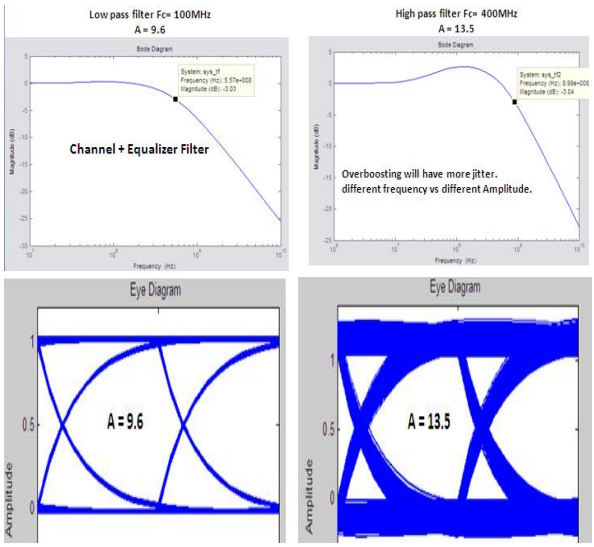


Fig. 12. input 1Gbps (a) magnitude response vs Frequency (b) eye diagram of after equalization

In Figure 12 shows poor adaptation will have over VGA gain and it generates jitter.

V. Results

1. Power Detecting filter - Mixer+filter

The DC offset of the low-pass filter, which allows you to have the ideal gain value, is significantly skewed power comparison, that in high speed operation, band-pass filters are preferred to use due to adaptation accuracy. However, high center frequency band-pass filters are complex and expensive to implement. Hence a mixer can be used to down convert the relevant information to a lower center frequency and utilize a power detecting filter around this frequency.

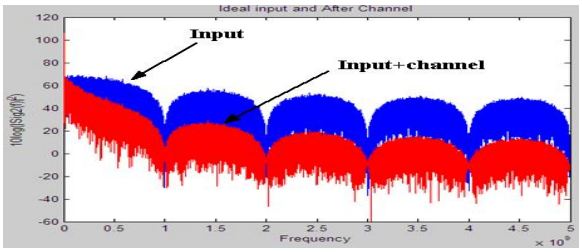


Fig. 13. Power spectrum vs Frequency

As mentioned above(Figure Ex), the input is NRZ 1Gbps and channel is 1st order LPF with Fc=50MHz. Figure 13 shows the power spectrum of Input and Input + channel. As we can see, the power spectrum after the

channel which was significantly attenuated necessitating applying channel equalization. To compare power of input of comparator and output of comparator, firstly, that applied the mixer. Of course it requires the reference signal. Therefore the center frequency was reduced 50MHz instead of 500MHz. After that using filter, we achieve VGA gain value such as 10. Figure 14 shows converge A = 10 and that figure 15 shows transient simulation about TX+Channel(up part) and TX+Channel+Equalizer filter(down part).

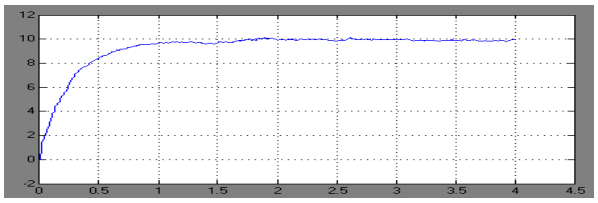


Fig. 14. VGA gain A vs Time (us)

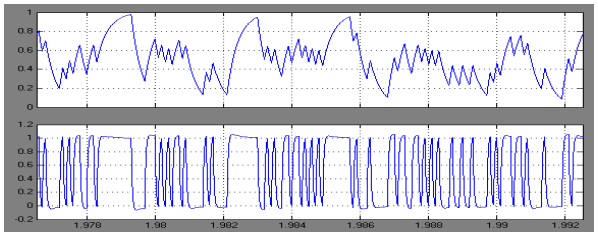


Fig. 15. Transient simulation (a) up part TX+Channel (b) down TX+Channel+Equalizer filter

2. Clock Adaptation & power detecting - Mixer+ filter

The accuracy of the clock adaptation and power detection resulting from high-speed transmission results in complex implementation and cost increases with the use of band pass filters. Thus, the application of blender+filter to clock-run channel equalization-based actions enables each receiver to operate without any power comparison and reduces power consumption and area. Figure 16 shows block diagram of continuous-time adaptive cable equalizer with clock.

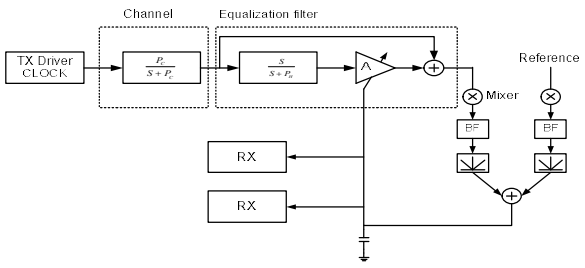


Fig. 16. Block Diagram of Continuous-time adaptive Cable equalizer with Clock

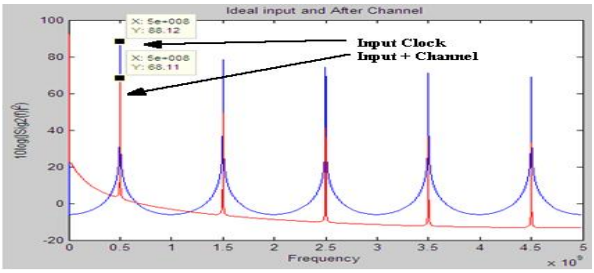


Fig. 17. Power spectrum vs Frequency input and input+channel

Figure 17 shows the power spectrum for 1Gbps Clock Signal and after channel. As we can see, at 500MHz, the signal attenuated due to limit bandwidth of channel which is 1st order LPF fc=50MHz. Based on power spectrum analysis of clock, we want to compensate losses at 500MHz, and that will be a sinusoidal signal if you apply the band-pass filter which has center frequency of 500MHz. Therefore, using TX PLL reference signal measures the attenuation amount without comparator, and equalization. In simulation, we set input signal 1Gbps, however, in high speed such as 20Gbps, it requires Fc=10 GHz band-pass filter. Therefore, we apply the mixer and lower down Fc and apply band-pass filter.

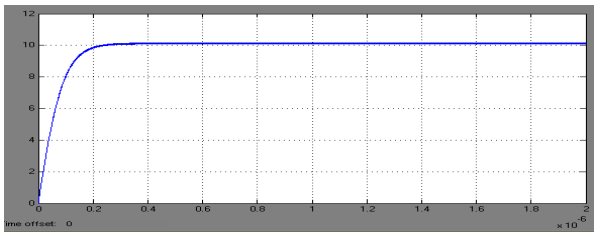


Fig. 18. VGA gain A vs Time (us)

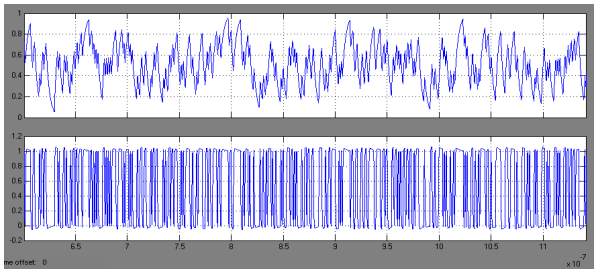


Fig. 19. Transient simulation (a) up part TX+ Channel (b) down TX+Channel+Equalizer filter

In this simulation, VGA gain values were satisfied with A=10(Figure 18), and that in Figure 19 shows the results of an transient simulation with the TX+Channel(up part) and TX+Channel+Equalizer filter(down part).

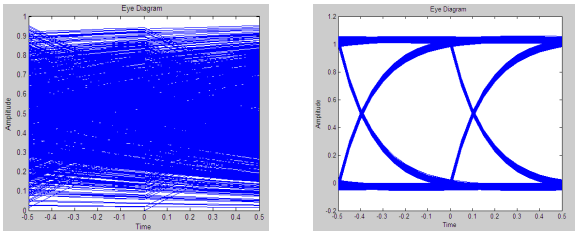


Fig. 20. input 1Gbps (a) Eye diagram of Before equalization (b) eye diagram of after equalization

In Figure 20 shows, we can clean eye diagram as utilizing this continuous time equalization. Applying clock adaptation we can reduce each receiver power comparison portion and can be operate high speed operation, however it requires extra pin using for adaptation.

VI. Conclusion

By limiting the speed limit and adaptability of conventional continuous equalization, the frequency of comparator power comparison applications is reduced, and that the operating speed can also be limited because the comparator itself does not affect the slice. As a result, each receiver can operate without power comparison by using clock-running channel levels, and updating and transmitting them to other receivers. These results are a major factor in reducing electricity consumption and areas. These channel-leveling can compensate for the loss of frequency through analysis of the power spectrum in the clock base, and applying a band-pass filter provides a stable sine wave signal.

In this paper, continuous time equalization, clock channel leveling, and band-pass filters were applied, and experiments and simulations were performed such as TX+channel and TX+Equalizer. These results can be seen to be very effective at high speeds, including the application of blender and band-pass filters in equalizing conditions and the amount of attenuation without comparator. Thus, as in the results of this study, applying clock adaptation not only reduces each receiver power comparison, but also operates at high speeds without a comparator. However, given the need for additional pins to be used for adaptation, this architecture has some disadvantages and requires a simple design that takes into account economics in the future.

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