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1.9-GHz CMOS Power Amplifier using Adaptive Biasing Technique at AC Ground

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Abstract

A 1.9-GHz linear CMOS power amplifier is presented. An adaptive bias circuit (ABC) that utilizes an AC ground to detect the power level of the input signal is proposed to enhance the linearity and efficiency of the power amplifier. The ABC utilizes the second harmonic component as the input to mitigate the distortion of the fundamental signal. The input power level of the ABC was detected at the AC ground located at the V_{DD} node of the power amplifier. The output of the ABC was fed into the inputs of the power stage. The input signal distortion was mitigated by detecting the input power level at the AC ground. The power amplifier was designed using a 180 nm RFCMOS process to evaluate the feasibility of the application of the proposed ABC in the power amplifier. The measured output power and power-added efficiency were improved by 1.7 dB and 2.9%, respectively.

Index Terms: AC ground, Adaptive biasing, Amplifier, Differential, Second harmonic

I. INTRODUCTION

Owing to the continuous increase in the required data rates for wireless communication, the linearity of power amplifiers has become important in recent times [1-3]. Therefore, various linearization techniques have been actively introduced [4, 5]. The adaptive biasing technique is a popular linearization technique regarded to be simpler and more effective than other such techniques [6]. In general, the input power of a power amplifier is detected using a coupler and fed into an adaptive bias circuit (ABC). The ABC then detects the envelope of the input signal and generates the gate bias voltage of the power stage based on the envelope as shown in Fig. 1. As the bias voltage varies according to the envelope of the radio frequency (RF) signal, the linearity of the power amplifier is enhanced. Although the adaptive biasing technique was developed for heterojunction bipolar transistor (HBT)-based power amplifiers, it could also be easily utilized in the linearization of CMOS power amplifiers.

However, some challenges must be addressed to improve the feasibility of applying the adaptive biasing technique to a power amplifier. As shown in Fig. 1, power detection is essential in the adaptive biasing technique. However, as the impedance at the node for power detection can be varied by the power detector, the power detection may distort the RF signal. Even if there is no signal distortion, as a part of the RF signal is used for power detection, the gain of the power

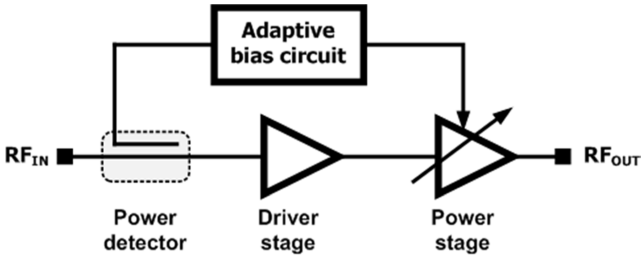

Fig. 1. Conceptual block of an adaptive biasing circuit for a power amplifier.

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amplifier may be degraded. In this study, the power is detected at an AC ground node located at the driver stage to minimize the signal distortion and gain degradation caused by power detection.

II. ADAPTIVE BIASING TECHNIQUE USING AC GROUND

Fig. 2 illustrates the concept of the adaptive biasing technique using an AC ground. In general, a CMOS power amplifier is designed using a differential structure to generate the AC ground to avoid gain reduction problems caused by the parasitic inductance of the bond wires. As shown in Fig. 2, if the fundamental signal is differentially fed, the AC ground for the fundamental signal is generated at the V_{DD} and ground pads. Therefore, the impedances of the bond wires connected to the V_{DD} and ground pads may be ignored for the fundamental signal. Conversely, for the even-harmonic components, which are the common-mode signals in the differential circuits, the parasitic inductances of the bond wires at the V_{DD} and ground pads should be considered as their impedances. Consequently, if the power amplifier operates as a perfect differential amplifier, only even-harmonic voltages exist at the V_{DD} and ground pads.

In general, a second harmonic component is dominant among even-harmonic components. Fig. 3 shows the power levels of the fundamental and second harmonic components. As shown in Fig. 3, the power level of the second harmonic components is proportional to that of the fundamental components. Accordingly, in this study, the power of the second harmonic components is detected for the adaptive biasing technique.

Fig. 4 shows the proposed power amplifier using the adaptive biasing technique. As shown in Fig. 4, the second harmonic power generated at the V_{DD} pad of the driver stage is fed into the input of an ABC. The ABC detects the envelope of the second harmonic power, which is proportional to the power of the fundamental component. The detected envelope becomes the gate bias of the power stage; this completes the implementation of the adaptive biasing technique. Moreover, the second harmonic component is typically suppressed in the linear power amplifier. The proposed power-detection method uses the second harmonic component and thus helps suppress it.

III. DESIGN OF THE PROPOSED POWER AMPLIFIER

A 1.9-GHz CMOS power amplifier and ABC are designed using a 180 nm RFCMOS process, which provides six metal layers, to investigate the feasibility of applying the proposed adaptive biasing technique to the linear power amplifier. Fig. 5 is a schematic of the designed ABC. The fed second harmonic component is first amplified using the two-stage amplifiers. For a stable operation of the two-stage amplifiers,

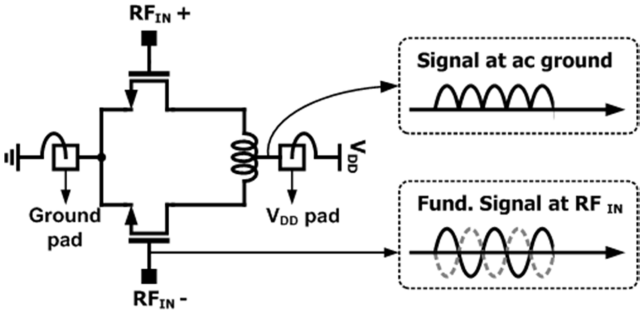


Fig. 2. Adaptive biasing technique using an AC ground.

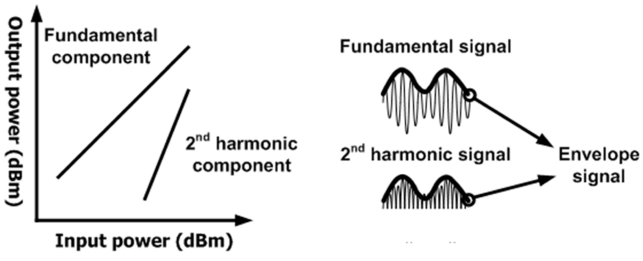


Fig. 3. Power levels and waveforms of the fundamental and second-harmonic components.

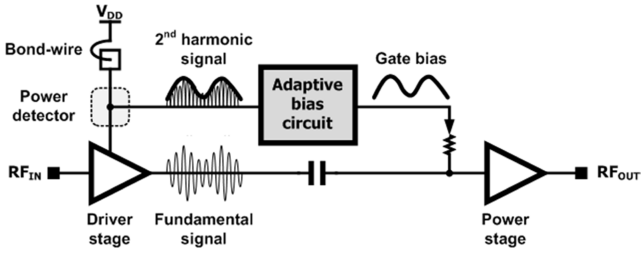


Fig. 4. Conceptual block of the proposed adaptive biasing technique.

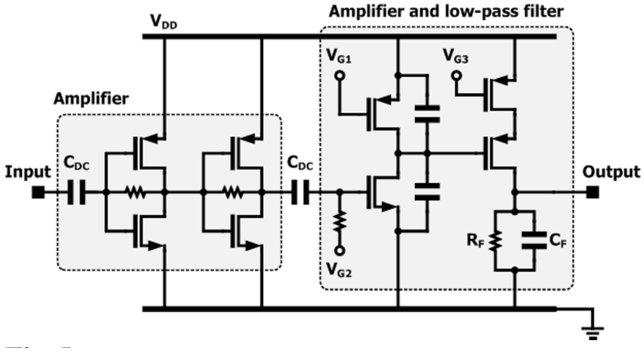


Fig. 5. Simple schematic of the designed ABC.

a feedback resistor is used between the input and output of each amplifier. The stage after the inverter-type two-stage amplifiers is a low-pass-filter-embedded amplifier as shown in Fig. 5. The ripple voltage of the output signal is minimized through the values of the capacitors and resistors of the low-pass-filter-embedded amplifier stage.

Fig. 6 is a schematic of the designed 1.9 GHz CMOS power amplifier with the proposed ABC with a supply voltage of 3.3 V. The amplifier is composed of driver and power stages to achieve an acceptable power gain. A cascade structure is adopted to avoid the breakdown problems of transistors [7-9]. For the differential operation with single-ended input and output signals, transformers are used in the input and output matching networks. The transformers are designed using the sixth metal layer to minimize the silicon substrate loss and resistive loss. The input and output matching networks are implemented using the transformers and metal-insulator-metal capacitors. The input and output transformers are designed using 2.5-dimensional electromagnetic simulation. The supply voltage of the power amplifier is fed through the center-tap of the primary part of the output transformer and the differential inductor of the driver stage. The input power of the ABC is detected at the V_{DD} node of the driver stage, as shown in Fig. 6. The output voltage of the ABC is fed into the gate of the common-source transistor of the power stage through the resistor.

Fig. 7 shows the simulated gain according to the output power of the power amplifier with and without the ABC. The power gain of the power amplifier with the ABC is slightly increased in the high-power region, as shown in Fig. 7, owing to the increase in the gate bias caused by the ABC. The output voltage of the ABC can be controlled by varying the value of R_F shown in Fig. 5.

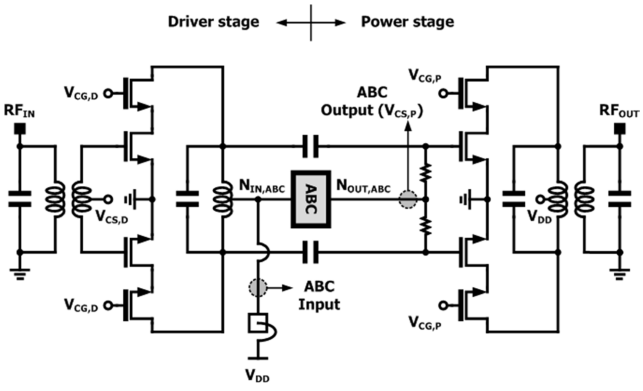


Fig. 6. Simple schematic of the designed CMOS power amplifier.

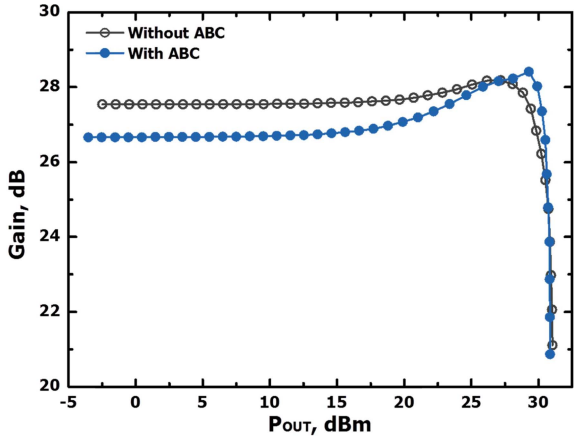
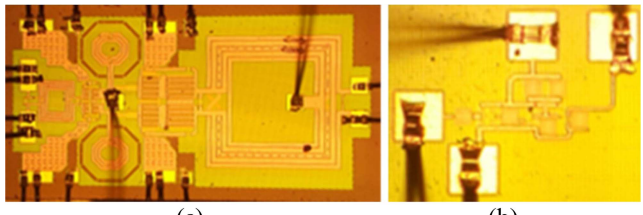


Fig. 7. Simulation results: gain according to the output power.

IV. EXPERIMENTAL RESULTS

Fig. 8 shows the chip photographs of the designed power amplifier and ABC. The chip sizes of the power amplifier and ABC are 0.98 mm × 2.07 mm and 0.27 mm × 0.6 mm, respectively. The core size of the ABC shown in Fig. 8(b) is 0.07 mm × 0.25 mm. In this study, the power amplifier and ABC are separately designed to place test pads for measuring the inner signals of the power amplifier and ABC. However, owing to the sufficiently small core size of the ABC, it could be readily integrated with the power amplifier without an additionally required chip area. The designed chips are mounted on a printed circuit board to obtain measurement data.

Fig. 9 shows the measured input power and output voltage at $N_{IN,ABC}$ and $N_{OUT,ABC}$, respectively. The measured second harmonic is not linear according to the input power of the power amplifier as shown in Fig. 9(a). However, the second harmonic increases monotonically as the input power increases until the input power reaches approximately 5 dBm. Considering the measured gain of the power amplifier, the input power of 5 dBm is sufficient to reach the saturation output power of the power amplifier. From the measured results shown in Fig. 9, we confirm that the designed ABC detects the power of the second harmonic at the ABC input, $N_{IN,ABC}$, until the input power reaches approximately 5 dBm. Fig. 9(b) shows the output voltage of the ABC according to the input power of the ABC, which is the second harmonic of the power amplifier. In this case, the designed power amplifier has the saturation power and gain of approximately 30



(a) (b)

Fig. 8. Chip photographs: (a) power amplifier and (b) adaptive bias circuit.

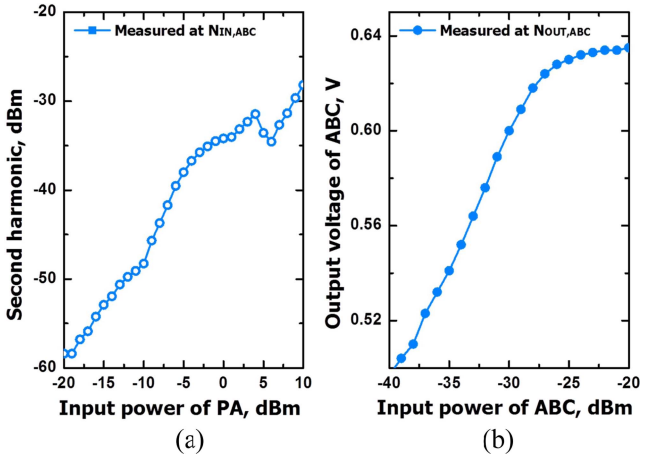


Fig. 9. Measured results based on input power: (a) second harmonic at $N_{IN,ABC}$ and (b) output voltage of ABC.

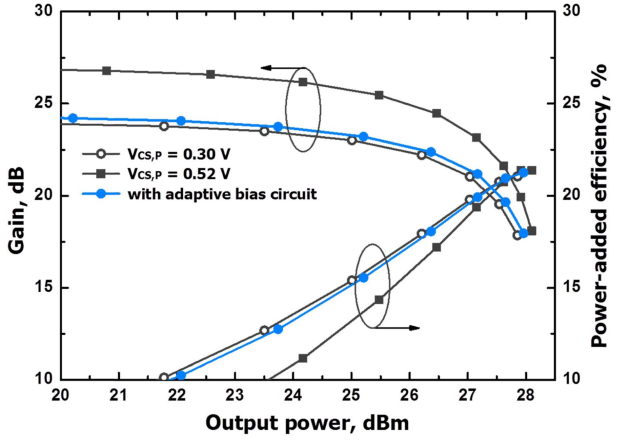


Fig. 10. Measured gain and PAE according to the output power.

dBm and 26.5 dB, respectively. Therefore, the maximum linear input power is lower than 5 dBm.

Fig. 10 shows the measured gain and power-added efficiency (PAE) according to the output power P_{OUT} of the proposed power amplifiers at the operating frequency of 1.9 GHz. The measured 1 dB compression point (P1dB) and the PAE at P1dB were 25.2 dBm and 15.5%, respectively. In the low-power region, the output of the ABC was approximately 0.3 V. Therefore, the PAE of the designed power amplifier with ABC was similar to that in the case of $V_{CS,P}$ of 0.3 V. However, as the output power increased, the output voltage of the ABC increased beyond 0.3 V. Consequently, the P1dB and the PAE at P1dB improved by 1.7 dB and 2.9%, respectively. In this case, the measured current consumption in the ABC was lower than 1 mA.

V. CONCLUSION

In this study, a 1.9-GHz CMOS power amplifier with adaptive biasing was designed using a 180 nm RFCMOS process.. In general, the adaptive biasing technique utilizes the fundamental signal to detect its power. However, in this work, the power of the second harmonic components generated at the AC ground node of the differential driver stage was used to detect the power of the fundamental signal. The signal distortion and gain degradation problems were also minimized by detecting the power of the second harmonic component. The output voltage of the ABC was fed into the gate of the common-gate transistor of the power stage. Based on the measured results, the feasibility of applying the proposed adaptive biasing technique in RFCMOS power amplifiers was confirmed.

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REFERENCES

[1] S. Kang, D. Baek, and S. Hong, "A 5-GHz WLAN RF CMOS power amplifier with a parallel-cascoded configuration and an active feedback linearizer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 9, pp. 3230-3244, 2017. DOI: 10.1109/TMTT.2017.2691766.

[2] J. Yoo, C. Lee, I. Kang, M. Son, Y. Sim, and C. Park, "2.4-GHz CMOS linear power amplifier for IEEE 802.11n WLAN applications," *Microwave and Optical Technology Letters*, vol. 59, no. 3, pp. 546-550, 2017. DOI: 10.1002/mop.30343.

[3] Y. Jin and S. Hong, "A 2.4-GHz CMOS common-gate combining power amplifier with load impedance adaptor," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 9, pp. 836-838, 2017. DOI: 10.1109/LMWC.2017.2734748.

[4] Y. Hu and S. Boumaiza, "Doherty power amplifier distortion correction using an RF linearization amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 5, pp. 2246-2257, 2018. DOI: 10.1109/LMWC.2017.2734748.

[5] A. K. Kwan, M. Younes, O. Hammi, M. Helaoui, and F.M. Ghannouchi, "Linearization of a highly nonlinear envelope tracking power amplifier targeting maximum efficiency," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 1, pp. 82-84, 2017. DOI: 10.1109/LMWC.2016.2629983.

[6] S. Chen, G. Wang, Z. Cheng, P. Qin, and Q. Xue, "Adaptively biased 60-GHz doherty power amplifier in 65-nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 3, pp. 296-298, 2017. DOI: 10.1109/LMWC.2017.2662011.

[7] J. Jang, J. Yoo, M. Lee, and C. Park, "A 2.4-GHz dual-mode CMOS power amplifier with a bypass structure using three-port transformer to improve efficiency," *Journal of Korea Institute of Information and Communication Engineering*, vol. 23, no. 6, pp. 719-725, 2019. DOI:

10.6109/jkiice.2019.23.6.719.
[8] S. Jang, C. Lee, and C. Park, "Differential 2.4-GHz CMOS power amplifier using an asymmetric differential inductor to improve linearity," *Journal of Korea Institute of Information and Communication Engineering*, vol. 23, no. 6, pp. 726-732, 2019. DOI: 10.6109/jkiice.2019.23.6.726.
[9] Y. Sim, J. Park, J. Yoo, C. Lee, and C. Park, "A CMOS power amplifier using an active balun as a driver stage to enhance its gain," *Microelectronics Journal*, vol. 63, pp. 160-169, 2017. DOI: 10.1016/j.mejo.2017.04.003.

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