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CMOS true-time delay IC for wideband phased-array antenna

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This paper presents a true-time delay (TTD) using a commercial 0.13-μm CMOS process for wideband phased-array antennas without the beam squint. The proposed TTD consists of four wideband distributed gain amplifiers (WDGAs), a 7-bit TTD circuit, and a 6-bit digital step attenuator (DSA) circuit. The T-type attenuator with a low-pass filter and the WDGAs are implemented for a low insertion loss error between the reference and time-delay states, and has a flat gain performance. The overall gain and return losses are >7 dB and >10 dB, respectively, at 2 GHz–18 GHz. The maximum time delay of 198 ps with a 1.56-ps step and the maximum attenuation of 31.5 dB with a 0.5-dB step are achieved at 2 GHz–18 GHz. The RMS time-delay and amplitude errors are <3 ps and <1 dB, respectively, at 2 GHz–18 GHz. An output P1 dB of <−0.5 dBm is achieved at 2 GHz–18 GHz. The chip size is 3.3 × 1.6 mm^2, including pads, and the DC power consumption is 370 mW for a 3.3-V supply voltage.

KEYWORDS
beam squint, CMOS, low-amplitude error, true-time delay, wideband phased-array antenna

1 | INTRODUCTION

Complementary metal-oxide semiconductor (CMOS)-based phased-array antennas have been widely used in radar and communication systems because of their electronic beam-forming, signal-to-noise ratio (SNR), and spatial diversity capabilities [1,2]. In general, phase shifters are used for narrowband phased-array antennas. However, phase shifters cannot be applied in wideband phased-array antennas owing to the beam squint, where the beam-steering angle is distorted depending on the frequency [3]. Therefore, the true-time delay (TTD), which provides a constant time delay over the frequency, is one of the most essential elements in wideband phased-array antennas because of the reduced beam squint and high resolution that are achieved. Insertion loss errors between reference and time-delay states are normally generated in switched-path TTD circuits [4]. In addition, the insertion loss of the time delay is increased as the frequency increases. Therefore, the passive circuit for the equalized insertion loss and an amplifier with a positive gain slope are required for low insertion loss errors and flat gain performance. CMOS-, microelectromechanical systems (MEMS)-, and GaAs-based TTDs have been reported as trombone or active distributed configurations, but they do not have a compact size or flat gain performance [5–8].

This paper presents the TTD for a wideband phased-array antenna using commercial 0.13-μm CMOS technology. The proposed TTD has a compact size and low insertion loss error with a T-type attenuator, and it has a flat gain performance with a distributed amplifier at 2 GHz–18 GHz.

2 | DESIGN OF CMOS WIDEBAND TRUE-TIME DELAY

Figure 1 shows the block diagram of the proposed CMOS-based TTD for a wideband phased-array antenna. The proposed TTD consists of a 7-bit TTD circuit, a 6-bit digital step attenuator (DSA) circuit, wideband distributed gain

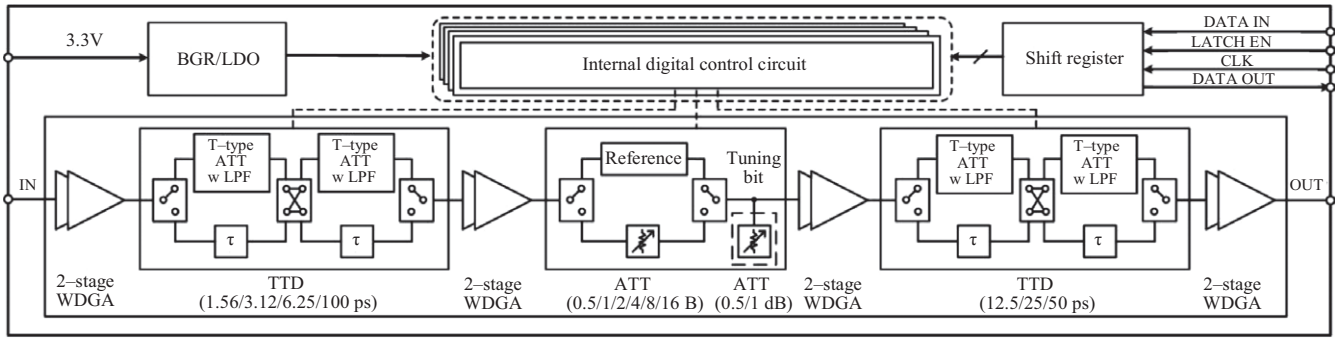

FIGURE 1 Block diagram of the proposed CMOS-based true-time delay

amplifiers (WDGAs), and a serial peripheral interface (SPI). Artificial transmission lines and single-pole double throw (SPDT) and double-pole double throw (DPDT) switches are used in the 7-bit TTD and the 6-bit DSA circuits. The DSA circuit, which includes 2-bit tuning bits of 0.5 dB and 1 dB, is between the WDGAs with the positive gain.

A 20-bit shift register is used to control the TTD and DSA circuits, and tuning bits provide a daisy-chain connection to make it easy to control the proposed TTD for large-scale antenna arrays. All of the inductors, grounded coplanar waveguide (CPW) lines, interconnection lines, and RF pads are simulated using an electromagnetic (EM) solver.

2.1 | Wideband distributed gain amplifier

Figure 2 shows the schematic of the WDGA. The distributed gain amplifier consists of two-stage cascade transistor pairs (T_1, T_2), distributed inductors (L_{G1}, L_{G2}, L_{D1}, L_{D2}), 50-Ω termination resistors (R_{TERM}), and RF choke inductors (L_C). Because the insertion losses in the TTD and DSA circuits are increased as the frequency increases, the DGA with a positive gain slope is designed to provide flat gain performance. Vertically stacked spiral inductors with top metal (M8) and two connected metals (M7 and M6) were used to reduce the inductor size and to improve the Q-factor of the inductors.

2.2 | 7-bit true-time delay

The proposed 7-bit TTD circuit is composed of SPDT and DPDT switches and time-delay elements, as shown in Figure 3. The long-time-delay elements of 6.25 ps, 12.5 ps, 25 ps, 50 ps, and 100 ps were implemented with cascading artificial transmission lines using a coupled line coupler (CLC) network. Vertically stacked spiral inductors were used in the artificial delay line to reduce the chip size. Metal-oxide metal (MOM) capacitors were implemented using the top plate of M2, M4, M6, and M8 metals and the bottom plate of M3, M5, and M7 metals. The amplitude error between the reference state and the time-delay state is high because the artificial delay line has a high insertion loss at long-time delays, which is caused by the limited Q-factor of the inductor. In order to compensate the amplitude errors in the long-time-delay elements, T-type attenuators with a negative gain slope are required at the reference

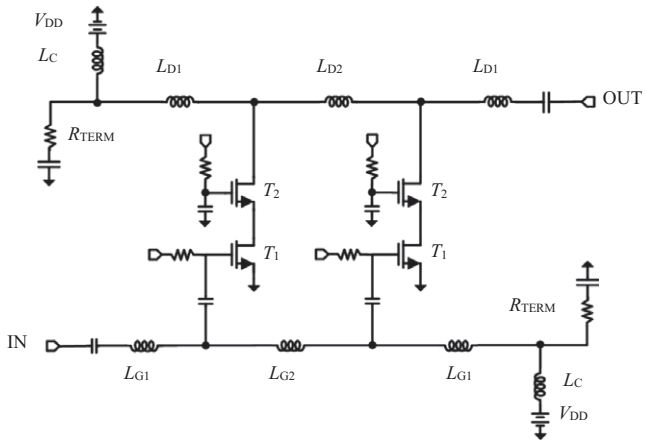

FIGURE 2 Schematic of the two-stage wideband distributed gain amplifier

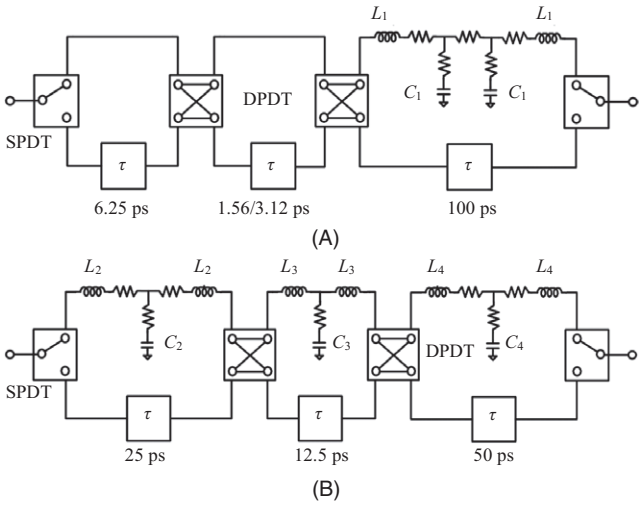

FIGURE 3 Schematics of the true-time delay circuits of (A) 1.56 ps, 3.12 ps, 6.25 ps, 100 ps and (B) 12.5 ps, 25 ps, 50 ps

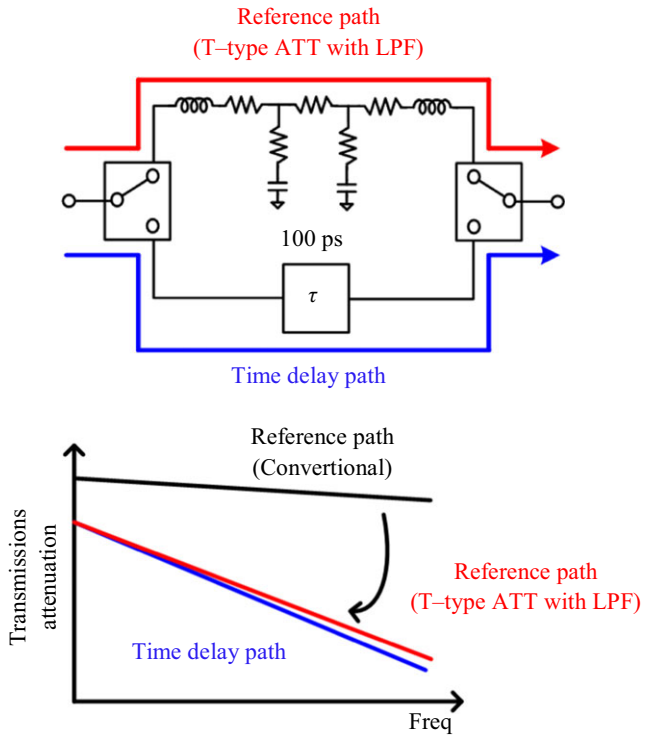

FIGURE 4 Schematic of the true-time delay circuit (100 ps) with a T-type attenuator at the reference path and the characteristic of transmission attenuation

state as amplitude equalizers, as shown in Figure 4. The short-time-delay elements of 1.56 ps and 3.12 ps were implemented using grounded CPW transmission lines.

2.3 | 6-bit digital step attenuator

The 6-bit DSA circuit was designed using the switched T-type topology, which is adequate for a small chip area and low insertion loss [9]. Figure 5A shows the schematic of the high attenuation states of 2 dB, 4 dB, and 8 dB including a phase-compensation capacitor (C_P). The attenuation state of 16 dB was implemented with two cascaded 8-dB attenuators. The low attenuation states of 0.5 dB and 1 dB, including two-bit tuning bits, which serve to correct the amplitude errors, were only implemented with a shunt resistor and a shunt switch transistor in the T-type attenuator, as shown in Figure 5B.

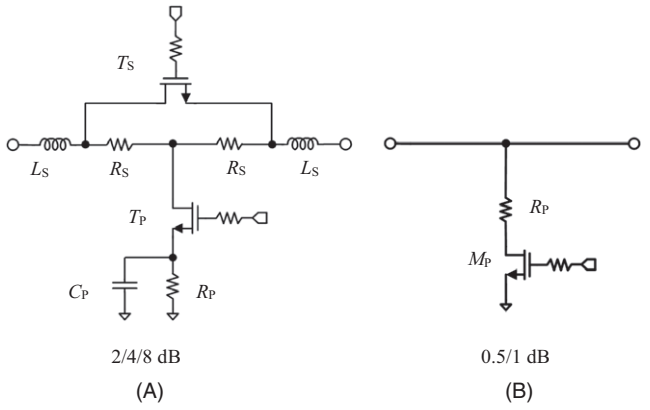

FIGURE 5 Schematics of the switched T-type attenuator circuits of (A) 2 dB, 4 dB, 8 dB and (B) 0.5 dB, 1 dB

3 | MEASUREMENT RESULTS

The proposed TTD for wideband phased-array antennas was fabricated using commercial 0.13-μm CMOS technology. Figure 6 shows the microphotograph of the fabricated TTD. The chip size is 3.3 × 1.6 mm^2, including pads. The proposed TTD was on-wafer tested using a performance network analyzer (PNA), for which the short, open, load, through (SOLT) calibration was performed. Figure 7 shows the measured *S*-parameters of the reference states. The measured gain and input/output return losses are >7 dB and >10 dB at 2 GHz–18 GHz, respectively. In general, two different delay functions, namely the time delay and the group delay, are used to determine the phase linearity

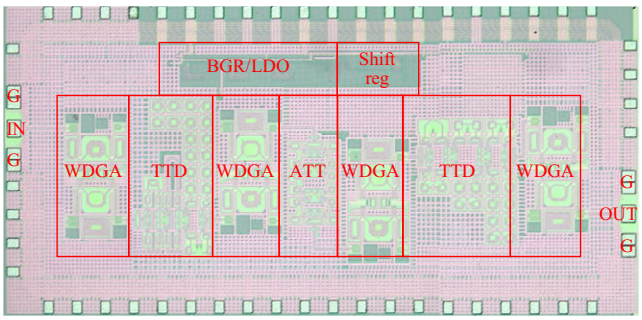

FIGURE 6 Microphotograph of the proposed CMOS-based TTD

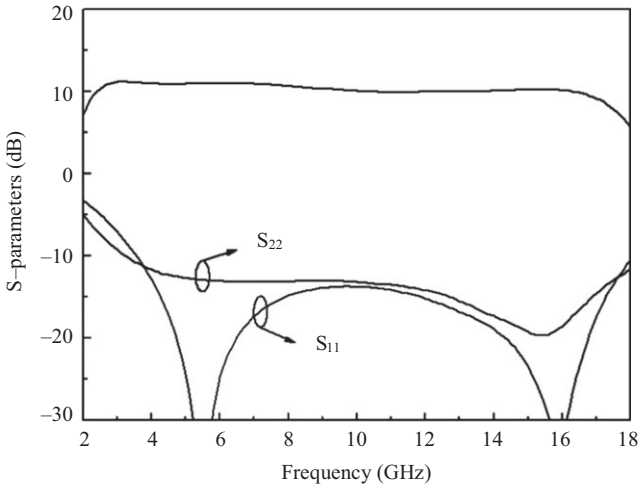

FIGURE 7 Measured S-parameters of the proposed wideband TTD

of systems [10]. The time delay ($\tau_{\text{Timedelay}}$) and the group delay ($\tau_{\text{Groupdelay}}$) are as follows:

$$\tau_{\text{Timedelay}} = -\frac{\phi}{\omega},$$

$$\tau_{\text{Groupdelay}} = -\frac{d\phi}{d\omega},$$

where ϕ is the total phase shift in radians and ω is the angular frequency in radians per unit time. The measured relative time-delay range of 198 ps with a 1.56-ps step and relative group delay of <0.25 ns in all states are achieved at 2 GHz–18 GHz, as shown in Figures 8 and 9. Figure 10 shows that the relative attenuation and the attenuation range of 31.5 dB with a 0.5-dB step in all states is achieved at 2 GHz–18 GHz. Figure 11 shows the measured RMS time-delay error of <3 ps and the RMS amplitude error of <1 dB for all states at 2 GHz–18 GHz, respectively. The measured output P1 dB of <−0.5 dBm was achieved at 2 GHz–18 GHz, as shown in Figure 12. Figure 13 shows the synthesized beam patterns for an 8 × 8 array antenna based on

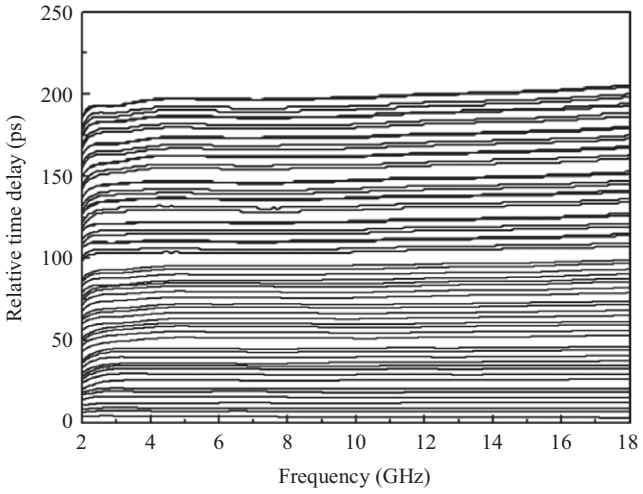

FIGURE 8 Measured relative time delay in all states

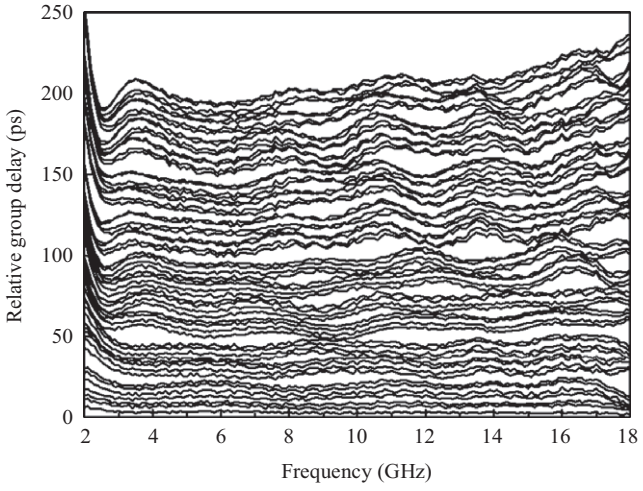

FIGURE 9 Measured relative group delay in all states

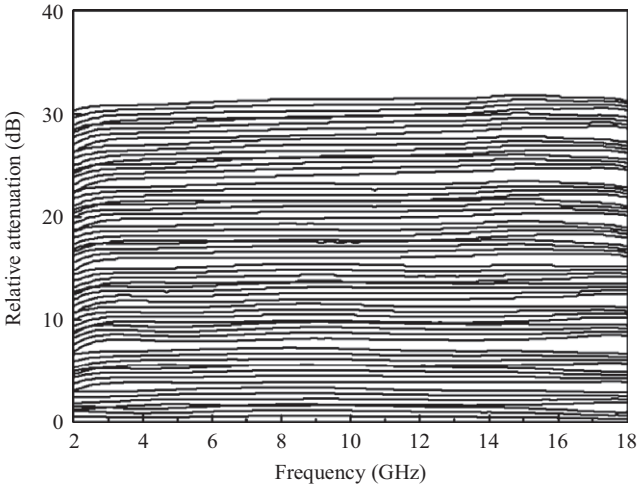

FIGURE 10 Measured relative attenuation in all states

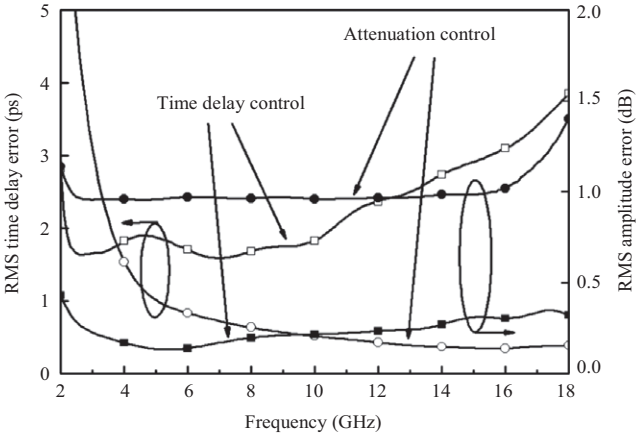

FIGURE 11 Measured RMS time-delay and amplitude errors

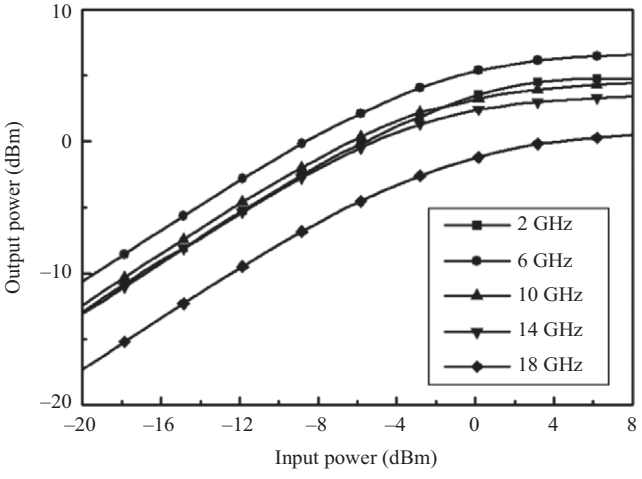

FIGURE 12 Measured power characteristics

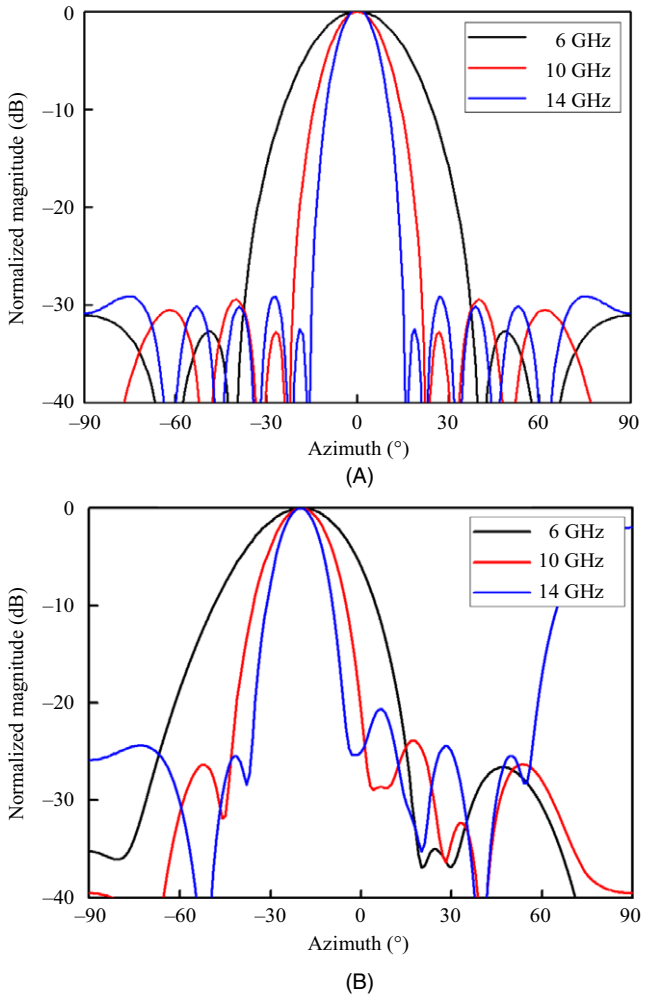

FIGURE 13 Synthesized beam patterns of (A) 0° scanned and (B) 20° scanned with the measured *S*-parameters

the measured *S*-parameters, and the reduced beam squint is achieved at 2 GHz–18 GHz. The total DC power consumption is 370 mW with a 3.3-V supply voltage. Table 1 shows a comparison of the previously published TTDs.

4 | CONCLUSION

This paper presents a CMOS-based TTD for wideband phased-array antennas. The proposed TTD exhibits a time-delay range of 198 ps and an amplitude range of 31.5 dB. For low-amplitude and time-delay errors, the T-type attenuators with a low-pass filter (LPF) in the TTD circuit and a shunt capacitor in the DSA circuit are required and achieved, with an RMS time-delay error of <3 ps and an RMS amplitude error of <1 dB at 2 GHz–18 GHz. WDGAs with a positive gain slope were implemented to compensate the high insertion loss and flat gain performance. In addition, a reduced beam squint with the synthesized beam patterns was achieved at 2 GHz–18 GHz. The proposed CMOS-based TTD with low cost and compact size can be applied to wideband phased-array antennas without the beam squint.

TABLE 1 Comparisons of true-time delays

	[11]	[12]	[13]	This work
Tech	0.55 μm pHEMT	0.25 μm pHEMT	0.13 μm CMOS	0.13 μm CMOS
Freq. (GHz)	2–17	6–18	8–16	2–18
Gain (dB)	6	12	–1	7
Time-delay range (ps)	124/4	255/1	198/1.56	198/1.56
Att. range (dB)	23.25/0.75	31.75/0.25	31.5/0.5	31.5/0.5
RMS time-delay error (ps)	N/A	1.7	N/A	3
RMS amplitude error (dB)	N/A	N/A	N/A	1
OP1 dB (dBm)	N/A	16.5	N/A	–0.5
Power (W)	2.3	1.6	0.28	0.37
Size (mm^2)	4.6 × 5.4	4 × 5	2.65 × 1.47	3.3 × 1.6

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