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Large Signal Determination of Non-Linear Output Capacitance of Gallium-Nitride Field Effect Transistors from Switch-Off Voltage Transients – A Numerical Method

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Abstract

The output capacitance of power semiconductor devices is important in determining the switching losses and in the operation of some resonant converter topologies. Thus, it is important to be able to accurately determine the output capacitance of a particular device operating at elevated power levels so that the contribution of the output capacitance discharge to switch-on losses can be determined under these conditions. Power semiconductor switch manufacturers usually measure device output capacitance using small-signal methods that may be insufficient for power switching applications. This paper shows how first principle methods are applied in a novel way to obtain more relevant large signal output capacitances of Gallium-Nitride (GaN) FETs using the drain-source voltage transient during device switch-off numerically. A non-linear capacitance for an increase in voltage is determined with good correlation. Simulations are verified using experimental results from two different devices. It is shown that the large signal output capacitance as a function of the drain-source voltage is higher than the small signal values published in the data sheets for each of the devices. It can also be seen that the loss contribution of the output capacitance discharging in the channel during switch-on correlates well with other methods proposed in the literature, which confirms that the proposed method has merit.

Key words: GaN FET, Large signal analysis, Numerical method, Output capacitance, Switching transients

I. INTRODUCTION

Output capacitance (C_{oss}) is defined as the sum total of the drain-source and gate-drain capacitances of field effect transistors such as MOSFETs, SiC MOSFETs and GaN-FETs [1]. Output capacitance is non-linear in nature and its value generally reduces as a function of the drain-source voltage of a device, V_{ds}. Manufacturers usually publish curves in datasheets representing output capacitance as a value of the drain-source voltage. However, the data is obtained using small-signal measurement methods, where the device is dc-biased and the capacitance is measured using appropriate instrumentation. This value is usually measured at 25V. Some attempts have been made to measure the C_{oss} of devices operating at elevated power levels [2]. However, the process is rather complicated. A more detailed discussion on the work done in the past follows in the next section.

In loss calculations, the discharge of the output capacitance and the dissipation of the energy in the drain-source resistance of the device is often ignored during switch-on. A significant output capacitance ends up yielding incorrect loss values if only the switching transients of the drain-source voltage and current are used [3]. Excessive ringing in these waveforms also hampers accurate loss determination [4].

The effects of the output capacitance of devices on switching transients are usually ignored under low frequency operation or when the rise and fall-times of the current through the device are relatively long. The rise and fall-times of new GaN-FET devices are in the order of a few nanoseconds and they are

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believed to be capable of switching at sub-nanosecond times [5], which makes the effect of output capacitance all the more important [6]. These devices enable designers to develop power converters operating at frequencies up to 100MHz [6], [7]. The resonant frequency of Class-E and Class DE converters are very sensitive to variations in circuit parameters, with the output capacitance being one of the most important [8], [9]. Some designers use a single value called C_{oss} effective, and a method for determining this value is described in [10]. This method is based on a capacitance value that gives the same charge time as the output capacitance when V_{DS} rises from 0V to 80% of the maximum value and the gate-source voltage is zero. This is the recommended value for resonant cases.

In the absence of analytical approaches, a better understanding and accurate measurement of non-linear output capacitance is required to enable a better design, analysis and switching loss prediction [11], [12]. The novel numerical method proposed here provides users with an accurate way of determining large signal output capacitance, as a function of drain-source voltage, easily and accurately. This ensures a quicker time-to-market for products since the cooling requirements can be designed more accurately from early in the design process.

II. PROBLEM STATEMENT AND PROPOSED METHOD

Capacitance is a measure of the ability of a structure to store energy in an electric field created within the structure. The output capacitance of a field effect transistor is a result of the complex semiconductor and packaging structure. However, the method by which a charge enters or exits a structure as well as the associated losses are not accounted for and will be determined by the electromagnetic properties of the structure. These effects cannot be predicted using analytical methods or finite element methods. Therefore, the values of the output capacitance of power electronic switching devices measured using small signal measurements are believed to differ from large signal capacitances as acknowledged in [2]. Methods for determining large signal non-linear capacitance have also been discussed in [13], [14] and [15]. The method in [13] relies on a linear capacitor used in series with the device, which is kept in the off-state. Assuming that the power amplifier in [13] produces a sinusoidal output voltage, the results are valid for resonant and quasi-resonant converter operations as discussed in [14]. In the present study, non-linear capacitance is determined for a device that is switched off hard, where the charge displacement vastly differs from pure or quasi-sinusoidal conditions and when the charge stored in the output capacitance discharges very quickly during turn-on.

A novel, simplified method is proposed here where the switch-off transient of a device is used to determine the output capacitance as a function of the drain-source voltage. This power semiconductor device is switched into a resistive load using a transmission line setup. This method of charging C_{oss} through a resistor has been used in other works [2], [10], [13], [16] and [17]. However, it must be stated that the transmission line setup should be used for very fast transients that can be accomplished with the GaN FETs used in this work, where the parasitic effects in the layout become very cumbersome since they obscure the true transient waveforms. For example, the switching transients in [16] are very long when compared to those of the GaN FETs achieved in this work, and the effects of parasitic circuital elements are either neglected or not reported.

Another important distinction to be aware of from the literature is that the reasons for being interested in C_{oss} are different for hard-switched and ZVS applications. In [2] the inadequacy of former methods is pointed out when it comes to ZVS loss estimates, and it also proposes a new figure of merit for the devices used in ZVS applications.

The method proposed in [17] is based on an integral relationship between small-signal values and large signal values. The maximum current in the experimental setup is only 80mA, which raises questions about charge distribution and current crowding in devices at higher current levels.

The authors of [16] admit that errors occurred with thermometric measurements in spite of attempts to calibrate them against values of dissipation obtained under known dc-conditions. It further emphasizes that true total loss measurement can only be done with calorimetric methods, which unfortunately do not separate loss contributions. The present work also distinguishes itself from other methods in that the numerical method devised is unique.

First, it is important to consider the origin of the proposed numerical method when a known value of capacitance is used to determine the capacitor voltage charging in a RC-circuit. The reverse numerical process are used later to determine the capacitance from the transient.

Consider the two simple RC-charge circuits in Fig. 1. One has a linear capacitor and the other has a non-linear capacitor with $C_{2\ Init} = C_1$. The resistance and capacitance values are arbitrarily chosen and $R_1 = R_2$.

Both circuits are subject to voltage steps with steady-state values $V_1 = V_2$. It is well-known that voltage across a linear capacitor as a function of time can be calculated with Equ. (1) and plotted as shown in Fig. 2. The same figure also shows a LTSpice® simulated transient response which should exactly follow the response obtained by the analytical method.

$$v_c(t) = V_{Step}(1 - e^{\frac{-t}{RC}}) \quad (1)$$

If the equation for a non-linear capacitor as a function of the capacitor voltage is known, the transient of the capacitor voltage can be predicted fairly accurately by following the process mathematically described in Equ. (2) and Equ. (3).

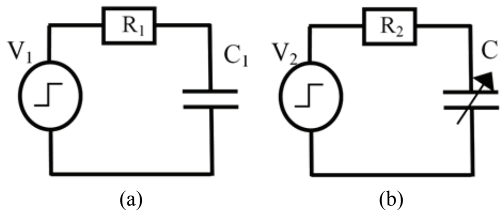

Fig. 1. Circuit diagrams of: (a) RC-circuit with a linear capacitance; (b) RC-circuit with a non-linear capacitance.

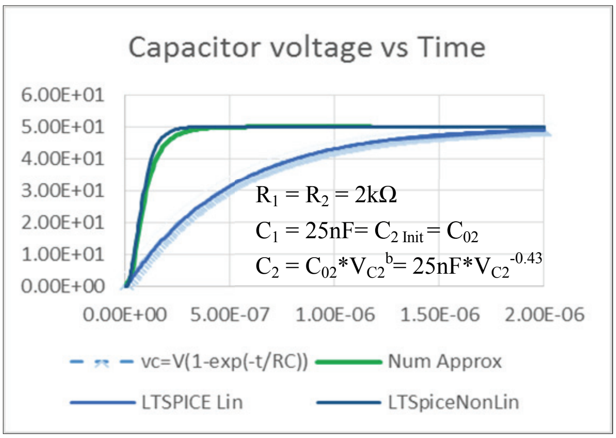

Fig. 2. Capacitor voltage transients for linear and non-linear capacitors.

Use Equ. (2) to accurately calculate the new value of the capacitance based on the previous capacitor voltage. Equ. (2) is used in this work to describe the output capacitance as a function of the capacitor voltage since it proved to yield the best fit for most of the results shown later.

$$C_n = C_o \times V_{n-1}^b \tag{2}$$

In Equ. (2) C_o is the capacitance at zero volts, and V_{n-1} is the value of the voltage calculated for the previous time step raised to the power of *b*, which is obtained from the curve fitting procedure. The value of b is also chosen arbitrarily. Thus, C_n is the new value of the capacitance based on the previous value of the voltage across it.

$$v_c(t_n) = V_{Step}(1 - e^{\frac{-t_n}{RC_{n-1}}}) \tag{3}$$

The process is repeated for each time step. The RC-circuit transients are simulated with LTSpice® and the method is applied for both linear and non-linear capacitors. The response is shown in Fig. 2 and is depicted as "Numerical Approximation". It can be seen from Fig. 2 that the numerical approximation closely resembles the simulated capacitor voltage for the non-linear capacitance.

If the non-linear capacitance as a function of the capacitor voltage is to be determined, the reverse numerical process is followed and is discussed after a brief discussion on how the actual switching transients were acquired and how the switching circuit can be simplified.

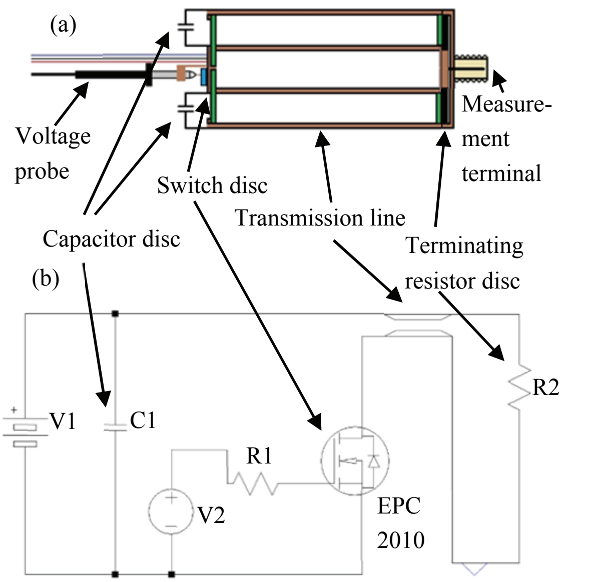

Fig. 3. Diagrams showing: (a) Sketch of transmission line of the experimental setup; (b) Transmission line experiment circuit.

A. Experimental Measurement of Switch-Off Transient Responses Using a Novel Transmission Line Setup

The work done in [14] and [15] accurately determined the switching transients of GaN-FETs. In order to do this, the switching transients should not be influenced by any circuit parameters such as the layout inductance or the power loop inductance as referred to and discussed in [1] and [4], which specifically address the issue where parasitic ringing hinders the extraction of switching losses. Although the switching devices in converters hardly ever switch into resistive conditions, a purely resistive load is the only load that reveals the true switching capability of the device. For experimental purposes a novel method has been employed where a transmission line, terminated into its characteristic impedance, was chosen to perform these measurements [14], [15]. Fig. 3(a) shows a graphic representation of the transmission line, and Fig. 3(b) shows a circuit diagram of the setup used in the simulation. Experimental switching transients were obtained by switching the GaN-FET in this electromagnetically defined environment. For practical reasons, a 50 Ω transmission line terminated into its characteristic impedance was used as explained in [13] and [14]. Very clean switching transients, free of any oscillatory or transmission line effects, were obtained for the EPC2010 (200V, 12A) and EPC2012 (200V, 3A) devices. The proposed methods are applied to both devices to evaluate the repeatability of the results yielded by them with different data sets.

B. Equivalent Circuits

Fig. 4 shows equivalent circuits resulting from the transmission line experiment. From Fig. 3, the GaN FET can be replaced with a switch S in Fig. 4(a), and the output capacitance of interest is added in parallel with the switch.

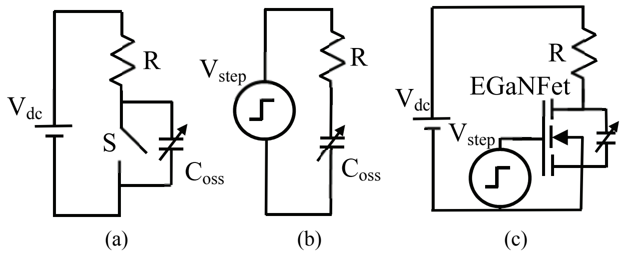

Fig. 4. Diagrams showing: (a) Switching circuit; (b) Simplified circuit used for simulation purposes; (c) LTSpice® circuit with the simulation and experimental setup.

When opening the switch in Fig. 4(a), the output capacitance, C_{oss}, charges through the load resistance, R, and the steady state open-circuit voltage should be equal to the source voltage, V_{dc}. Although the switch-off transients cannot be used to determine the switch-off time of the device, they are useful in determining the output capacitance under large signal conditions. The equivalent circuit can now be simplified further as shown in Fig. 4(b). This simplified circuit can then be used in simulations where the RC-circuit is stepped with a voltage source, which eliminates the necessity of using a switch in LTSpice®.

The actual device model used in the simulations in [13] and [14] is shown in Fig. 4(c), and the results of these simulations are shown and discussed in the experimental section of this work.

III. EXPERIMENTAL RESULTS

A. Device Switch-Off Transient Response

The switch-off transient waveforms of two different GaN power switches labeled ("Exp"=Experimental, and "Sim"= Simulated) are shown in Fig. 5 for the EPC2010 device and later in Fig. 8 for the EPC2012 device. The simulated transients were originally obtained using the circuit represented in Fig. 4(c) for the two devices and the experimental data with the transmission line experiment discussed earlier. The data in these graphs is used next to determine the output capacitance of each device using the reverse method previously discussed.

B. Determining Device Output Capacitance

With discrete voltage values obtained from the switch-off transients the values of C_{oss} can be calculated for each of the discrete steps using (4). The curves of the output capacitance as a function of voltage are called CExp and CSim in Fig. 6 for the EPC2010 device and again later in Fig. 9 for the EPC2012 device. The same figures contain graphs for the datasheet capacitance values labeled Datasheet and Power (Datasheet).

$$C_{oss}(v_c(t)) = \frac{-t}{R * \ln\left(1 - v_c(t)/V_{Step}\right)} \quad (4)$$

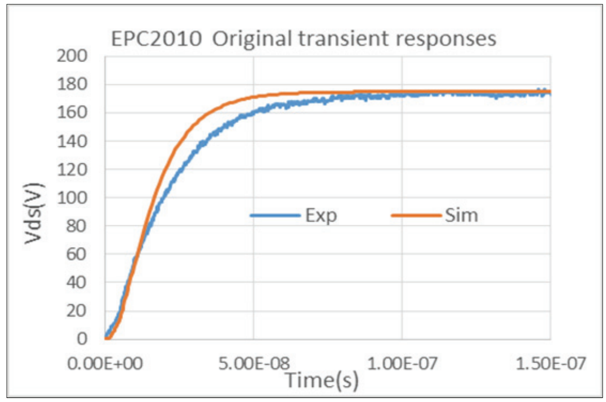

Fig. 5. Original experimental and simulated transient responses for an EPC2010.

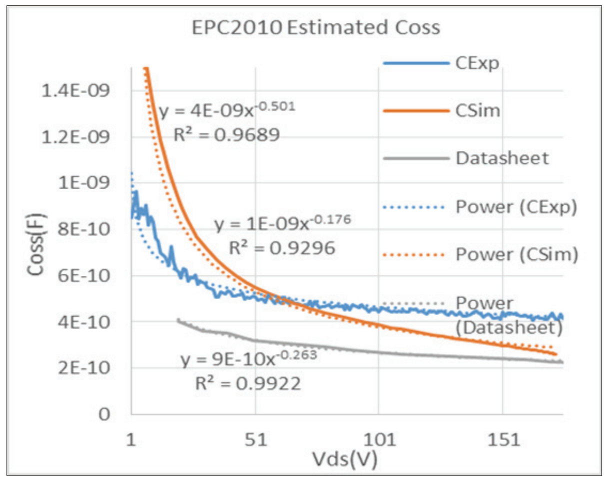

Fig. 6. Estimated output capacitance (EPC2010).

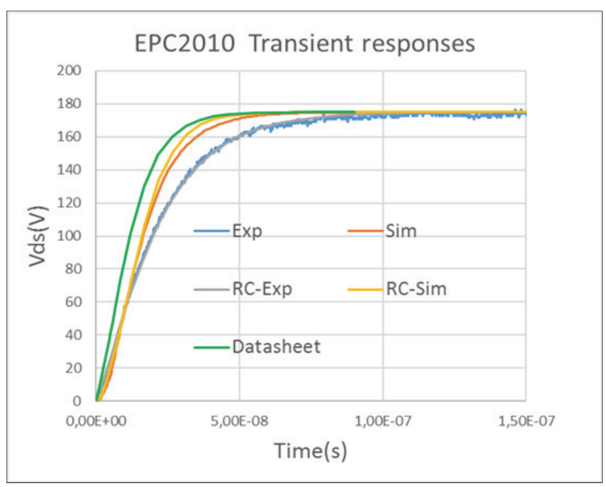

Fig. 7. Resulting transients using an estimated C_{oss} - EPC2010.

C. Curve Fitting

A curve fitting method in Microsoft EXCEL® can now be used to obtain an equation for the output capacitance as a function of the switch voltage for each of the mentioned

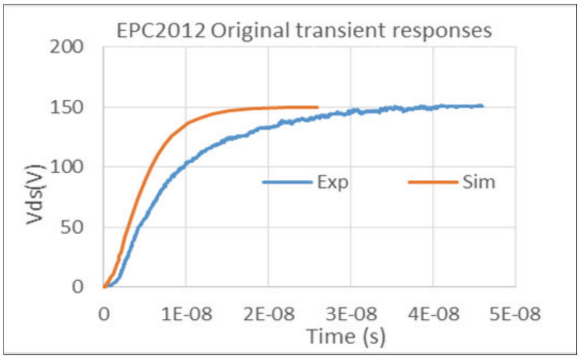

Fig. 8. Original experimental and simulated transient responses for an EPC2012.

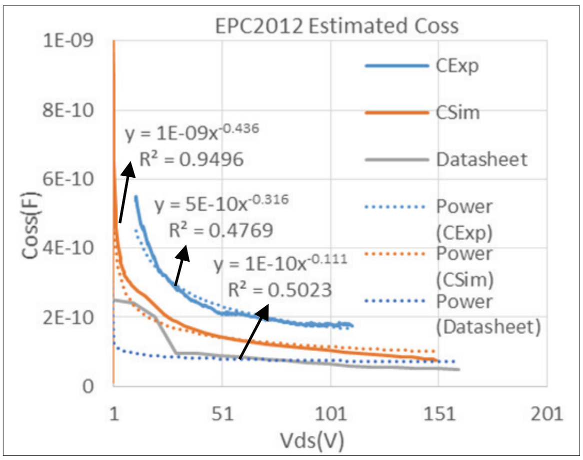

Fig. 9. Estimated output capacitance (EPC2012).

curves. These curves appear as dotted lines in Fig. 6 and Fig. 9. They are prefixed with the word "Power" because a power regression of the form indicated in Equ. (5) is used for case studies with a correlation factor that is higher than 0.9 in most cases. Even for lower correlation factors the graphs visually correlate well over a wide range of values for the drain-source voltages. The coefficients, *a* and *b*, translate into the value of the capacitance when the switch voltage is zero (C_{Init}) and the power to which the voltage (V_{ds}) is raised as shown in Equ. (6).

$$y = a * x^b \tag{5}$$

$$C_{New} = C_{Previous} * V_{ds}^b \tag{6}$$

D. Use of Approximated Output Capacitance to Determine Transient Response through Simulation

LT Spice is used to check how the transient response obtained with the calculated values of the output capacitance correspond to the original response. The original equivalent circuit shown in Fig. 4(a) was reduced to a simple RC-circuit subject to a voltage step function as shown in Fig. 4(b) as previously discussed. This assumption is made since the output capacitance charges through the load resistor when as the switch opens. In simulations, the rise time of the step function should be made as small as possible to minimize the effect on the transient response of the circuit. The effect of the drain-source resistance R_{DS}, which effectively changes from the value R_{DSon} to a very high value in parallel with C_{oss}, also has little effect if the load resistance is high and is omitted from the equivalent circuit. In LTSpice®, non-linear capacitance is in the form of Q=C*x, where C is the initial capacitor value and LTSpice® handles *x* as capacitor voltage during the simulation.

Fig. 4(c) shows the circuit diagram used to simulate the switching circuit of a GaN-FET into a resistive load. GaN-FET models for LTSpice®, provided by EPC (Efficient Power Conversion Corporation®), are used in these simulations. Upon investigation, the models provided by EPC turn out to be a lot more comprehensive than most of the models for MOSFETs and the other devices included in the LTSpice® libraries.

Simulated transient responses are shown in Fig. 7 for the EPC2010 device and later in Fig. 10 for the EPC2012 device. A very good correlation can be seen between the true experimental transients (Exp) and the simulated transients resulting from the estimated output capacitance (RC-Exp) for each of the devices.

The overall results will now be discussed with a specific emphasis on the estimate output capacitance and the loss contribution of this capacitance discharging into the device on-resistance during a switch-on event.

E. Comparison of Loss Estimations

The following two methods were used to calculate the estimated loss contribution of the output capacitance during the switch-on of a device where the energy stored in the output capacitance dissipates in the device channel.

First, the method discussed in [10] is employed and energy is stored in the output capacitance calculated for a few different values of drain-source voltage using Equ. (5). These values are used as a reference.

$$E = f * C_{osseff} * V^2 \tag{5}$$

Secondly, charge-voltage (q-v) curves for the devices are drawn from the capacitance-voltage curves obtained so far in this work and the stored energy calculated using numerical integration based on equation (6).

$$W = v * \int dq \tag{6}$$

Furthermore, the power dissipation is calculated using the pulse width and the repetition frequency of power pulses. The loss contribution of the output capacitance at 1MHz is plotted in Fig. 11 and Fig. 12 for the two devices.

A last thought on the output capacitance discharge current is that it is not possible to measure it directly [17]. However,

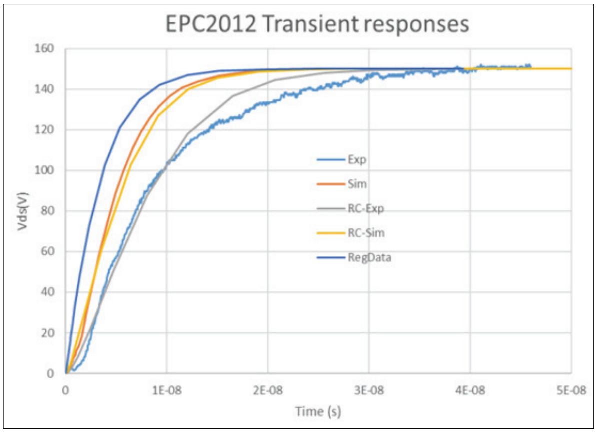

Fig. 10. Resulting transients using an estimated C_{oss} - EPC2012.

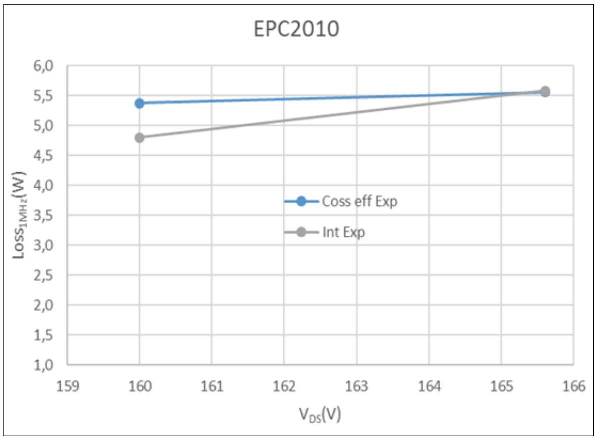

Fig. 11. Loss contribution values due to the output capacitance for an EPC2010 calculated using the effective output capacitance (C_{oss}-eff) and through the integration of the q-v curve obtained from experimental results (Int Exp).

indirect measurement methods may exist and should be investigated.

The full details of this method, including loss estimations obtained through simulation and using datasheet values, will be published in a follow-up paper.

IV. Discussion of Results

The results for an EPC2010 device are displayed and discussed in this section. Similar results were obtained for an EPC2012 device to determine the level of repeatability. The EPC2012 trends differ from the EPC2010 in some areas and references are made to some of the phenomena observed.

No attempt was made to filter the data. Oscilloscope noise in the experimental transient data however results in erratic behavior of the capacitance values at the extreme lower and higher ends of the voltage values. This makes the omissions of small ranges of data necessary with the determination of the power regressions in only two out of the six data sets. The degree of correlation between the original experimental data (Exp) and the data obtained from the simulation (RC-Exp) in Fig. 7 and Fig. 10 is particularly important because it gives an indication of how well the large signal capacitance is estimated when compared to the measured values of the respective devices.

Similarly, the transient responses for the EPC2012 device are shown in Fig. 8 and the capacitance graphs are shown in Fig. 9.

The estimated output capacitances for both devices exceed the datasheet values for all of the values of the drain-source voltage. As expected, the capacitance values for the EPC2010 are higher than the EPC2012 capacitance values due to the higher current rating calls for an increased device area.

As far as the expected and simulated values are concerned, the values for the capacitance estimated from the simulation (CSim in Fig. 6) for the EPC2010 are higher than the values estimated from the experimental data for voltages up to 70V. However, for the EPC2012 device, the values obtained from experimental values are higher for all of the voltages as can be seen in Fig. 9. It should be noted that the peak test current for the devices are both the same. However, the EPC2010 device has a higher current rating which may influence the results.

Although the correlation factor for the power regressions of two of the EPC2012 device curves were rather low, the curves visually display a reasonable correlation. The curve fitted to the datasheet values is obscured by high values of the capacitance at lower voltages. The low correlation of the curve fitted to the capacitance values obtained from the simulated switching transient may be due to a deviation in the lower voltage range.

The experimental transient response and the response generated using estimated values of the capacitance are very similar for the EPC2010 device. However, some errors occur between the corresponding curves for the EPC2012 device. Upon a close inspection of the CExp and Power (CExp) curves it can be seen that although the correlation factor for the entire curve is high, the two curves start to diverge in the region of 100V and higher.

This is also the region in which the two transient responses differ. This may be attributed to the noise present in the original experimental transient response (Exp).

Some error should be expected due to the numerical methods involved in the proposed method. The step size in the voltage and the associated time step size are limited by the number of data points of the drain-source voltage gathered during initial experiments.

It is also not clear how the output capacitance is represented in the LTSpice® model provided by the device manufacturer. There are indications that an equation is used to generate the values of the non-linear capacitance as a function of the drain-source voltage. This equation is likely derived from the datasheet values, which are first of all small

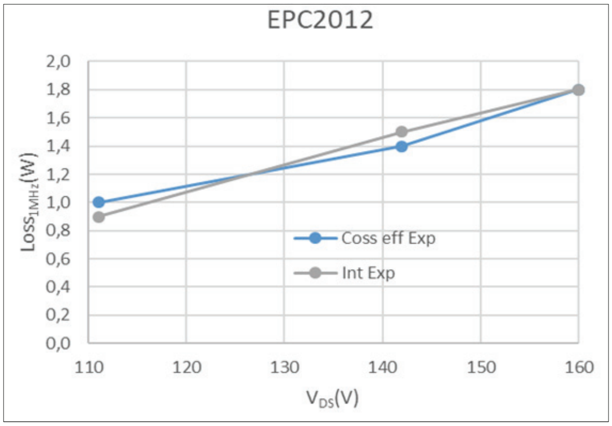

Fig. 12. Output capacitance loss contribution predicted for an EPC2012 calculated using the effective output capacitance (C_{oss}-eff) and through integration of the q-v curve obtained from experimental results (Int Exp).

signal values. Furthermore, it can be seen from the nature of these graphs that some error can be expected when a curve is fitted through it.

The loss contribution of the output capacitance is calculated using the C_{oss} - effective method [10] and it is also shown in Fig. 11 and Fig. 12 for a few different values for the two different devices. It can be seen that the largest error amongst the sampled values is an 11% underestimation for the EPC2010 device and a 7% underestimation for the EPC2012 device when using the method proposed in [10] as a reference. The fact that there is such a good correlation means that the new proposed method for estimating the output capacitance of devices is fairly accurate.

V. Conclusions and Future Work

The steps of the proposed method are summarized briefly for the convenience of the reader.

- Switch-off voltage transients for the device, switching into a known resistive load, should be available with a minimum of noise or oscillatory effects caused by the measurement circuit. These measurements should be done with current levels close to the operating conditions of the device in an actual application.
- Use Equ. (4) to calculate the discrete values of C_{oss}.
- Fit a curve through the discrete values of C_{oss} using Equ. (5) and Equ. (6). Microsoft EXCEL® may be used for convenience.
- Simulation software, capable of handling non-linear capacitance values, can be used to apply a voltage step to a circuit similar to Fig. 1(b). The capacitor voltage resulting from the simulation represents the transient response of a switch during switch-off.
- Compare the simulated response to the original transient obtained from the experiment. Close correlation between these two curves shows how well the capacitance as a function of the drain-source voltage is estimated under large signal conditions.
- Data-sheet values may be handled in the same way to obtain small-signal transients and they can be used for comparison.

Small errors occur between the transient responses predicted for the non-linear capacitor as shown in Fig. 2, Fig. 7 and Fig. 10.

The results show that non-linear output capacitance as a function of an increased voltage is higher than the datasheet values. The estimated values of the capacitance are quite accurate since the transient responses generated using them correlate well with the original measured transient responses. These transient responses show the same small error experienced in Fig. 2 and the cause of this error needs to be found if deemed necessary. A different simulation method is used in the process of generating new transient responses leading to more confidence in the results.

An attempt was made to show the hysteresis in the output capacitance using a modified equivalent circuit. However, this proved to be very complicated since the non-linear nature of r_{DS}, a function of V_{DS}, has to be considered.

Results obtained with the proposed method should be compared using the method proposed in [13] to determine how the obtained losses compare to those for different operating conditions.

However, the worst-case losses may be calculated assuming that C_{oss} completely discharges and dissipates in R_{DS}.

The method using the effective output capacitance to calculate the switching losses in [13] should also be compared with the results obtained in this work.

Experimental work should also be carried out with reverse biased diodes. This method should be applicable. However, reverse recovery effects may influence the results.

References

[1] M. Liang, T. Q. Zheng, and Y. Li, "An improved analytical model for predicting the switching performance of SiC MOSFETs," *J. Power Electron.*, Vol. 16, No. 1, pp.374-387, Jan. 2016.

[2] J. B. Fedison, M. Fornage, M. J. Harrison, and D. R. Zimmanck, "Coss related energy loss in power MOSFETs used in zero-voltage-switched applications," in *Proc. IEEE Power Electronics Conference and Exposition*, pp. 150-156, 2014.

[3] Y. Li, T. Q. Zheng, Y. Zhang, M. Cui, Y. Han, and W. Dou, "Loss analysis and soft-switching behavior of flyback-forward high gain DC/DC converters with a GaN FET," *J. Power Electron.*, Vol. 16, No. 1, pp.84-92, Jan. 2016.

[4] N. Z. Yahaya, M. B. K. Raethar, and M. Awan, "Review on gallium nitride HEMT device technology for high

frequency converter applications," *J. Power Electron*., Vol. 9, No. 1, pp. 36-42 , Jan. 2009.

[5] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. N. Pilawa-Podgurski, A. Sagneri, and C. R. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *Proc. Applied Power Electronics Conference and Exposition*, pp. 1-14, 2009.

[6] A. D. Sagneri, D. I. Anderson, and D. J. Perreault, "Optimization for integrated transistors for very high frequency DC-DC converters," *IEEE Trans. Power Electron.*, Vol. 28, No. 7, pp. 3614-3626, Jul. 2013.

[7] J. M. Rivas, D. Jackson, O. Leitermann, A. D. Sagneri, Y. Han, and D. J. Perreault, "Design considerations for very high frequency DC-DC converters," in *Proc. Power Electronics Specialists Conference*, PESC '06, pp. 1-11, 2006.

[8] M. Madsen, A. Knott, and M. A. E. Andersen, "Low power very high frequency switch-mode power supply with 50 V input and 5V output", *IEEE Trans. Power Electron.*, Vol. 29, No. 12, Dec. 2014.

[9] H. Sekiya, R. Miyahara, and M. K. Kazimierczuk, "Design of class-DE amplifier with linear and nonlinear shunt capacitances for 25 % Duty Ratio," in *Proc. IEEE International Symposium on Circuits and Systems*, pp. 2870-2873, 2009.

[10] International Rectifier Application Note (AN-1001A), "More Realistic characterization of power mosfet output capacitance coss," [Online]. Available: www.irf.com/technical-info/appnotes/an-1001.pdf

[11] D. Murthy and M. K. Kazimierczuk, "Performance evaluation of flyback converter," in *Proc. Electrical Insulation Conference and Electrical Manufacturing Expo*, pp. 408-416, 2005.

[12] Y. Cui, W. Zhang, L. M. Tolbert, D. J. Costinett. F. Wang, and B. J. Blalock, "Efficiency impact of MOSFET output junction capacitance on a high step down ratio phase shift full bridge DC/DC converter," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 2083-2089, 2015.

[13] J. B. Fedison and M. J. Harrison, "Coss hysteresis in advanced superjunction MOSFETs," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 247-252, 2016.

[14] A. J. L. Joannou, "A study of switching transients of gallium-nitride power field effect transistors in a defined electromagnetic environment," Thesis, University of Johannesburg, Nov. 2015.

[15] A. J. L. Joannou, D. C. Pentz, J. D. van Wyk, and A. S. de Beer, "An experimental study of switching GaN FETs in a coaxial transmission line," in *Proceeding of EPE'14-ECCE Europe*, pp. 1-9, 2014.

[16] G. Zulauf, W. Liang, K. Surakitbovorn, and J. Rivas-Davila, "Output capacitance losses in 600 V GaN power semiconductors with large voltage swings at high- and very-high-frequencies," in *Proc. IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA),* pp. 352-359, 2017.

[17] D. N. Pattanayak and O. G. Tornblad, "Large-signal and small-signal output capacitances of super junction MOSFETs," in *Proc. IEEE 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD),* pp. 229-232, 2013.

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