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Three-phase Three-level Boost-type Front-end PFC Rectifier for Improving Power Quality at Input AC Mains of Telecom Loads

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Abstract

A three-phase, three-switch, and three-level boost-type PWM rectifier (Vienna rectifier) is proposed as an active front-end power factor correction (PFC) rectifier for telecom loads. The proposed active front-end PFC rectifier system is modeled by the switching cycle average model. The relation between duty ratios and DC link capacitor voltages is derived in terms of the system input currents. Furthermore, the feasible switching states are identified and applied to the proposed system to reduce the switching stress and DC ripples. A detailed equivalent circuit analysis of the proposed front-end PFC rectifier is conducted, and its performance is verified through simulations in MATLAB. Simulation results are verified using an experimental setup of an active front-end PFC rectifier that was developed in the laboratory. Simulation and experimental results demonstrate the improved power quality parameters that are in accordance with the IEEE and IEC standards.

Key words: Average model, Front-end PFC rectifiers, Power quality, Switched mode telecom power supplies, Three-switch, Total harmonic distortion

I. INTRODUCTION

In India, 82% of the urban population and 18% of the rural population are dependent on mobile devices and the internet. In addition, the subscriber count for various services, such as fixed line, wireless, and broadband services, is rapidly increasing. This growing user base, along with the benefits given by the government, such as an auction of 3G and 4G spectra, is fueling large-scale hiring in the telecom and allied service sectors. As a result of this increasing importance of the telecom sector, the power supply to telecom loads has become crucial. Different power supply designing techniques have been discussed in [1]. These techniques should meet the power quality parameters specified under the IEEE-519 and IEC-61000-3-2 standards [2], [3]. The improved power quality converters used in switched mode power supplies for telecom applications have been discussed in [4], [5]. For low power levels of less than 5 kW, single-phase power quality converters have been mostly accepted. As for high power levels, three-phase power quality converters are generally adopted. Telecom systems require high-current low-voltage rectifiers. The power ratings of these rectifiers vary from tens of kW to hundreds of MW. The conventional front-end high-power diode bridge rectifier (DBR) with a capacitive DC link voltage results in main voltage and current distortion, which in turn leads to power quality problems. One of the most popular methods for improving power quality is the use of multi-pulse converter-based front-end AC–DC converter systems [6]-[10]. In addition, active current injection techniques are commonly used in low and medium power applications to draw near sinusoidal currents from the utility, along with multi-pulse transformers [10]-[13]. The advancement of multi-pulse techniques has led to the betterment of input power quality. The main issue with these techniques is the increased magnetic

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rating, weight, and volume. An active front-end converter is proposed in the present study to overcome the disadvantages of front-end multi-pulse converters. The proposed active front-end converter is an improvement of power factor correction (PFC) rectifiers due to its high efficiency, high reliability, and suitable semiconductor device availability.

This study is organized as follows. Section II outlines existing DBR-fed telecom power systems and the proposed front-end PFC rectifier in detail. Section III describes an average model of the proposed rectifier, including the DC link capacitor design procedure. Section IV presents modulation and control techniques. Section V discusses the simulation and experimental results. Finally, Section VI provides the conclusions.

II. Configuration of Proposed Front-End PFC Rectifier

Fig. 1 shows a schematic diagram of a telecom system using an IGBT-based DC–DC converter with a six-pulse conventional DBR at the front end. A filter (L_f, C_f) placed on the DC link is used to filter out high frequency components. A high frequency transformer (HFT) at the output of the DC–DC converter provides isolation between the primary and secondary windings. The balanced DC link current at the output side is provided by the secondary series connection of the HFT. In addition, the output side diode rectifier is connected in a center-tapped fashion to reduce diode conduction losses. For a conventional six-pulse rectifier, the input and output power quality indices deviate from the IEEE and IEC standards. In addition, the front-end six-pulse AC–DC rectifier is fed from a three-phase isolated star-delta transformer, thereby resulting in an increased magnetic rating of 210% of the load rating. An appropriate active front-end PFC rectifier for power quality improvement in telecom power systems, which replaces the three-phase DBR unit in Fig. 1, is proposed in this study to overcome the disadvantages associated with a front-end DBR.

Fig. 2 shows the proposed active front-end PFC rectifier for telecom power supply. The front end consists of an input side six-pulse conventional rectifier, which is followed by a bidirectional three-legged switching circuit. The bidirectional three-legged switching circuit is connected between the conventional front-end six-pulse DBR and the center point of DC link capacitors. The DC link voltage of high voltage magnitude results from the proposed front-end PFC rectifier, which is thus unsuitable for telecom applications that require a low voltage and high current. Hence, a back-end DC–DC converter is required to convert the high voltage to a low one. This study analyzes only the front-end PFC converter used for power quality improvement. The technical details of the back-end DC–DC converter for telecommunication applications are discussed in [14].

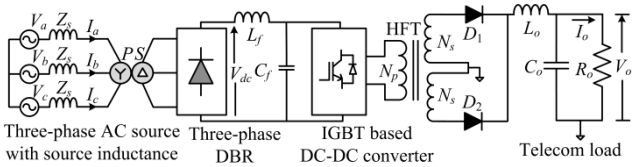


Fig. 1. Schematic diagram of a six-pulse AC–DC converter-fed telecom system.

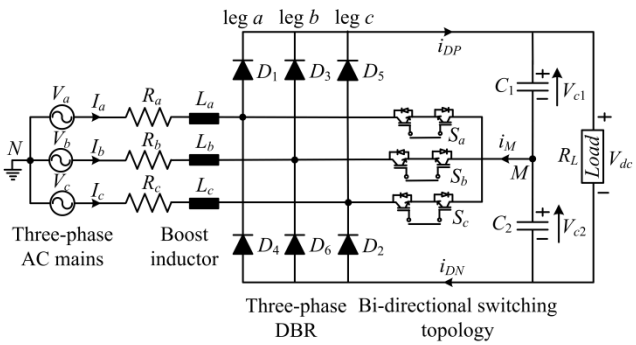


Fig. 2. Schematic diagram of the proposed front-end PFC rectifier.

The input voltage generation of the proposed active front-end PFC rectifier depends on the input inductance value and phase current sign. Three-level voltage is produced at the input side by the six-pulse conventional DBR and bidirectional switching topology. Hence, proposed topology is also called a three-level converter. The upper positive and lower negative voltage is produced with respect to the center point (M), to which the output side of the bidirectional switching circuit is connected. The blocking voltage of the switches is only half of the line–line voltage due to the three-level input voltage. The fundamental current ripple in the input side is reduced by the increased number of levels. Therefore, the size of the input boost inductance is reduced. This condition results in low switching losses and minimal electromagnetic interference. The output DC link voltage V_{dc} of the proposed system has minimum and maximum voltage range values of $\sqrt{2}\ V_N$,*rms* and $2\sqrt{2}\ V_N$,*rms*, respectively. A high value of DC output voltage is obtained with low input inductance value. During a single phase outage, the topology operates under a reduced power and maintains a sinusoidal input current in the remaining phases [15].

III. Average Model of the Switching Cycle of the Proposed PFC Rectifier

The average model of the switching cycle of the proposed three-phase three-level boost-type [16, 17] front-end PFC rectifier is shown in Fig. 3. The phase voltages [18] are expressed as follows by applying a KVL at the nodes:

$$\begin{aligned} \overline{V}aN &= \overline{V}a - (R_a + j\omega L_a)\overline{I}a, \\ \overline{V}bN &= \overline{V}b - (R_b + j\omega L_b)\overline{I}b, \\ \overline{V}cN &= \overline{V}c - (R_c + j\omega L_c)\overline{I}c, \end{aligned} \tag{1}$$

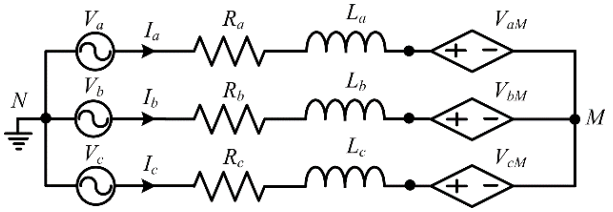


Fig. 3. Average model of switching cycle of a converter.

where L_a, L_b, L_c and R_a, R_b, R_c are the three-phase boost input inductance and line resistance of the proposed system, respectively. $\overline{V}aN$, $\overline{V}bN$, $\overline{V}cN$ are the input phase voltages; $\overline{V}a$, $\overline{V}b$, $\overline{V}c$ are the voltages available at the converter phase leg; and ω is the angular frequency of the proposed system. The resistance and inductance can be eliminated in the analysis because their values are extremely small relative to the system frequency. Therefore, Eq. (1) can be rewritten as follows:

$$\overline{V}aN = \overline{V_a}; \overline{V}bN = \overline{V_b}; \text{ and } \overline{V}cN = \overline{V_c}. \tag{2}$$

The 120°-displaced three-phase input voltage can be written as

$$\overline{V}a = V_m \sin\omega t; \overline{V}b = V_m \sin(\omega t + 120^O); \text{ and } \overline{V}c = V_m \sin(\omega t + 240^O). \tag{3}$$

This equation leads to

$$\overline{V_a} + \overline{V_b} + \overline{V_c} = 0 \Rightarrow \overline{V}aN + \overline{V}bN + \overline{V}cN = 0. \tag{4}$$

The cyclic average voltage is written by applying a KVL at the converter input terminal.

$$\begin{aligned} V_a &= V_{aM} + V_{MN}, \\ V_b &= V_{bM} + V_{MN}, \\ V_c &= V_{cM} + V_{MN}. \end{aligned} \tag{5}$$

The following relation can be obtained by Eqs. (4) and (5):

$$V_{MN} = -\frac{1}{3}(V_{aM} + V_{bM} + V_{cM}). \tag{6}$$

The resultant three-phase equation is acquired by substituting Eqs. (3) and (5) into Eq. (6).

$$\begin{aligned} V_a &= V_{aM} - \frac{1}{3}(V_{aM} + V_{bM} + V_{cM}), \\ V_b &= V_{bM} - \frac{1}{3}(V_{aM} + V_{bM} + V_{cM}), \\ V_c &= V_{cM} - \frac{1}{3}(V_{aM} + V_{bM} + V_{cM}). \end{aligned} \tag{7}$$

Eq. (7) is simplified in matrix form as

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & \frac{-1}{3} & \frac{-1}{3} \\ \frac{-1}{3} & \frac{2}{3} & \frac{-1}{3} \\ \frac{-1}{3} & \frac{-1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} V_{aM} \\ V_{bM} \\ V_{cM} \end{bmatrix}. \tag{8}$$

The cyclic switching voltages for all three phases under continuous conduction mode are as follows:

$$\begin{aligned} V_{aM} &= \begin{cases} (1-D_a) & \text{if } I_a \geq 0 \\ -(1-D_a) & \text{if } I_a < 0 \end{cases}, \\ V_{bM} &= \begin{cases} (1-D_b) & \text{if } I_b \geq 0 \\ -(1-D_b) & \text{if } I_b < 0 \end{cases}, \\ V_{cM} &= \begin{cases} (1-D_c) & \text{if } I_c \geq 0 \\ -(1-D_c) & \text{if } I_c \geq 0 \end{cases}, \end{aligned} \tag{9}$$

where D_a, D_b, D_c are the duty ratios of the switches S_a, S_b, S_c, respectively. The duty ratio D is given by

$$D_{a,b,c} = \begin{cases} 0 & \text{if } S_{a,b,c} \text{ is turned off} \\ 1 & \text{if } S_{a,b,c} \text{ is turned on} \end{cases}. \tag{10}$$

The output capacitors can be expressed by Eq. (11) as follows:

$$\begin{aligned} C_1 \frac{dV_{c1}}{dt} &= i_{c1} - \frac{V_{dc}}{R_L}, \\ C_2 \frac{dV_{c2}}{dt} &= i_{c2} - \frac{V_{dc}}{R_L}, \end{aligned} \tag{11}$$

where i_{c1} and i_{c2} are the currents passing through the upper and lower capacitors, respectively. The output DC voltage is the sum of the upper and lower capacitor voltages, and ΔV is the unbalance in the DC link voltages. These voltages can be expressed as follows:

$$V_{dc} = V_{c1} + V_{c2}; \Delta V = V_{c1} - V_{c2}. \tag{12}$$

The average voltage is expressed by considering the unbalance in the output capacitor voltage and duty ratio.

$$\begin{aligned} V_{aM} &= \frac{V_{dc}}{2}\left[sign(I_a) + \frac{\Delta V}{V_{dc}} \right](1-D_a), \\ V_{bM} &= \frac{V_{dc}}{2}\left[sign(I_b) + \frac{\Delta V}{V_{dc}} \right](1-D_b), \\ V_{cM} &= \frac{V_{dc}}{2}\left[sign(I_c) + \frac{\Delta V}{V_{dc}} \right](1-D_c), \end{aligned} \tag{13}$$

where $sign(I_a)$, $sign(I_b)$, $sign(I_c)$ depend on the polarity of the inductor current.

$$sign(I_a) = \begin{cases} 1 & \text{if } I_a \geq 0 \\ -1 & \text{if } I_a < 0 \end{cases} \tag{14}$$

$\Delta V/V_{dc}$ is neglected because ΔV is particularly small in comparison with V_{dc}. Eq. (13) can be rewritten as

$$\begin{aligned} V_{aM} &= \frac{V_{dc}}{2}\left[sign(I_a) \right](1-D_a), \\ V_{bM} &= \frac{V_{dc}}{2}\left[sign(I_b) \right](1-D_b), \\ V_{cM} &= \frac{V_{dc}}{2}\left[sign(I_c) \right](1-D_c). \end{aligned} \tag{15}$$

Eq. (15) is substituted into Eq. (8). The final voltage expression in terms of the duty ratio is given in matrix form as follows:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{V_{dc}}{2} \begin{bmatrix} \frac{2}{3} & \frac{-1}{3} & \frac{-1}{3} \\ \frac{-1}{3} & \frac{2}{3} & \frac{-1}{3} \\ \frac{-1}{3} & \frac{-1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} (1-D_a)sign(I_a) \\ (1-D_b)sign(I_b) \\ (1-D_c)sign(I_c) \end{bmatrix}. \quad (16)$$

The generalized average duty ratio expression is given by considering the diode conduction state as

$$D_{a,b,c} = (1-T_{a,b,c})sign(I_{a,b,c}) = D'_{a,b,c} + D_O, \quad (17)$$

where $T_{a,b,c}$ is the average switch on time for $S_{a,b,c}$ and $D'_{a,b,c}$ and D_o are the sinusoidal and zero-sequence components, respectively. In a three-phase system, the sum of the phase current is given by

$$I_a + I_b + I_c = 0. \quad (18)$$

Therefore, the phase voltage expression becomes

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{V_{dc}}{2} \begin{bmatrix} \frac{2}{3} & \frac{-1}{3} & \frac{-1}{3} \\ \frac{-1}{3} & \frac{2}{3} & \frac{-1}{3} \\ \frac{-1}{3} & \frac{-1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} D'_a \\ D'_b \\ D'_c \end{bmatrix}. \quad (19)$$

Through KCL, the diode current is given in Eq. (20), where i_{DP} and i_{DN} are the sums of the positive and negative side diode currents, respectively. The positive and negative side diodes are denoted as D_1, D_3, D_5 and D_4, D_6, D_2, respectively.

$$\begin{aligned} i_{DP} &= i_{a,D1} + i_{b,D3} + i_{c,D5}, \\ i_{DN} &= i_{a,D4} + i_{b,D6} + i_{c,D2}. \end{aligned} \quad (20)$$

The sums of the positive and negative side currents are given in terms of the duty ratio of the converter.

$$i_{DP;a,b,c} + i_{DN;\,a,b,c} = D_{a,b,c} i_{a,b,c}. \quad (21)$$

The average DC link currents (upper and lower diodes) in terms of the duty ratio with corresponding phase currents are given by

$$i_{DP} + i_{DN} = D_a i_a + D_b i_b + D_c i_c. \quad (22)$$

The converter midpoint current is the difference between the lower and upper diode currents, and it is given by

$$i_M = i_{DN} - i_{DP}. \quad (23)$$

The cyclic average DC link current (upper or lower diodes) is obtained by the average of the input phase currents given by

$$\frac{|I_a| + |I_b| + |I_c|}{2}. \quad (24)$$

The 120°-displaced three-phase input phase currents can be written as

$$\overline{I_a} = I_m \sin\omega t; \overline{I_b} = I_m \sin(\omega t + 120^o); \overline{I_c} = I_m \sin(\omega t + 240°). \quad (25)$$

The average current through the diode is calculated by the expression in [10] as follows:

$$\frac{1}{T_s/6} \int_{-T_S/12}^{T_S/12} \mathrm{I_m} \cos(\omega t) dt = \frac{3}{\pi} \mathrm{I_m}. \quad (26)$$

The instantaneous DC output power is given by

$$P_{dc} = \frac{V_{dc}}{2}(i_a + i_b + i_c) = \frac{3}{2} V_m \mathrm{I_m}. \quad (27)$$

On the basis of Eqs. (3) and (25), the instantaneous AC power is given by

$$\begin{aligned} &P_{ac} = \overline{V}_{aN} \overline{I}_a + \overline{V}_{bN} \overline{I}_b + \overline{V}_{cN} \overline{I}_C, \\ &P_{ac} = V_m I_m \sin^2 \omega t + V_m I_m \sin^2(\omega t + 120^o) + V_m I_m \sin^2(\omega t + 240°), \\ &P_{ac} = \frac{3}{2} V_m \mathrm{I_m}. \end{aligned} \quad (28)$$

The input–output power balance is verified by Eqs. (27) and (28).

A. Design of DC Link Capacitor

The energy stored in the capacitor for half a cycle of the power ripple is given by Eq. (29).

$$W_C = \int_0^{\pi/2} p\, dt = \frac{P_o}{\omega}, \quad (29)$$

where ω is the angular frequency of the input power supply and P_o is the output power. The DC link capacitor charges and discharges power at twice the line frequency. Therefore, a DC link capacitor ripple with twice the line frequency is applied across the DC output. The charge in the capacitor is obtained by Eq. (30).

$$W_C = \frac{1}{2} C \left(V_{dc\max}^2 - V_{dc\min}^2 \right), \quad (30)$$

where V_{dcmax} and V_{dcmin} are the maximum and minimum allowable DC voltages at the output side, respectively. The ratings of the devices can be calculated from the allowable maximum and minimum voltages at the output side. The required capacitance of the DC link part is calculated by Eq. (31).

$$C \geq \frac{2P_o}{\omega \left(V_{dc\max}^2 - V_{dc\min}^2 \right)}. \quad (31)$$

On the basis of Eq. (31), the DC link capacitor is calculated from the angular line frequency, allowable maximum and minimum voltage ripples of the DC link voltage, and output power. The ripple in the DC link side is calculated by Eq. (32).

$$V_{ripple}=V_{dc\max}-V_{dc\min}. \quad (32)$$

The capacitance value is entirely dependent on the voltage ripple. In practice, the allowable voltage ripple is 1%–5% of the output voltage level. A high voltage ripple indicates a low capacitance requirement, and vice versa.

IV. Modulation and Control Techniques

A per phase equivalent circuit of the proposed rectifier is shown in Fig. 4(a). In Fig. 4(b), switch S_a is closed, and the positive cycle of the phase voltage V_a is applied to the leg *a*. During this positive cycle, the positive upper diode conducts and thereby charges the upper capacitor to the positive peak of the applied voltage. The return path is formed through an anti-serial connected bidirectional switch, in which a switch and a switch anti-parallel diode conduct. During the negative cycle of the input phase voltage V_a, the negative lower diode conducts, and thus, the lower capacitor is charged to the negative peak of the applied voltage.

The current path is completed by an anti-serial connected bidirectional switch, as shown in Fig. 4(c). In both of the states, the capacitor is charged to $+V_{dc}/2$ and $-V_{dc}/2$. The possible combinations of switching states and their corresponding voltages/currents with respect to the midpoint *M* are given in Table I.

The input AC voltage arrangement mainly depends on the magnitude of the current phasors. In Fig. 5, for $I_a > 0$ and I_b, $I_c > 0$, the four switching state results are (011), (010), (000), and (100). Here, the positive and negative offset values lead to the increase and decrease of the on time of the switching state (100) relative to that of (011). The charging and discharging of the capacitor are decided by these switching states [19]-[23]. Fig. 6 shows the equivalent circuit with a resultant average current at the converter and the charging of the capacitors for the switching states (011), (010), (000), and (100). These four switching states have been applied to the switching pulse period $T_S/2$, thereby resulting in a minimum input current ripple [24]. The input current ripple is dependent on carrier frequency. A high carrier frequency equates to a low input current ripple [25, 26]. Furthermore, augmenting the carrier frequency results in increased switching losses in the switches. Thus, a tradeoff is made among the switching frequency, input current ripple, and switching loss [27]-[29].

The control technique for the proposed system to obtain the aforementioned switching states is shown in Fig. 7. Here, the voltage error V_{error} between the reference, V_{ref}, and the sensed V_{dc} DC output voltages is processed by a proportional and integral (PI) controller. Then, a three-phase input voltage magnitude of $V_{aN}/V_{bN}/V_{cN}$ and a phase displacement of 120° are multiplied with the PI controller output, and the resultant signal is $I_a/I_b/I_{c,ref}$.

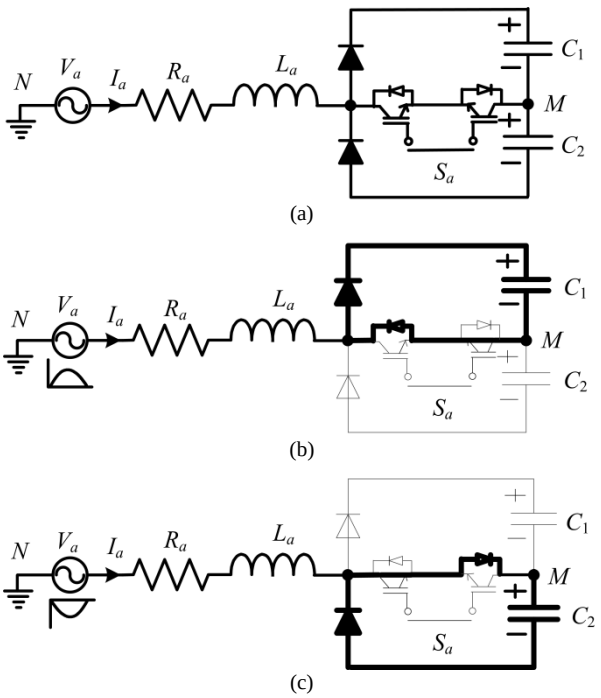


Fig. 4. A per phase equivalent circuit of the proposed rectifier. (a) Single phase equivalent circuit and its operating modes during: (b) Positive input cycles; (c) Negative input cycles.

TABLE I
Switching States and Corresponding Voltages/Currents with Respect to the Midpoint (*M*)

S_a	S_b	S_c	V_{aM}	V_{bM}	V_{cM}	i_M
0	0	0	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	0
0	0	1	$V_{dc}/2$	$-V_{dc}/2$	0	$-I_c$
0	1	0	$V_{dc}/2$	0	$-V_{dc}/2$	$-I_b$
0	1	1	$V_{dc}/2$	0	0	I_a
1	0	0	0	$-V_{dc}/2$	$-V_{dc}/2$	$-I_a$
1	0	1	0	$-V_{dc}/2$	0	I_b
1	1	0	0	0	$-V_{dc}/2$	I_c
1	1	1	0	0	0	0

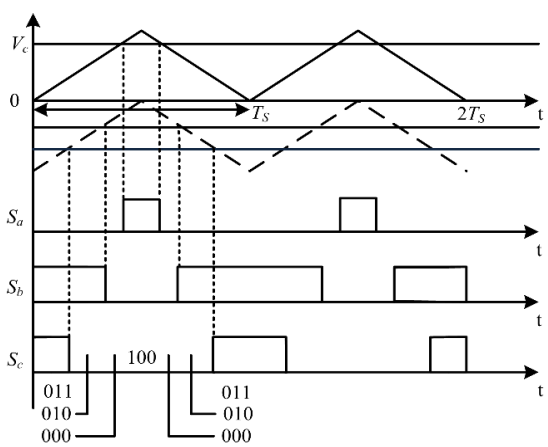


Fig. 5. Modulation scheme for the proposed front-end PFC rectifier.

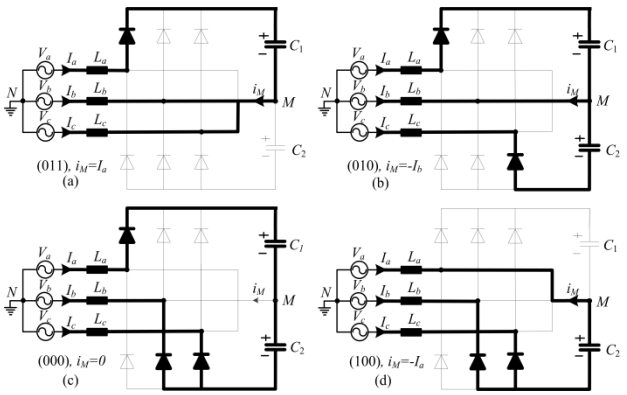


Fig. 6. Conduction states for the converter during switching states: (a) (011); (b) (010); (c) (000); (d) (100).

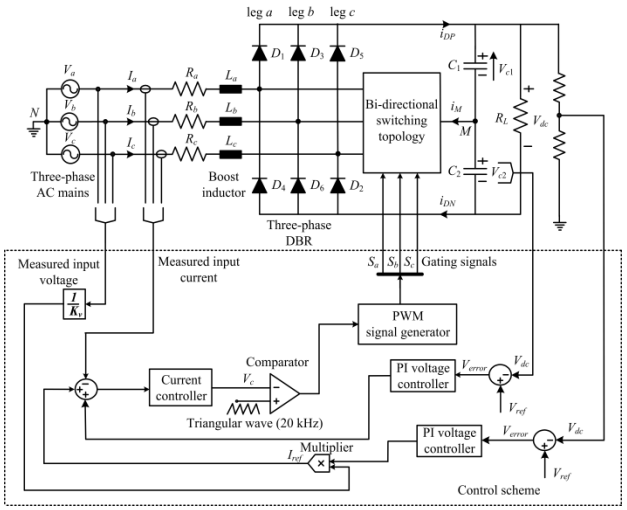


Fig. 7. Control scheme for the proposed front-end PFC rectifier.

The DC link voltage is balanced by considering either the upper or the lower capacitor voltage in the PI voltage controller loop. It also holds the output DC magnitude information. The sampled input current $I_a/I_b/I_c$ is analogized with the referral current signal and then processed by the current controller. A high frequency triangular wave of 20 kHz is compared with the current controller output to generate PWM pulses to the bidirectional switching topology. For the input, current $I_a > 0$, and I_b, $I_c < 0$. The resultant switching states are applied to the bidirectional switch through control logic. Any variations in the measured quantities are reflected in the duty ratios D_a, D_b, and D_c, which balance the DC link voltage and maintain the sinusoidal input current for all of the possible switching states.

V. Results and Discussion

A. Simulation Results

The proposed front-end PFC rectifier is modeled, designed, and validated in the MATLAB/SIMULINK environment.

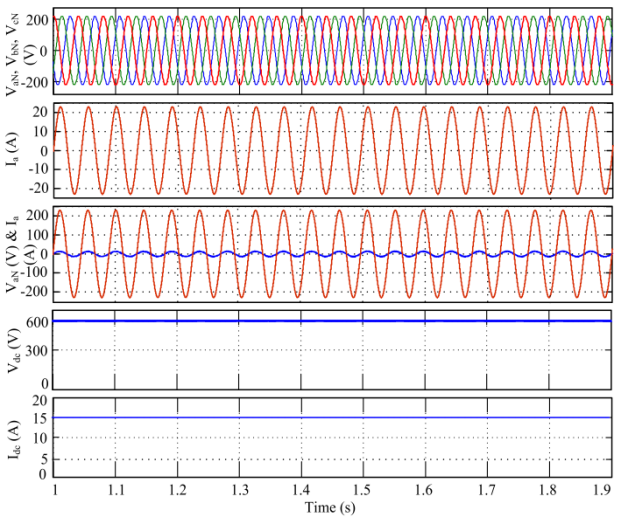


Fig. 8. Simulation results of the input phase voltage, input phase current, input voltage, input current, DC link voltage, and DC current for the proposed front-end PFC rectifier at the rated load condition.

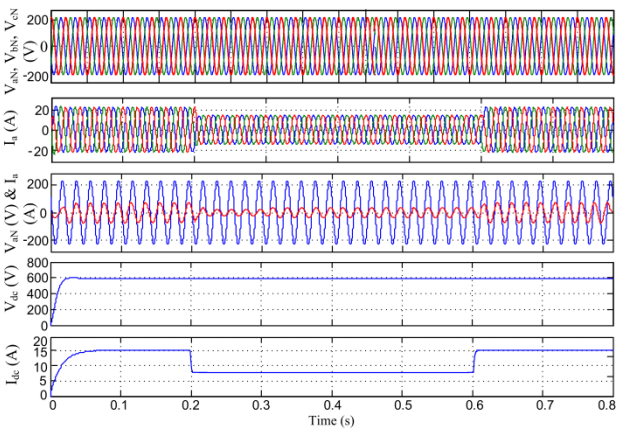
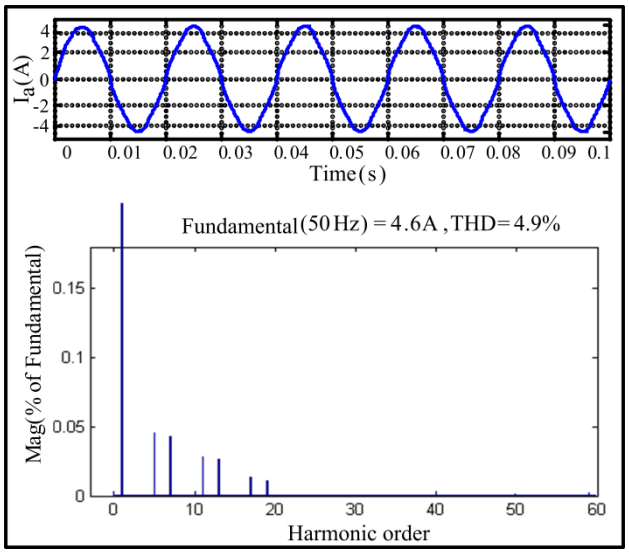
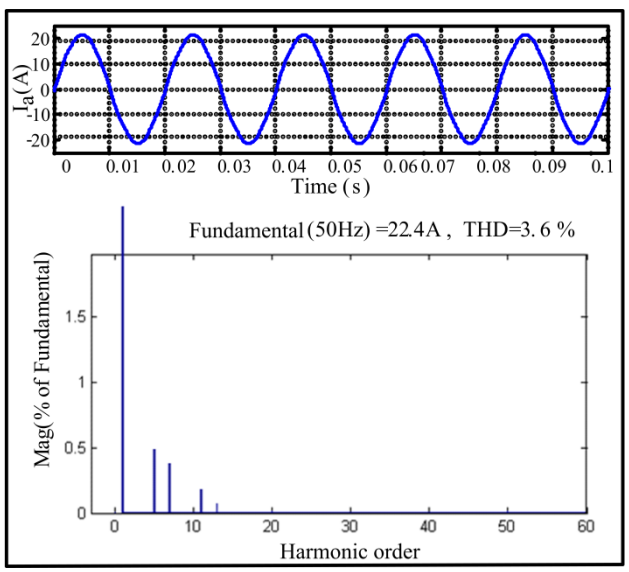


Fig. 9. Simulation results of the input phase voltage, input phase current, input voltage, input current, DC link voltage, and DC current for the proposed front-end PFC rectifier under load variations.

Figs. 8 and 9 show the input phase voltage, input phase current, input voltage, input current, DC link voltage, and DC current for the proposed front-end PFC rectifier at rated and varying load conditions. According to the simulation results, the input voltage and current are in phase with each other, thereby ensuring the consistency of the power factor (PF) operating condition. A waveform of the supply current, along with its harmonic spectrum, under full (100% of a full load) and light (20% of a full load) load conditions is shown in Figs. 10(a) and 10(b), respectively. The power quality indices obtained from the proposed rectifier at varying load conditions are summarized in Table II. The power quality parameters under varying load conditions are in accordance with the IEEE standards. According to the results, the elimination of the input current harmonics results in improved consistency in the total harmonic distortion (THD) and PF.



(a)



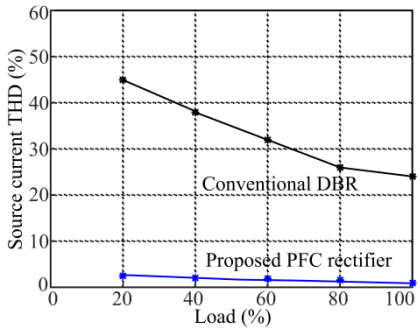
(b)

Fig. 10. Simulation results of the main input AC current (I_a) and its frequency spectrum for the proposed front-end PFC rectifier at: (a) Light load condition; (b) Full load condition.

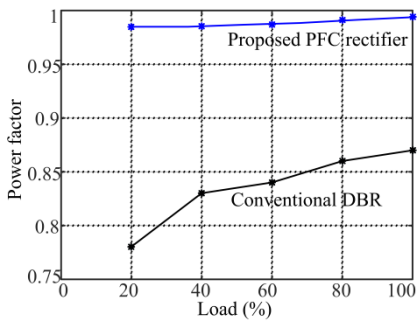
TABLE II
POWER QUALITY INDICES FOR THE PROPOSED FRONT-END PFC RECTIFIER UNDER VARYING LOAD CONDITIONS

Load (%)	v_{THD} (%)	i_{THD} (%)	DPF	DF	PF	Ripple Factor
20	1.2	4.9	0.9867	0.9981	0.9849	0.020
40	1.5	4.7	0.9883	0.9984	0.9868	0.012
60	1.8	4.5	0.9897	0.9987	0.9884	0.009
80	2.1	4.1	0.9919	0.9991	0.9913	0.008
100	2.4	3.6	0.9949	0.9989	0.9938	0.006

The performance of the proposed rectifier system is compared with that of a conventional six-pulse DBR. The results of the conventional six-pulse DBR-fed telecom system are from [30]. The simulated results are analyzed to study the



(a)



(b)

Fig. 11. Variation of the power quality indices with a load for an active three-phase, three-switch, and three-level boost-type PFC rectifier: (a) THD; (b) PF of the input current with a load.

effects of the load variations of the proposed PFC converter. Subpanel labels (a) and (b) of Fig. 11 show the effects of load variations on the THD and PF of the input current of the proposed system in comparison with that of the conventional DBR. According to the comparison results, the source current THD is below 5% and that the PF is kept almost consistent under varying load conditions.

B. Hardware Implementation

Digital control for the proposed rectifier is carried out using a fast digital processor (Altera Cyclone-IV-based FPGA controller). The FPGA controller board consists of an EP4CE30F484 processor and its associated on-chip peripherals. Figs. 12 and 13 show a schematic diagram of the hardware implementation and demonstrator of the proposed PFC rectifier. The following peripherals of the processor are used for the implementation.

1) A 16-channel, 12-bit analog-to-digital converter is used to sense the input and output voltage/current.

2) A 4-channel, 12-bit digital-to-bipolar analog converter is used to convert digital data into an analog signal, which is taken from the signals from the FPGA. The generated PWM pulses are given to the drivers of the IGBT of the front-end PFC rectifier.

A laboratory prototype for the 9 kW front-end PFC rectifier is developed, and the specifications are described in the Appendix. Hardware results are taken with reduced input voltage of 100 V. The test results are recorded with the Fluke

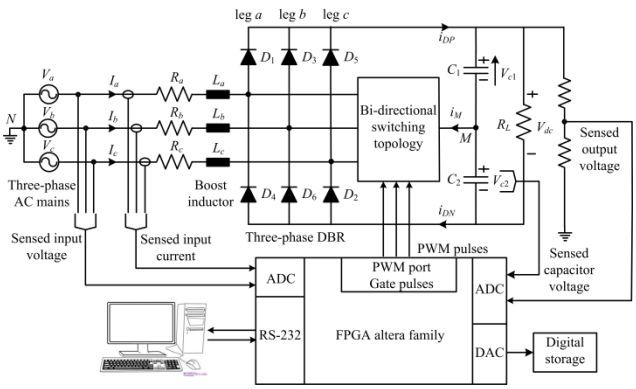


Fig. 12. Schematic diagram of the hardware implementation using an FPGA controller.

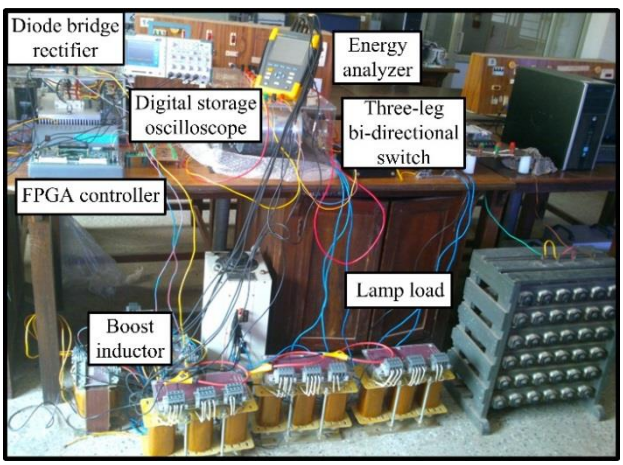
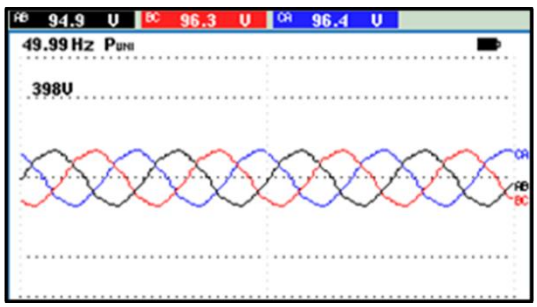


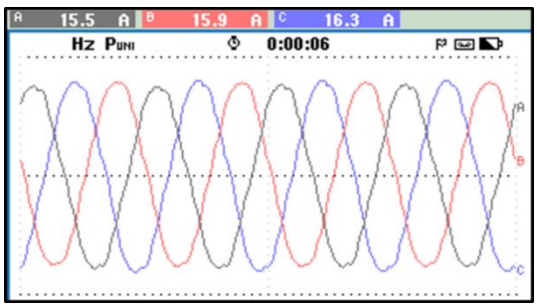
Fig. 13. Hardware demonstrator of the active three-phase, three-switch, and three-level boost-type PFC rectifier.

434-II energy analyzer shown in Fig. 14. An IGBT-based DBR is chosen for hardware realization. An SKM300GM12T4 switch that has a 40 A current rating is chosen for the bidirectional switching topology. The switching frequency of the proposed system can be considered as 20 kHz, which results in low input current THD and improved power quality parameters. Fig. 14 shows the steady-state test results obtained with the proposed rectifier. The voltage and current shown in Fig. 14(c) are in phase with each other. The frequency spectrum shows the corresponding THD under a reduced load rating. For the reduced and rated load conditions, the THD is in accordance with the IEEE standards.

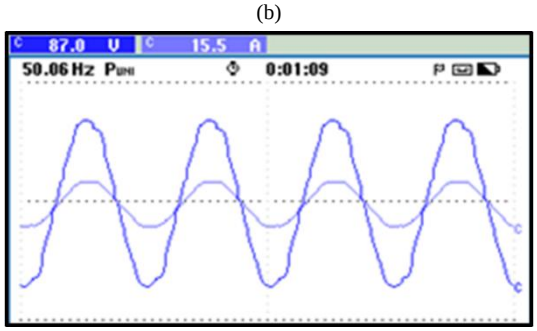
The performance of the proposed PFC rectifier is also validated by applying a sudden variation in the load. The corresponding test results are shown in Fig. 15. Fig. 15(a) shows the three-phase input currents with DC link voltage. During a load change, a small deviation in the DC link voltage with respect to the reference voltage is observed. The DC link voltage then returns to its original value without any overshoot. In addition, the input phase voltage and current are in phase with each other, thereby ensuring the consistency of the PF operation, as shown in Fig. 15(b). The THD of the



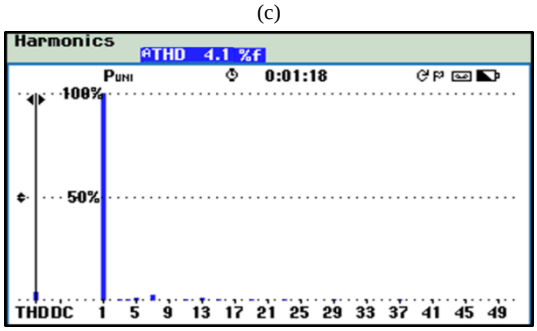
(a)



(b)



(c)



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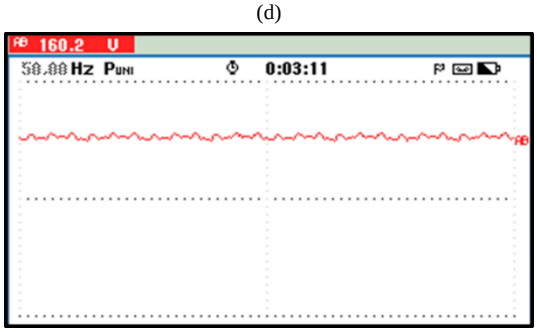
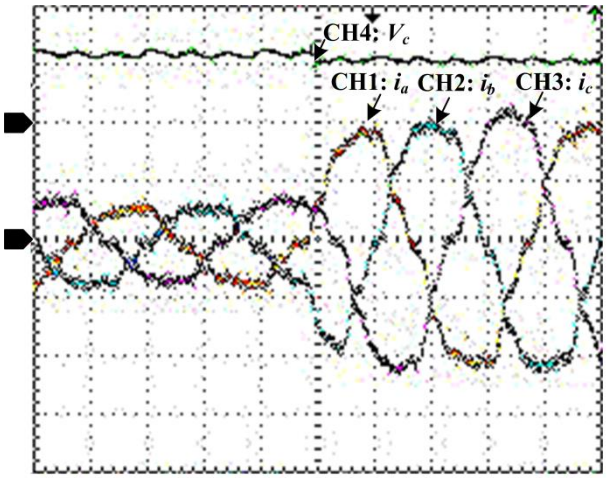
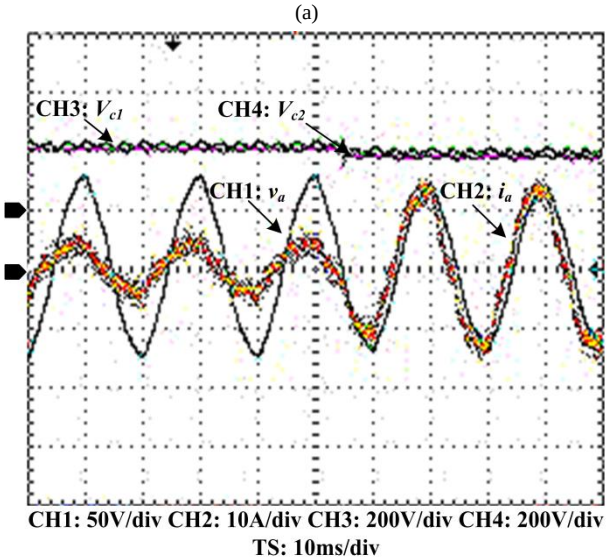


(e)

Fig. 14. Hardware results of: (a) Input line-to-line AC voltage (V_{L-L}); (b) Input phase current (I_a); (c) Input voltage and current; (d) Input current frequency spectrum; (e) DC link voltage for the proposed front-end PFC rectifier at light load conditions.



(a)



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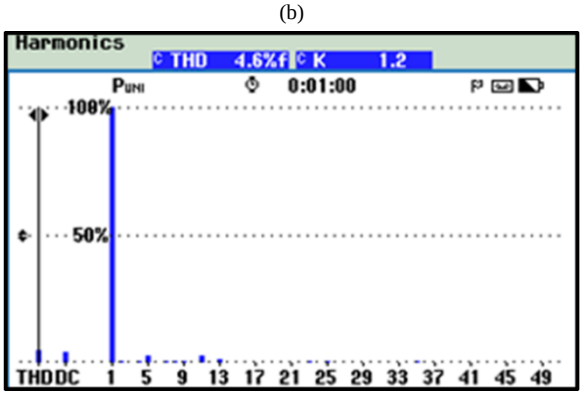

(c)

Fig. 15. Hardware results of: (a) Three-phase input currents with DC link voltage; (b) Input phase voltage and phase current with DC link voltage; (c) Input current frequency spectrum for the proposed front-end PFC rectifier under dynamic load conditions.

input current of the proposed front-end rectifier is 4.6% according to the current harmonic spectrum shown in Fig. 15(c). This value is in accordance with the limitations of the IEEE standards. Hence, the ability of the controller is verified by this dynamic response.

VI. Conclusion

This study presents an active front-end PFC rectifier for high power telecom applications. The feasible switching states of the bidirectional switches are identified and incorporated into the system. Triangular carrier-based control logic is applied to reduce the input current ripples and thereby cause the current shape to become nearly sinusoidal. Hence, the proposed system results in low THD of the input current and voltage and maintains a close to unity PF. The proposed active front-end PFC rectifier is modeled and designed. In addition, the performance of the proposed rectifier is analyzed by MATLAB simulations under varying load conditions. The power quality parameters, such as the THD of the source voltage/current, displacement PF, distortion factor, PF, and ripple factor, are in accordance with the IEEE standards. Furthermore, the performance of the proposed system is verified using the test results taken from the developed prototype. According to the analysis and results, the power quality performance of the proposed rectifier is improved. Hence, the proposed system is applicable to high- power telecom applications.

Appendix

Parameters of the Proposed Front-End Rectifier

Three-phase source voltage, V_{ab}	400 V (line-line rms)
Source frequency, f	50 Hz
Source inductance, L	4 mH
Switching frequency, f_S	20 kHz
DC-link capacitor, C	900 µF
DC-link voltage, V_{dc}	600 V
Load power, P_o	9 kW

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