JPE 18-6-4

https://doi.org/10.6113/JPE.2018.18.6.1642
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Flyback AC-DC Converter with Low THD Based on Primary-Side Control

Changyuan Chang†, Luyang He*, Zixuan Cao*, and Dadi Zhao*

†,*School of Microelectronics, Southeast University, Nanjing, China

Abstract

A single-stage flyback LED AC-DC converter based on primary-side control under constant current mode is proposed in this study. The proposed converter features low total harmonic distortion (THD) and high power factor (PF). It also consists of a zero-crossing distortion compensation circuit and a variable duty ratio control compensation circuit to deal with the line current distortions caused by fixed duty ratio control. The system model and layout are built in Simplis and Cadence, respectively. The feasibility and performance of the proposed circuit is verified by designing and fabricating an IC controller in the HHNEC 0.35 μm 5 V/40 V HVCMOS process. Experimental results show that the PF can reach a level in the range of 0.985–0.9965. Moreover, the average THD of the entire system is approximately 10%, with the minimum being 6.305%, as the input line voltage changes from 85 VAC to 265 VAC.

Key words: AC–DC, Fixed duty ratio control distortion, Flyback converter, Low THD, Zero-crossing distortion

I. INTRODUCTION

LED lighting has attracted much attention in green development applications [1]-[3]. As key components, different architectures and techniques of LED drive circuits have been studied, and flyback power factor correction (PFC) converters are the most widely used because of their strong anti-interference ability, flexible conversion, low cost, and simple structure [4]-[7]. Existing studies have shown that single-stage flyback PFC converters involve various control strategies [8], [9]. The common control modes used are peak current mode control, average current mode control, and single-cycle mode control.

The harmonics generated by power electronic devices for switching power supply can cause serious pollution to power grids. These harmonics increase power grid losses and cause interferences to communication lines, radar equipment, and other surrounding communication systems. In addition, harmonics exert adverse effects on power electronic devices, such as switching power supplies. Harmonics decrease the power factors (PFs) of circuits and influence the utilization rate of electric energy. In addition, harmonics cause the circuit to generate large spike currents, which seriously damage filter capacitors on the DC side. Meanwhile, an input side electromagnetic interference (EMI) filter should be large due to high peak current pulses [10].

To improve the efficiency, increase the reliability, and minimize the harmonic pollution of power grids, considerable studies have analyzed line current distortions and the reduction of the distortion effect on circuit performance by increasing system complexity [11]-[13]. In 2010, Shi Huang, Tang, Dan, Chen, and others developed two methods to compensate for those distortions [14]. The first method replaces the traditional zero-current detector with zero-voltage switching to obtain an accurate demagnetization time. The second method reverses the voltage on an input capacitor and multiplies it by a certain factor to correct the turn-on time. With this method, the distortion caused by the reverse current can be compensated for. The study used a direct truncation approach instead of making the circuit work properly in a zero-crossing distortion region. In 2012, Li Yani, Yang Yintang, and others proposed a periodically self-starting timing circuit, in which a shunt resistor was added between the oscillator and the auxiliary winding to reduce zero-crossing distortions and prevent the system from reaching a zero state [15]. However, an extra circuit is required and thus increases system complexity. At the same

Manuscript received Jan. 23, 2018; accepted Sep. 6, 2018
Recommended for publication by Associate Editor Il-Oun Lee.
†Corresponding Author: ccyycc@seu.edu.cn
Tel: +86- 25-83791835-8206, Southeast University
*School of Microelectronics, Southeast University, China

time, the shunt resistor is inaccurate because it is easily affected by external factors, such as temperature and noise. In 2013, Jen-Chieh Tsai, Chi-Lin Chen, and others presented a new approach to decrease input current distortions [16]. This approach adds an original sawtooth wave to make the signal follow the input voltage amplitude, and the comparison result of the sawtooth wave and the output voltage is used to control the switching transistor. In addition, the study proposed a non-negative voltage and zero current detection circuit that uses an up-and-down clamping method to improve switch sensitivity. In 2015, Xiaoru Xu and Huiqiang Chen developed a frequency-limiting circuit to avoid EMIs and to reduce input current distortions [17]. An adaptive blanking time control circuit was also presented to deal with zero-crossing distortions. Although the distortion problem in light loads and small input line voltages is resolved, the heavy load and large input line voltage problems were not analyzed. The PF can reach 0.96 when the input voltage is 220 VAC, which is unsuitable.

Section 2 presents two kinds of distortion that frequently occur in traditional single-stage flyback AC–DC converters based on primary side control. Section 3 analyzes the simulation result of the Simplis model of compensated circuits. Section 4 describes the chip layout and test results, and Section 5 provides the content summary.

II. Analysis and Construction of Two Kinds of Compensation Circuit

The structure of the proposed circuit is shown in Fig. 1. The ideal waveforms of the input line voltage V_{in}, inductance current I_p, freewheeling diode current I_D, switch gate voltage V_{gs}, output current I_{out}, and output voltage V_{out} are shown in Fig. 2.

The ideal relation among V_{in}, input average current I_{av}, inductance peak current I_{pk}, duty cycle D, and turn-on time T_{on} is illustrated as follows:

$$I_{av} = \frac{1}{2} \cdot I_{pk} \cdot D = \frac{1}{2} \cdot \frac{V_{in}}{L} \cdot T_{on} \cdot D \qquad (1)$$

However, the practical fact can be complicated. Next, the influence of nonideal factors on the PF and total harmonic distortion (THD) of the system is analyzed, and the corresponding compensation circuits are established.

A. Analysis of Zero-Crossing Distortion and Construction of Compensation Circuit

Zero-crossing distortion is mainly caused by two conditions. First, due to the presence of residual charges, the input capacitance C_{in} cannot be normally charged when the input line voltage is small (near the zero-crossing area). Meanwhile, the diodes in the bridge rectifier are reverse biased, and the circuit cannot normally work. Second, the output energy delivered is reduced due to the resonance

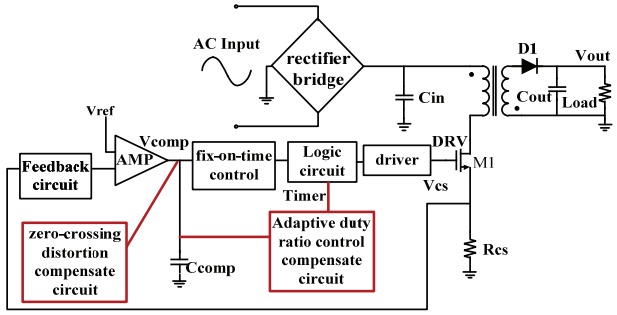


Fig. 1. Structure of the proposed circuit.

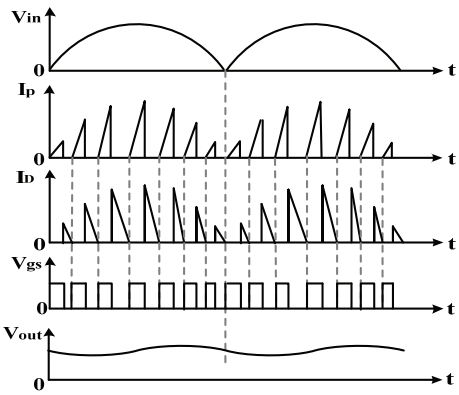


Fig. 2. Ideal waveforms of the system.

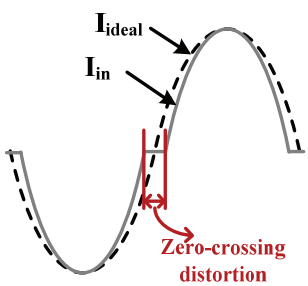


Fig. 3. Distorted waveform caused by zero-crossing distortion.

among inductance L, parasitic capacitance C_{ds} of the switch transistor, and input capacitor C_{in}, which causes zero-crossing distortion. This kind of distortion worsens when the input line voltage is small or the system is in light load. Thus, T_{on} should be increased under small input voltage, and the discharging time of C_{in} and charging time of the inductor should be extended. The distorted input current and the ideal sinusoidal waveform are shown in Fig. 3.

The zero-crossing distortion compensation circuit is shown in Fig. 4. The output of comparator COMP controls switch transistor MN7, consequently affecting the working state of switch MP4. EN1 is an enable signal. The circuit operates normally when EN1 is low. COMP outputs a high voltage and turns switches MN7 and MN4 on when the COMPENSATION signal is lower than that of the reference voltage. Thus, the COMPENSATION signal is compensated for by the system. The output is low, and switches MN7 and

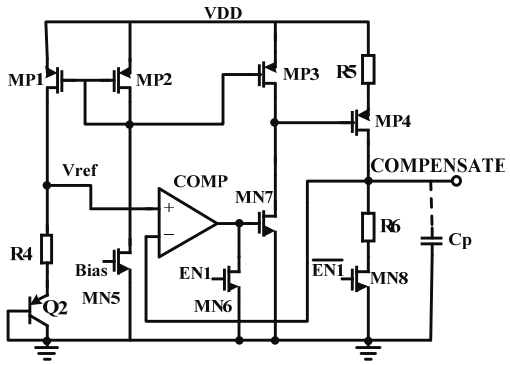


Fig. 4. Schematic of zero-crossing distortion compensation circuit.

MN4 are sequentially turned off when the voltage of the COMPENSATION signal reaches the value of the positive terminal of COMP. The values of resistances R5 and R6 influence the compensated input current waveform.

In addition, a temperature-independent reference voltage V_+ is generated by triode Q2, load resistance R4, and transistors MP1, MP2, and MN5. This reference voltage is used as the positive input of COMP. V_+ can be expressed as follows:

$$V_+ = I_1 \cdot R_4 + V_{EB} \tag{2}$$

where V_{EB} is the voltage drop between the emitter and the base of triode Q2 and I_1 is the current flowing through transistor MP1, resistor R4, and triode Q2 collector.

Output voltage $V_{COMPENSATION}$ is used as the feedback to access the negative input of COMP.

$$V_- = V_{COMPENSATION} \tag{3}$$

When the reference voltage as the control signal of COMP is less than that of V_+, $V_{COMPENSATION}$ is compensated to the following value:

$$V_{COMPENSATION} = \frac{R_6}{R_5 + R_6} \cdot V_{DD} = K_R \cdot V_{DD} \tag{4}$$

where R5 and R6 are the resistance values of R5 and R6, respectively. Thus, the effect of the zero-crossing compensation module on the entire system is influenced by V_+ and K_R.

The above discussion is based on an ideal case. In actual circuits, Equation (4) can be rewritten by considering parasitic capacitance C_P of resistance R6 and by ignoring the slightly important parasitic capacitance of resistance R5 and switch MP4 due to the existence of the parasitic capacitance of resistance.

$$V_{COMPENSATION} = \frac{R_6}{sC_P \cdot R_5 \cdot R_6 + (R_5 + R_6)} \cdot V_{DD} \tag{5}$$

The relationship between current i_R flowing through resistor R6 and current i_C through parasitic capacitance C_P is shown as follows:

$$i_c = C_P \frac{dv_C}{dt} \tag{6}$$

$$i_R = \frac{v_C}{R_6} \tag{7}$$

Equations (6) and (7) are substituted with the following equations:

$$(i_R + i_C) \cdot R_5 + v_C = V_{DD} \tag{8}$$

$$R_5 \cdot C_P \cdot \frac{dv_C}{dt} + \left(1 + \frac{R_5}{R_6}\right) \cdot v_C = V_{DD} \tag{9}$$

$$v_C = \frac{R_6}{R_5 + R_6} \cdot V_{DD} \cdot \left(1 - e^{-\frac{t}{\tau}}\right) = K_R \cdot V_{DD} \cdot \left(1 - e^{-\frac{t}{\tau}}\right) \tag{10}$$

$$\tau = \frac{R_5 \cdot R_6}{R_5 + R_6} \cdot C_P = K_\tau \cdot C_P \tag{11}$$

Therefore, the output of the entire compensation circuit satisfies the following equation:

$$V_{Compensation\_OUT} = \begin{cases} \frac{1}{2} \cdot K_R \cdot V_{DD} \cdot \left(1 - e^{-\frac{1}{Kt} \frac{t}{C_P}}\right) + \frac{1}{2} \cdot V_{COMPENSATION}, & V_{COMPENSATION} < V_{REF} \\ V_{COMPENSATION}, & V_{COMPENSATION} \geq V_{REF} \end{cases} \tag{12}$$

where

$$V_{REF} = V_+ = I_1 \cdot R_4 + V_{EB} \tag{13}$$

Compensated output $V_{Compensation\_OUT}$ is used as reference V_{REF} in Equation (12) to control the input current and thereby achieve a high PF and low THD.

B. Analysis of Input Current Distortion Caused by Fixed Duty Cycle Control and Construction of Compensation Circuit

The average value of the input current can be expressed as (1). The PF of the system is improved when $I_{pk} \times D$ is proportional to V_{in}, which indicates that $T_{on} \times D$ is constant and I_{av} is proportional to V_{in}. The average current expression is shown in (1). However, because T_{on} is fixed, T_{off} is extended with the increase of V_{in}, and the duty cycle D decreases. Therefore, I_{av} is not directly proportional to V_{in}, and the PF cannot reach 1. The fixed on time-controlled active PFC circuit can only ensure that peak current I_{pk} is proportional to V_{in}; it cannot guarantee that I_{av} is proportional to V_{in}. Thus, the fixed on time control is unable to achieve a high PF and low THD.

For the boundary model system, the following formula is expressed as

$$\frac{V_{in}}{L} \cdot T_{on} = I_{pk} = \frac{N_{ps} \cdot V_{out}}{L} (T_{sw} - T_{on}) \tag{14}$$

where N_{ps} is the former side turn ratio and T_{sw} is the switching cycle. Equation (14) can be obtained by (15).

$$\frac{T_{on}}{T_{sw}} = \frac{N_{ps} \cdot V_{out}}{V_{in} + N_{ps} \cdot V_{out}} \tag{15}$$

By combining (1) and (15), we can obtain (16) as follows:

$$I_{av} = \frac{1}{2} \cdot I_{pk} \cdot D = \frac{1}{2} \cdot \frac{V_{in}}{L} \cdot T_{on} \cdot \frac{T_{on}}{T_{sw}} = \frac{1}{2} \cdot \frac{T_{on} \cdot N_{ps} \cdot V_{out}}{L} \cdot \frac{V_{in}}{V_{in} + N_{ps} \cdot V_{out}} \tag{16}$$

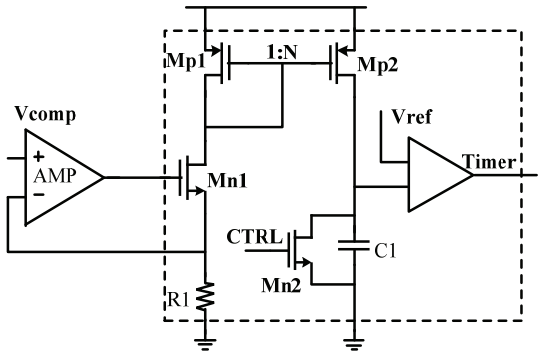


Fig. 5. Schematic of the adaptive duty cycle control compensation circuit.

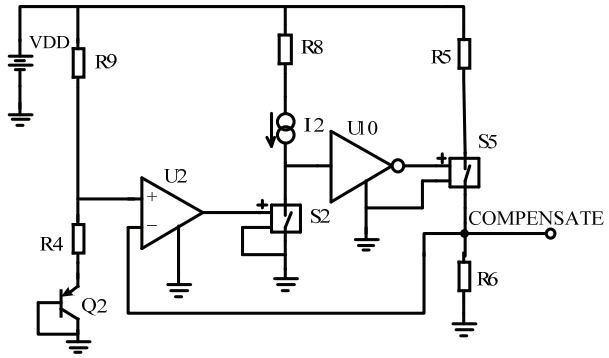


Fig. 6. Simplis model of zero-crossing compensation circuit.

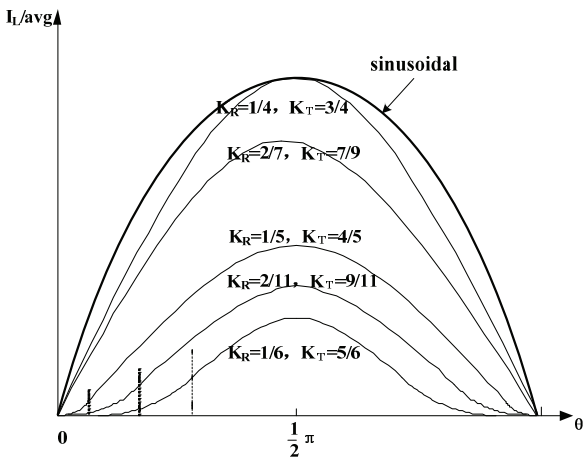


Fig. 7. Input current waveforms in different values of K_R and K_τ.

As shown in (16), I_{av} deviates from the voltage waveform with the changes of V_{in}, resulting in the increase of the THD and decrease of the PF. Solving this problem requires the use of other methods apart from the control of T_{on}. Therefore, a new variable duty ratio compensation circuit is proposed. Its schematic is shown in Fig. 5.

As shown in Fig. 5, voltage V_{comp}, which is used to control T_{on}, is converted into current I_{comp} through amplifier AMP, resistor R1, and transistor Mn1.

$$I_{comp} = \frac{V_{comp}}{R1} \tag{17}$$

Then, current I_{comp} is converted into the charging current of C1 through a current mirror with a ratio of 1: N (the ratio of W/L of transistors Mp1 and Mp2 is 1: N), and the output signal Timer can be expressed as follows:

$$Timer = \frac{C1 \cdot V_{ref}}{\frac{V_{comp}}{R1} + 1}. \tag{18}$$

Then, the corresponding frequency of Timer can be written as f_{timer} = 1/Timer $\propto$ V_{comp}. The circuit operates as follows: the increase of the line voltage or the decrease of the output voltage results in the rise of V_{CS} and the output voltage of feedback circuit. Then, reference voltage V_{ref} and the output voltage of the feedback circuit are sent to the positive and negative points of the error amplifier, respectively. Consequently, output voltage V_{comp} of the error amplifier decreases, and the voltage Timer increases, thereby increasing opening time T_{on}. This condition indicates that the negative effect caused by the increase of input voltage V_{in} and decrease of duty ratio D can be offset or reduced. In sum, the modulation of system frequency is achieved by controlling voltage V_{comp}.

III. Simulation and Test Verification

A. Modeling, Simulation, and Analysis of Zero-Crossing Distortion Compensation Circuit

As shown in Fig. 6, the Simplis model is built on the basis of the construction in Fig. 4. The reference circuit that generates the voltage of the positive point of comparator COMP is replaced with resistors R9 and R4. The COMP in Fig. 4 represents comparator U2 in Fig. 6. To simulate the function of the compensation circuit, we set the default value of EN1 to low. In this case, MN6 and MN8 can be omitted, and transistors MN7 and MP4 are replaced with switches S2 and S5, respectively.

As shown in Equation (12), the different values of coefficients K_R and K_T affect the output voltage of the compensation circuit. In other words, they determine the impact of the compensation circuit on the system. The comparison of the different values of K_R and K_τ of the input current waveforms is shown in Fig. 7. At this time, input voltage V_{in} is 220 VAC, and reference voltage V_{REF} is 0.2 VDC. As shown in Fig. 7, the input current can follow the change of the input voltage without any distortion in a half period when K_R = 1/4 and K_τ = 3/4. Compared with several data sets, the input current is remarkably improved when K_R = 1/4 and K_τ = 3/4.

As shown in Fig. 8, the Simplis model is built on the basis of the construction in Fig. 5. The current mirror consisting of transistors MP1 and MP2 in Fig. 5 is replaced with current-controlled current source G1, and resistor R3 in Fig. 5 is represented by the impedance of transistor MP2. U3 is a buffer. Timer turns from high to low when the voltage across

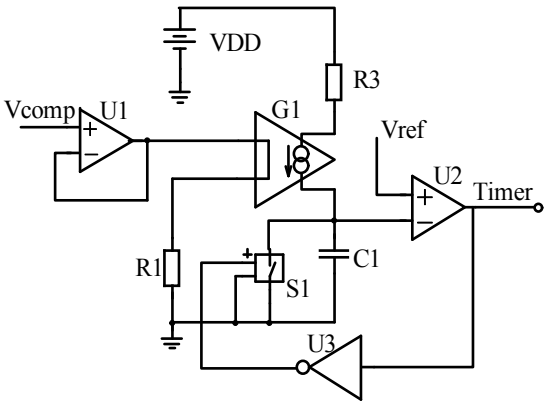
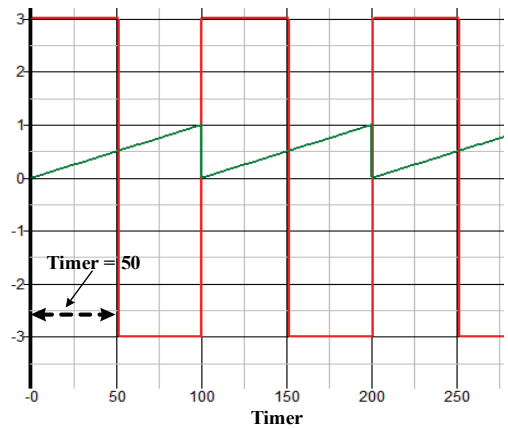
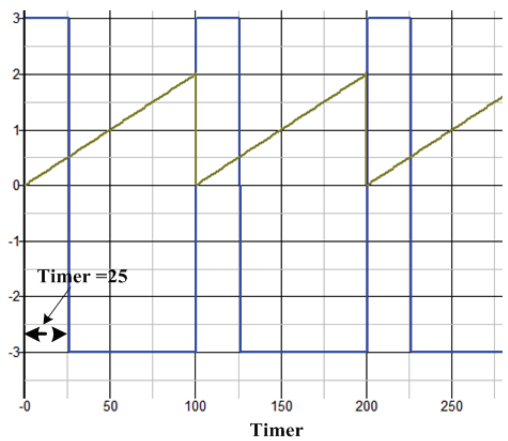


Fig. 8. Simplis model for adaptive duty cycle control compensation circuit.



(a)



(b)

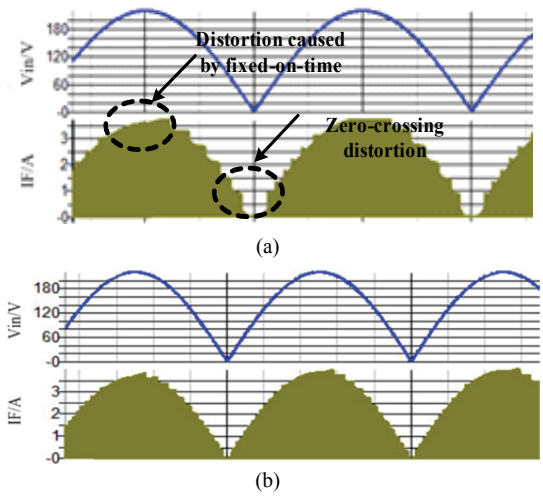
Fig. 9. Simulation waveforms of adaptive duty cycle control compensation circuit. (a) Waveforms for V_{comp} = 1 V. (b) Waveforms for V_{comp} = 2 V.

the capacitor is charged to a value greater than or equal to V_{ref}. Then, switch S1 is closed, capacitor C1 is discharged, and Timer changes to a high level again to prepare for the next flip.

The simulation waveforms are presented in Fig. 9. The duty cycle of Timer is 50%, and the voltage slope of the negative side of comparator U2 is 1 V/100 μs when V_{comp} equates to 1 V. The duty cycle of Timer becomes approximately 25%, and the slope is 2 V/100 μs when V_{comp} is changed to 2 V. In conclusion, the value of Timer can be adjusted by detecting the value of V_{comp}, and Timer changes in the opposite direction of V_{comp}. Therefore, the desired control can be achieved when this compensation circuit is added to the system.

TABLE I
PARAMETERS OF FLYBACK AC–DC CONVERTER

Key	Value
Input voltage V_{in}	85~265V_{ac}
Output current I_o	450mA
Transformer turn's ratio	48:16:6
Output capacitor	441.1μF/50V
Rectifier	MB6S
Primary inductance	890uH
Power transistor	AP03N70
Transformer frame	EE6



(a)

(b)

Fig. 10. Simulation results before and after compensation: (a) Simulation result of the uncompensated system; (b) Simulation result of the compensated system.

Several parameters of the proposed flyback AC–DC converter are listed in Table I. The simulation results in Simplis are shown in Fig. 10, where (a) is the simulation result of the uncompensated system and (b) is the result of the compensated system. Vin is the waveform of the 220 VAC input line voltage, and IF is the input current waveform.

As shown in Fig. 10, the input line current has serious distortions, and those distortions are reduced to a great extent after the addition of compensation circuits in the system. The THD of Fig. 10(a) measured by Simplis is approximately 25%. The PF can be calculated on the basis of the relationship between the THD and the PF in Equation (19). Suppose that $\cos\psi_1$ is 1. The PF of Fig. 10(a) can then be obtained as 0.97. By using the same method, the THD and PF of Fig. 10(b) can be calculated as 5.2% and 0.9986,

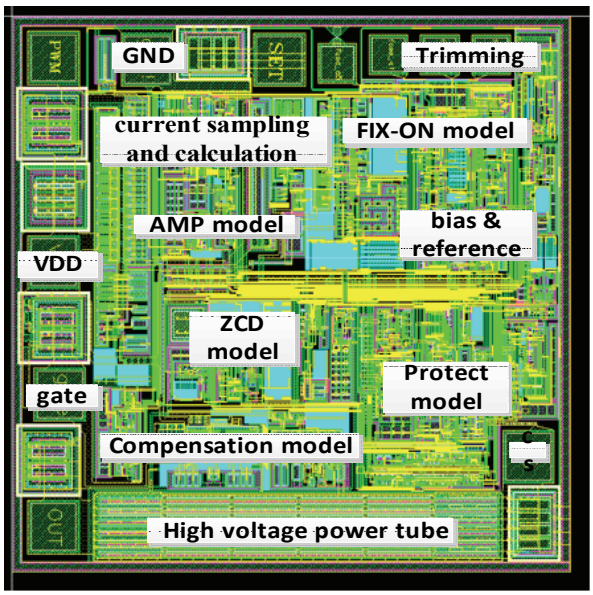


Fig. 11. Micro-graph of the fabricated chip.

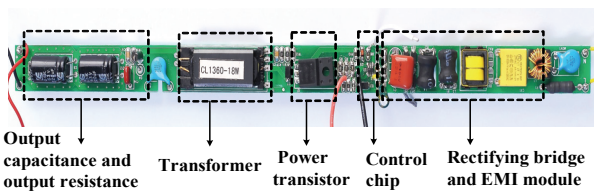


Fig. 12. System test board.

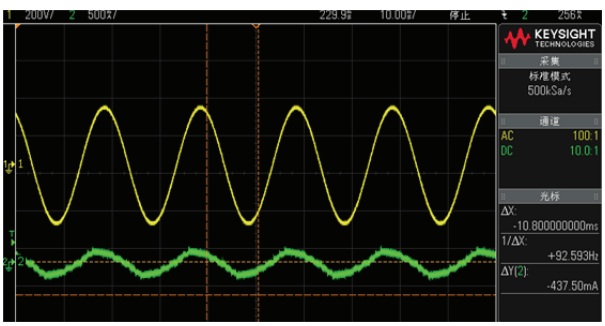


Fig. 13. Waveforms of input current and voltage.

respectively. The results indicate that the THD and PF are improved by the compensation circuit.

$$PF = \frac{\cos \varphi_1}{\sqrt{1+THD^2}} \tag{19}$$

IV. Experimental Results

The IC is implemented in the HHNEC 0.5 μm 5 V/40 V HVCMOS process. A micro-graph of the fabricated chip is shown in Fig. 11. The operating AC voltage of the PCB is 85–265 VAC, and the output power is 3–20 W. As shown in Fig. 12, the basic modules of the circuit, such as output capacitance and resistance, transformer, power transistor, control chip, rectifying bridge, and EMI module, are labeled.

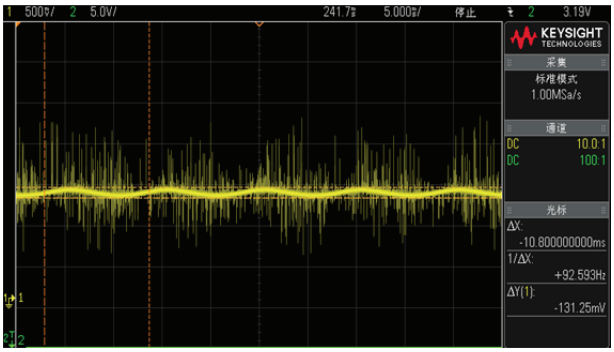


Fig. 14. Waveform of voltage V_{comp}.

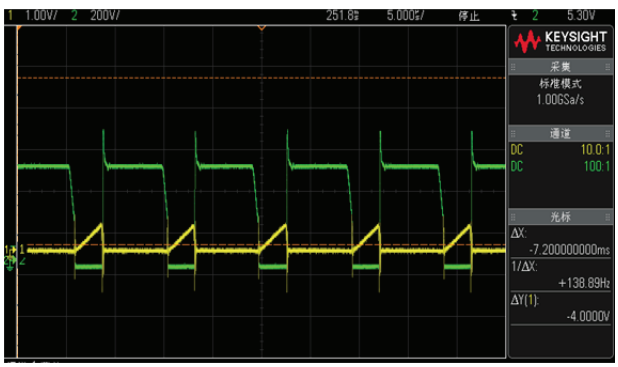


Fig. 15. Waveforms of V_{gate} and V_{cs}.

Fig. 13 illustrates the waveforms of 220 VAC/60 Hz input voltage and current. The test result shows that the current follows the input voltage well.

The voltage waveform of V_{comp} is shown in Fig. 14. The test result shows that V_{comp} remains approximately constant under the steady operation of the circuit. Although several ripples are superimposed on V_{comp}, its value basically remains at 130.5 mV.

In Fig. 15, the green and yellow lines are the waveforms of switch gate voltage V_{gate} and voltage V_{cs} on sampling resistor R_{cs} respectively. The system is in good operation state.

The PF line chart of different systems at several input line voltages is shown in Fig. 16. The zero-crossing distortion and adaptive duty cycle control compensation circuits effectively improve the PF. Specifically, the PF increases from 0.973 (maximum before compensation) to 0.9965. The THD line chart of different systems at several input line voltages is shown in Fig. 17. The zero-crossing distortion and adaptive duty cycle control compensation circuits effectively reduce the harmonic component of the system. Specifically, the THD is reduced from 23.72% (before compensation) to 6.305%.

Obviously, the system performance is improved by using the proposed design. On the basis of the test results of the chip at different voltages and formula of efficiency in (20), the following equation is derived:

$$\eta = \frac{P_o}{P_{in}} \tag{20}$$

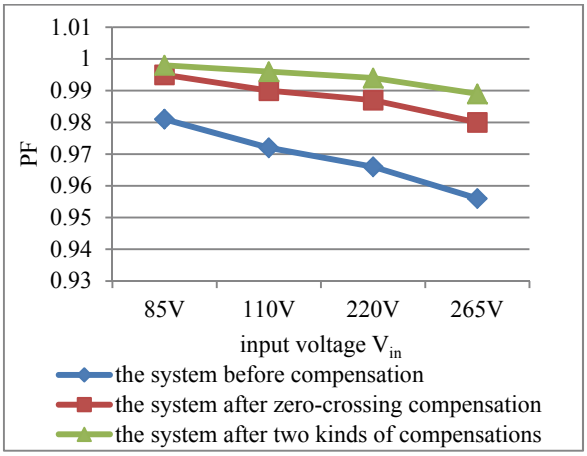


Fig. 16. PFs of different systems at several input voltages.

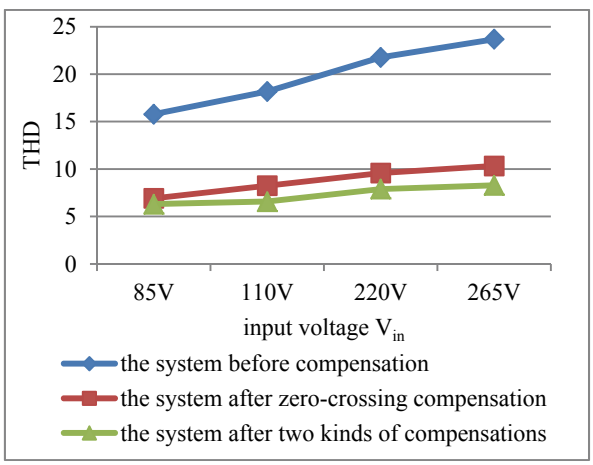


Fig. 17. THDs of different systems at several input voltages.

TABLE II
EFFICIENCY TABLE

Input voltage V_{in}/Vac	Input power P_{in}/W	Output voltage V_o/Vdc	Output current I_o/mA	Output power P_o/W	Efficiency η
90	24.1	45.25	449	20.3274	85.931%
120	23.48	45.35	449	20.3621	86.721%
180	23.21	45.37	450.6	20.4437	88.082%
220	23.43	45.38	451.1	20.4709	87.371%
264	23.76	45.37	451.5	20.4846	86.214%

TABLE III
PERFORMANCE PARAMETERS OF FLYBACK AC–DC CONVERTER

Key	Value
Input voltage V_{ac}	85~265V_{ac}
Output current I_o	450mA
Power factor	0.9965~0.987
THD	6.305%~10.05%
Efficiency	86%~88%
Output current ripple	62.5mA
Switch frequency	60kHz~140kHz

TABLE IV
COMPARISON OF THE PROPOSED CONVERTER AND OTHER PRODUCTS

	This paper	**FL7732**	**SY5802**	**BP3318**
Input voltage	85~265Vac	90~265Vac	90~265Vac	85~265Vac
Output power	3~20W	9W	10.8W	100W
Max switch frequency	100kHz	120kHz	120kHz	100kHz
Conversion efficiency	>86%	>85%	87%	84.8%
Power factor	0.985	>0.9	>0.9	>0.92
THD	<11.5%	<25%	<20%	<18%
Linear regulation rate	±2%	±3.5%	±3%	±4.1%
Load regulation rate	±2%	±2.5%	±3%	±2.2%

The performance parameters of the proposed flyback AC–DC converter are shown in Table III. The comparison of the performances of the proposed converter and other products is shown in Table IV.

V. CONCLUSION

The proposed flyback AC–DC converter uses zero-crossing distortion and adaptive duty cycle control compensation circuits to compensate for two kinds of line current distortions caused by zero-crossing distortions and fixed duty ratio control. With the proposed converter, the input line current waveform is close to the sinusoidal waveform. A model is built, and a new AC–DC converter circuit is simulated in Cadence to verify the effect of the two proposed circuits. The simulation results show that the compensation circuits are valuable in improving system performance. The test results indicate that the average THD of the entire system is approximately 10%, with the minimum being 6.305%. The PF is above 0.965, with the maximum being 0.9965.

REFERENCES

[1] S. Y. Hui, S. N. Li, X. H. Tao, W. Chen, and W. M. Ng, "A novel passive offline LED driver with long lifetime," *IEEE Trans. Power Electron.*, Vol. 25, No. 10, pp. 2665-2672, Oct. 2010.

[2] Q. Hu and R. Zane, "LED driver circuit with series-input-connected converter cells operating in continuous conduction mode," *IEEE Trans. Power Electron.*, Vol. 25, No. 3, pp. 574-582, Mar. 2010.

[3] B. Wang, X. Ruan, K. Yao, and M. Xu, "A method of

reducing the peak-to- average ratio of LED current for electrolytic capacitor-less AC–DC drivers," *IEEE Trans. Power Electron.*, Vol. 25, No. 3, pp. 592-601, Mar. 2010.

[4] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: A survey," *IEEE Trans. Power Electron.*, Vol. 18, No. 3, pp. 749-755, May 2003.

[5] D. G. Lamar, J. S. Zuniga, A. R. Alonso, M. R. Gonzalez, and M. M.H. Alvarez, "A very simple control strategy for power factor correctors driving high-brightness LEDs," *IEEE Trans. Power Electron.*, Vol. 24, No. 8, pp. 2032-2042, Aug. 2009.

[6] T. L. Chern, L. H. Liu, P. L. Pan, and Y. J. Lee, "Single-stage flyback converter for constant current output LED driver with power factor correction," in *Proc. IEEE Ind. Electron. Appl.*, pp. 2891-2896, 2009.

[7] D. G. Lamar, M. Arias, A. Rodriguez, A. Fernandez, M. M. Hernando, and J. Sebastian. "Design-oriented analysis and performance evaluation of a low-cost high-brightness LED driver based on flyback power factor corrector," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 7, pp. 2614-2626, Jul. 2013.

[8] X. Xie, J. Wang, C. Zhao, Q. Lu, and S. Liu, "A novel output current estimation and regulation circuit for primary side controlled high power factor single-stage flyback LED driver," *IEEE Trans. Power Electron.*, Vol. 27, No. 11, pp. 4602-4612, Nov. 2012.

[9] J. Zhang, H. Zeng, and T. Jiang, "A primary side control scheme for high power-factor LED driver with TRIAC dimming capability," *IEEE Trans. Power Electron.*, Vol. 27, No. 11, pp. 4619-4629, Nov. 2012.

[10] H. Q. Ben, J. H. Zhang, G. H. Liu, and T. Liu, *Active Power Factor Correction in Switching Power Supply*, the China Machine Press, pp. 2-6, 2010.

[11] J. M. Zhang, S. Y. Zhao, H. L. Zeng, and X. K. Wu, "An optimal peak current mode control scheme for critical conduction mode (CRM) buck PFC converter," in *2013 10th China International Forum on Solid State Lighting*, pp. 182-189, 2013.

[12] K. Mahmud and L. Tao, "Power factor correction by PFC boost topology using average current control method," in *2013 IEEE Global High Tech Congress on Electronics*, pp. 16-20, 2013.

[13] K. Yao, X. B. Ruan, X. J. Mao, and Z. H. Ye, "Variable-duty-cycle control to achieve high input power factor for DCM BOOST PFC converter," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 5, pp. 1856-1865, May 2011.

[14] S.-H. Tang, D. Chen, C.-S. Huang, C.-Y. Liu, and K.-H. Liu, "A new on-time adjustment scheme for the reduction of input current distortion of critical-mode power factor correction boost converters," in *Proc. IEEE Int. Power Electron. Conf.*, pp. 1717-1724, 2010.

[15] Y. N. Li, Y. T. Yang, Z. M. Zhu, W. Qiang, and L. X. Liu, "Optimal design of zero-crossing distortion for single period CRM PFC converter," *Journal of Xi'an Electronic and Science University (Natural Science Edition)* , Vol.2, pp. 108-113, Apr. 2012.

[16] J.-C. Tsai, C.-L. Chen, Y.-T. Chen, C.-L. Ni, C.-Y. Chen, and K.-H. Chen, "Perturbation on-time (POT) technique in power factor correction (PFC) controller for low total harmonic distortion and high power factor," *IEEE Trans. Power Electron.*, Vol. 28, No. 1, pp. 199-212, Jan. 2013.

[17] X. R. Xu, H. Q. Chen, B. D. You, and X. B. Wu, "Power factor corrected primary side regulated flyback controller for smart LED lighting system," in *2015 12th China International Forum on Solid State Lighting*, pp. 110-113. 2015.

Changyuan Chang received his M.S. and Ph.D. degrees in Electronic Engineering from Southeast University, Nanjing, China, in 1990 and 2000, respectively. He is currently serving as an Associate Professor in the School of Integrated Circuit in Southeast University. His main research interests include the design of analog-controlled and digitally controlled ICs for power management.

Luyang He was born in 1995 in Henan, China. He received his B.S. degree from XiDian University, Xi'an, China, in 2017. He is presently working toward his M.S. degree in IC Design at Southeast University, Nanjing, China. His current research interests include analog integrated circuits, power electronics, and AC–DC converters.

Zixuan Cao received her B.S. degree from Xi'an University of Posts and Telecommunications, Xi'an, China, in 2015. She is presently working toward her M.S. degree in IC Engineering at Southeast University, Nanjing, China. Her current research interests include switch-mode power and AC–DC converters.

Dadi Zhao was born in Jiangsu, China, in 1995. He received his B.S. degree from Nantong University, Nantong, China, in 2016. He is presently working toward his M.S. degree in IC Engineering at Southeast University, Nanjing, China. His current research interests include analog integrated circuits, power electronics, and CV/CC AC–DC converters.