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Rapid Dynamic Response Flyback AC-DC Converter Design

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Abstract

A constant voltage AC-DC converter based on digital assistant technology is proposed in this paper, which has rapid dynamic response capability. The converter operates in the PFM (Pulse Frequency Modulation) mode. According to the load state, the compensation current produced by the digital compensation module was injected into the CS pin to adjust the switching pulse width dynamically and improve the dynamic response. The control chip is implemented based on NEC 1μm 5V/40V HVCMOS process. A 5V/1.2A prototype has been built to verify the proposed control method. When the load jumps from idle to heavy, the undershoot time is only 7.4ms.

Key words: Constant voltage, PFM mode, Rapid dynamic response

I. INTRODUCTION

In recent years, portable electronic products have been springing up, and the demand of high performance AC-DC converters has become huge. The output voltage of conventional secondary-side regulation (SSR) flyback converters is detected directly and transferred to the controller by an optical coupler and a precise voltage source [1], [2]. It is easy for SSR converters to obtain a rapid dynamic response. However, the complex structure of SSR converters and the sensitivity of optical couplers to temperature are the drawbacks [3]-[6]. Indeed, the primary-side regulation (PSR) flyback converter is popular due to the fact that its structure is simple and it does not need an optical coupler or a precise voltage source [7], which reduces both the cost and volume. In addition, the PSR structure has good system reliability and anti-interference [8]-[12].

In 2010, USB battery charging specification 1.2 put forward stringent requirements on the output performance of the switching power supplies for USB charging, which imposed strict specifications on the output voltage variations caused by load jumping. Therefore, scholars and experts from various countries have initiated research aimed at improving the dynamic response capability of switching power supplies.

A rapid dynamic response flyback AC-DC converter based on digital assistant technology is proposed in this paper. The detailed operation principle and design of compensation modules are illustrated in Section II. Simulation results will be given in Section III. Experimental results based on a prototype will be given in Section IV. Section V will make some conclusions of the proposed design.

II. DESIGN OF THE CONTROL IC

A. System Review

The system diagram of the PSR AC-DC flyback converter with the proposed control chip is shown in Fig. 1, which consists of a bridge rectifier BD, EMI filter, RCD clamp circuit, freewheel diode D_0, capacitors C_0 and C_{f3}, inductor L_{f3}, transformer, power triode Q_1, primary current sensing resistor R_{CS}, pull-up resistor R_1, pull-down resistor R_2, filter capacitor C_C, and control IC [13], [14]. In this control chip, the FB pin is to detect information on the output voltage through the auxiliary winding, the CS pin is to detect the primary side current, the VC pin, which is connected to an external capacitor, is to convert the digital compensation current to an analog current, and the BASE pin is to drive the power triode.

A block diagram of the control IC presented in Fig. 2 is mainly comprised of a sampling module, which contains a

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TABLE I
USB BATTERY CHARGING SPECIFICATION 1.2

Parameter	Symbol	Value
Max output voltage	Vo,max	6V
Min output voltage	Vo,min	4.1V
Max undershoot time	TUDST	10ms

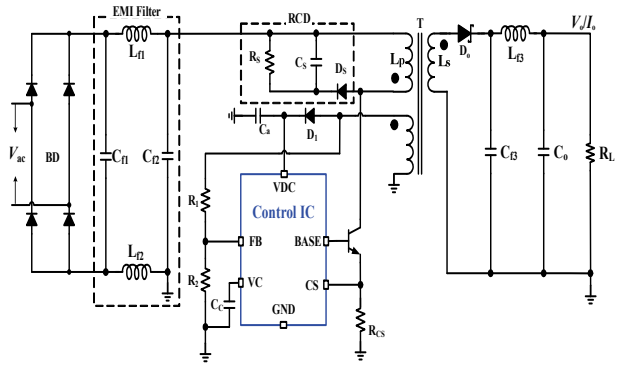


Fig. 1. System diagram of the proposed PSR constant voltage AC-DC converter.

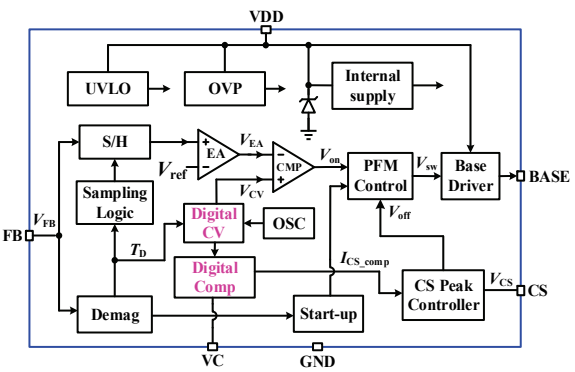


Fig. 2. Block diagram of the proposed CV control IC.

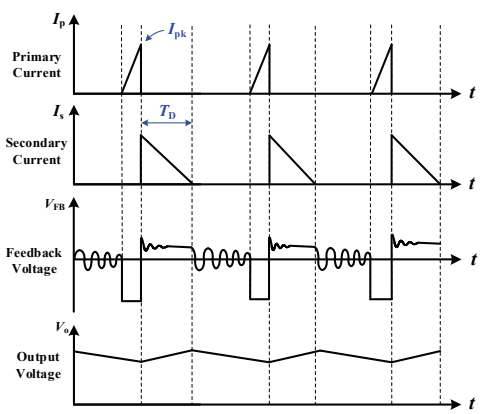


Fig. 3. Typical operating waveforms of PSR flyback AC-DC converter.

S/H and a logic module, OSC (oscillator) module, PFM generator, EA (error amplifier), digital CV (constant voltage) module, digital compensation module, CS peak controller, Base driver, internal supply, and protection module (UVLO, OVP).

Key operating waveforms of the PSR flyback converter are depicted in Fig. 3. During the conduction time, the primary side inductor current I_p ramps up linearly and the electromagnetic energy is stored in the primary inductor. Once the peak value of I_p reaches the threshold, Q_1 is turned off. The energy is released through the secondary inductor, which starts to demagnetize. The secondary side inductor current I_s decreases from its peak current to zero. T_D is the completion time of demagnetization. The auxiliary winding of the transformer is used to sense the output voltage V_o and demagnetization time. Then the information is fed back to the control IC. V_{FB} is the voltage across the auxiliary winding.

B. Principle of Dynamic Response Compensation

The PSR structure adopts a cycle by cycle sampling method. The output voltage is sampled at some point in the demagnetization time in one switching period, and the result is provided to the controller through the auxiliary winding. According to the sampling result, the controller adjusts the switching frequency to keep the output voltage stable. However, if the load jumps just after the sampling point, the controller cannot respond to this change before the next sampling point because the variation of output voltage has not been fed back into the controller, which results in a fluctuation of the output voltage. If the load jumps from light to heavy, the output voltage drops drastically since the switching period is too large under a light load and the sampling interval is too long. It takes a long time until the controller senses the variation of the output voltage again. However, if the load jumps from heavy to light, due to a high sampling frequency, the controller can make a rapid response, which avoids the large overshoot of the output voltage.

Therefore, the undershoot voltage and undershoot time are determined by the switching frequency under a light load when the load jumps from light to heavy. The higher the switching frequency under a light load, the stronger the dynamic response capability becomes.

In order to acquire a higher response speed, the switching pulse width should be adjusted dynamically on the basis of the PFM mode, which makes the frequency regulation more flexible.

From above, the switching pulse width is related to the primary peak current I_{pk}. For the CV converter operating in the PFM mode, the primary peak current I_{pk} can be expressed as:

$$I_{pk} = \frac{V_{in}}{L_P} \cdot T_{on} \tag{1}$$

Where V_{in} is the rectified line voltage, L_p is the primary inductor, and T_{on} is the turn-on time of the power diode Q1. Then the input power P_{in} can be expressed as:

$$P_{in} = \frac{L_P I_{pk}^2}{2T_s} \tag{2}$$

Where, T_s is the switch period. The substitution of Eq. (1) into Eq. (2) leads to:

$$P_{in} = \frac{V_{in}^2 T_{on}^2}{2T_s L_p} \tag{3}$$

The converter output power P_{out} is:

$$P_o = \frac{V_o^2}{R_L} \tag{4}$$

Where R_L is the load resistor.

$$\eta = \frac{P_o}{P_{in}} \tag{5}$$

According to the relationship among the input power P_{in}, output power P_o and efficiency η which is shown in Eq. (5), V_o can be defined as follows by combining Eq. (2) and Eq. (3):

$$V_o = V_{in} \cdot T_{on} \cdot \sqrt{\frac{R_L \eta}{2T_s L_p}} \tag{6}$$

By substituting Eq. (1) into Eq. (6), the output voltage can be redefined as:

$$\begin{aligned} V_o = I_{pk} \cdot \sqrt{\frac{R_L L_p}{2T_s}} &= \frac{V_{pk}}{R_{cs}} \cdot \sqrt{\frac{1}{2} \cdot \eta \cdot R_L \cdot L_p \cdot F_s} \\ &= \sqrt{\frac{1}{2} \cdot \eta \cdot R_L \cdot L_p \cdot F_s} \cdot \frac{V_{th\_cs}}{R_{cs}} \end{aligned} \tag{7}$$

Where the primary peak voltage V_{pk} is set to a constant value V_{th_cs}, and F_s is the switch frequency.

From Eq. (7), when the system is operating in the CV mode, if the primary peak voltage V_{pk} decreases, the switching frequency F_S increases, and the dynamic response capability is enhanced. Thus, a dynamic response compensation method, which can adjust V_{pk} based on the load state, is proposed. A schematic diagram of this is shown in Fig. 4.

The compensation current I_{CS_comp} is generated by the compensation module based on the switching frequency F_S. I_{CS_comp} is linear to the switching period T_S. The ratio coefficient of I_{CS_comp} and T_S is set to α, and the compensation current is:

$$I_{CS\_comp} = I_{C,max} - \alpha \cdot F_S \tag{8}$$

In Eq. (8), $I_{C,max}$ is the maximum compensation current. I_{CS_comp} is injected into the positive port of the comparator CMP and then flows out of the CS pin. The product of the primary peak current I_{pk} and the primary sensing resistor R_{CS} is the primary peak voltage V_{pk}. After compensation, V_{pk} can be derived as:

$$\begin{aligned} V_{pk} &= V_{CS\_th} - I_{CS\_comp} \cdot R_{comp} \\ &= V_{CS\_th} - I_{C,max} \cdot R_{comp} + \alpha \cdot F_S \cdot R_{comp} \end{aligned} \tag{9}$$

It can be seen in Eq. (9) that when the system is operating under a heavy load, F_S is relatively high and the compensation current I_{CS_comp} is small, which makes the primary peak voltage V_{pk} high. On the other hand, when the circuit is under a light load, F_S drops to a low level, and the large compensation current I_{CS_comp} causes V_{pk} to be relatively low. Therefore, the switching pulse width can be adjusted based on the load state after the dynamic response compensation. Since V_{CS_th}-$I_{C,max}$·R_{comp} is the minimum value of the primary peak voltage, Eq. (9) can be simplified as:

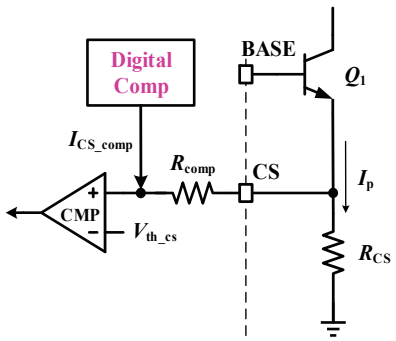


Fig. 4. Schematic diagram of dynamic response compensation.

$$V_{pk} = V_{pk,min} + \beta \cdot F_S \tag{10}$$

In Eq. (10), $V_{pk,min}$ is the minimum primary peak voltage, and β is equal to the product of α and R_{comp}. Substituting Eq. (10) into Eq. (7), the output voltage formula is expressed as:

$$V_o = \sqrt{\frac{1}{2}\eta \cdot L_P \cdot R_L \cdot F_S} \cdot \frac{V_{pk,min} + \beta \cdot F_S}{R_{CS}} \tag{11}$$

By comparing Eq. (11) with Eq. (7), it is easy to see that the regulation of V_o based on the switching frequency F_S is more sensitive. The dynamic response capability after compensation is stronger.

From another point of view, when the system is working in the CV mode, compensation current is generated depending on the load state. If the load is light, the compensation current is large. V_{pk} is forced to drop to a low level, causing the switching pulse width to become very small. As a result, the switching frequency must be improved to maintain the output voltage constant.

C. Design of the Dynamic Response Compensation Module

The digital assistant dynamic response compensation module consists of a data storage unit, encoder, current source array, RC filter and V/I converter. Based on the binary counting number T_{rise} of the switching period T_S, which is from the digital exponential waveform generator, the compensation current is produced and injected to the CS pin. A schematic diagram of compensation module can be seen in Fig. 5.

In the digital exponential waveform generator, when the power triode Q1 is turned on, the binary counting number T_{rise} is reset and increases from zero. T_{rise} is then converted into real time T_s in the data storage. However, it has not been stored until the rising edge of V_{sw} comes (T_{rise} is transmitted

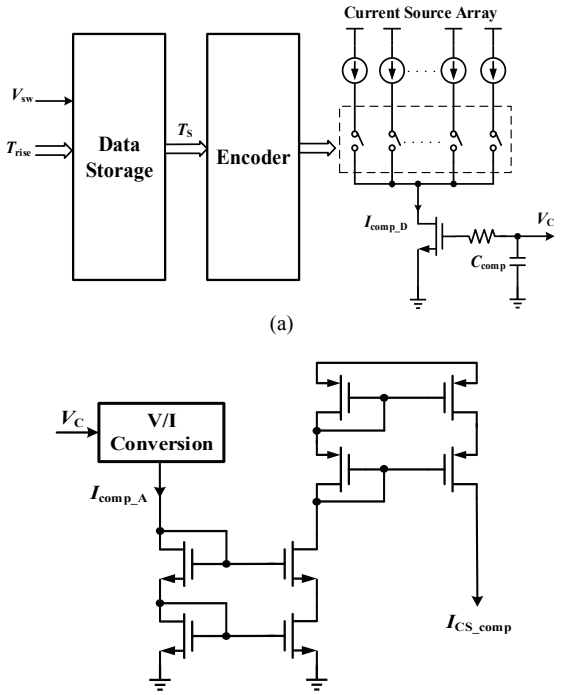


Fig. 5. Schematic diagrams of the dynamic response compensation module. (a) Digital compensation current generator; (b) Analog compensation current generator.

to the data storage in real time but has not been stored). Once the exponential waveform voltage reaches the EA output voltage, the Q1 control signal V_{sw} jumps to a high level and Q1 is turned on again. The rising edge of V_{sw} informs the data storage to store T_{rise}. At this time, T_{rise} is equal to the switching period T_S. The binary switching period T_S is encoded and the most relevant channels in the current source array are turned on, which generates the digital compensation current I_{comp_D}. The lighter the load, the more channels are turned on.

Since the digital compensation current is discrete, has large glitches and is unsuitable for injection into the CS pin, it is necessary to obtain an analog compensation current. I_{comp_D} is converted to the analog capacitor voltage V_C by RC filtering, as shown as Fig. 5(a). Then V_C is transmuted into the analog compensation current I_{comp_A}, as shown as Fig. 5(b). Through the current mirror, I_{comp_A} is converted into the dynamic response compensation current I_{CS_comp}.

III. Simulation Results

From the principle of the compensation circuit, it can be known that the compensation current is linear to the system load. In this section, the circuit is simulated under different loads. The corresponding data results are shown in TABLE II.

Key waveforms of the system load jumping from a light (load resistance is 280Ω) to a heavy (load resistance is 4.2Ω) are shown in Fig. 6. Without dynamic response compensation,

TABLE II
Switching Frequency and Compensation Current Data

Io (A)	*Ts*(μs)	*Fs*(kHz)	CS Compensation current(μs)
1.1870	22.1356	45.1761	2.660622
1.0860	23.5817	42.4058	6.286886
0.9625	24.9978	40.0035	9.74302
0.8460	26.8883	37.1909	14.39283

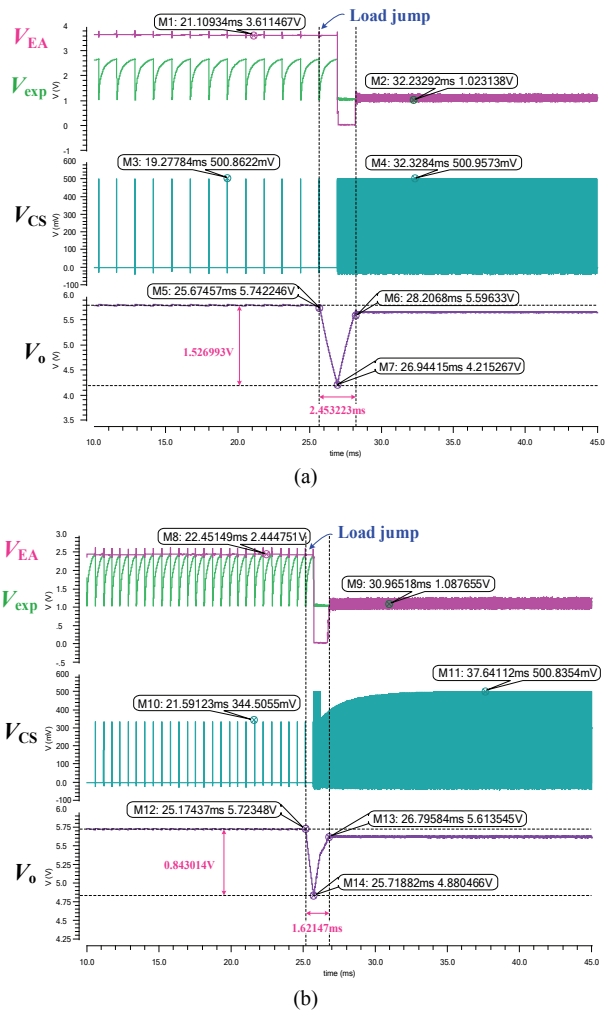


Fig. 6. Key simulation waveforms of a load jump from a light to a heavy load: (a) Simulation without dynamic response compensation; (b) Simulation with dynamic response compensation.

the undershoot of the output voltage is 1.53V and the undershoot time is 2.45ms. However, the undershoot of V_o is just 0.843V and the undershoot time is only 1.62ms when the dynamic response compensation is adopted.

IV. Experimental Results

A. Layout Design of the Control IC

The proposed AC-DC controller is implemented in NEC

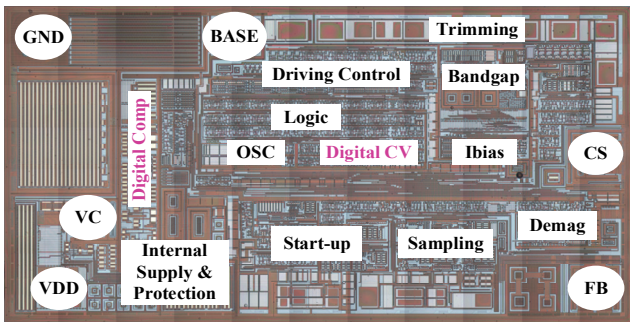


Fig. 7. Layout of proposed control IC.

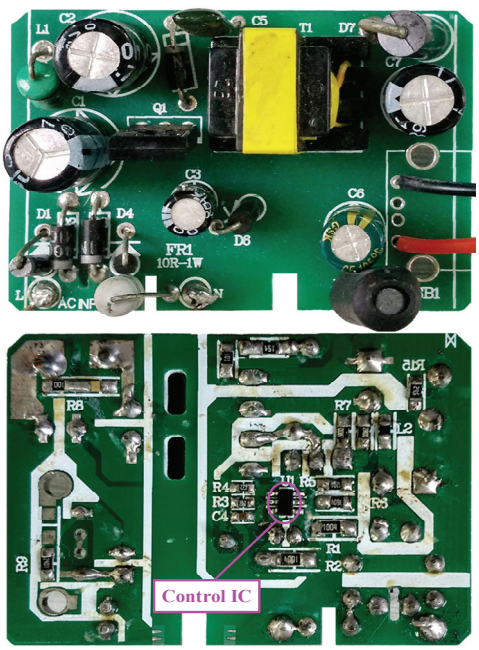
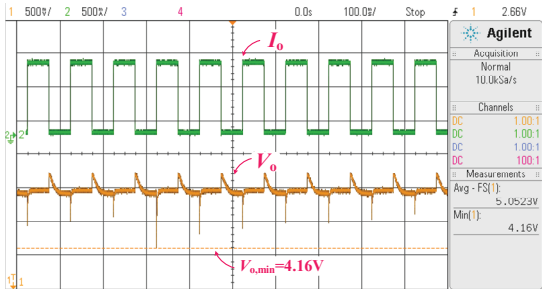


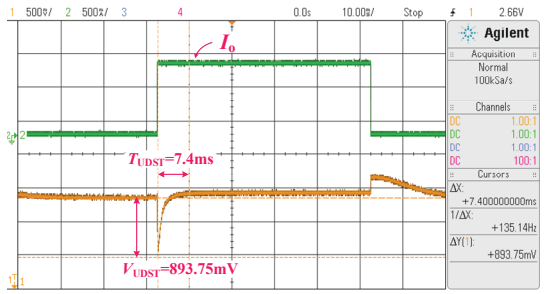
Fig. 8. Photograph of the fabricated PCB.

TABLE III
KEY COMPONENTS AND PARAMETERS

Components	Symbol	Value or Specification
Bridge rectifier	BD	1N4007
EMI filter inductor	L_{f1}, L_{f2}	1mH, 4.7μH
EMI filter capacitor	C_{f1}, C_{f2}	4.7μF
Primary-side inductor	Lp	1.4mH
Transformer core	T	EE13
Power switch	Q_1	NPN 13003
Transformer turn's ratio	$N_P/N_S/N_{AUX}$	126/11/32
Pull-up resistor	R_1	27KΩ
Pull-down resistor	R_2	3.6KΩ
Auxiliary-side Freewheel diode	D_1	FR107
Primary current sense resistor	R_{CS}	1Ω
Output filter inductor	L_{f3}	4.7μH
Output filter capacitor	C_{f3}	680μF
Output capacitor	C_o	470μF
Secondary-side Freewheel diode	D_o	SR3100



(a)



(b)

Fig. 9. Tested waveforms of the output current jumping from 0 to 1.2A. (a) Measured waveforms of several switching periods. (b) Measured waveforms of one switching period.

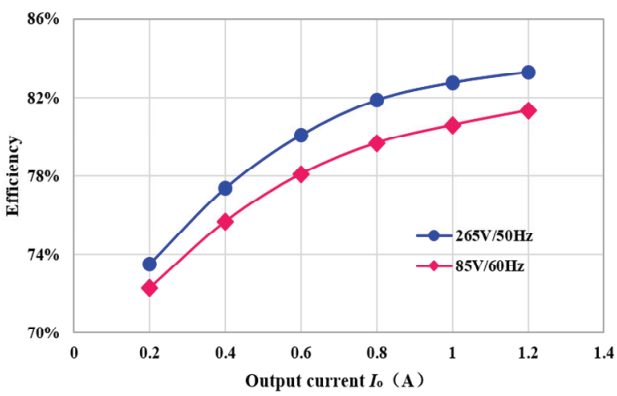


Fig. 10. Measured efficiency versus V_o under an 85Vac, 60Hz-input and a 265Vac, 50Hz-input.

1μm 5V/40V HVCMOS and the area is 974.8×510.5μm^2. The layout of this controller is shown in Fig. 7. The key modules and pins are marked in the photograph.

B. Test Results of the Proposed Control Chip

A prototype of the test board is shown in Fig. 8, and its size is about 4.8cm×3.6cm. The key components and parameters of the circuit are listed in TABLE III.

In order to verify the response capability, the load current jumps from 0A to 1.2A. The corresponding waveforms are shown in Fig. 9. The undershoot voltage V_{UDST} is about 893.75mV. As a result, the output voltage can be maintained above 4.1V. The undershoot time is 7.4ms. Therefore, the test results of the load jump all meet the requirement of USB Specification 1.2.

TABLE IV
COMPARISON BETWEEN DIFFERENT METHODS

	This work	[15]	iW1760
Topology	Flyback	Flyback	Flyback
Controller type	Analog	Analog	Digital
Output voltage	5V	5V	5V
Max output current	1.2A	1A	2V
Standby power consumption	40mW	N/A	50mW
Max efficiency	83.3%	N/A	85%
undershoot voltage V_{UDST}(0-1.2A)	893.75mV	680mV	N/A
undershoot time(0-1.2A)	7.4ms	22.09ms	6ms
Meeting USB Specification 1.2	Yes	No	Yes

The efficiency in the CV mode is tested and depicted in Fig. 10. Obviously, the efficiency under a low input voltage is lower than that under a high input voltage. The maximum efficiency of the CV output can reach about 83.3%.

A comparison between the proposed work with other similar technologies is shown in TABLE IV. The dynamic response capability of the method proposed in this paper and iW1760 satisfy the demand of USB Specification 1.2. However, the method proposed in [15] does not. The undershoot time of [15] is too large at almost 22ms. The method in [15] and this work adopt analog technology. However, iW1760 adopts digital technology. The circuit structure of iW1760 is too complex and the cost is much higher than that of the proposed work, which indicates that the proposed rapid dynamic response converter has good prospects.

V. CONCLUSIONS

A rapid dynamic response AC-DC CV converter based on digital assistant technology is designed in this paper. The system adopts a flyback structure, omitting the optical coupler and a precise voltage source. It also reduces both the size and cost. A digital compensation module is proposed to dynamically adjust the switching pulse width for the sake of good dynamic response capability. The control IC is implemented based on a NEC 1μm 5V/40V HVCMOS process, and a 5V/1.2A prototype has been built to verify the proposed control method. The minimum output voltage can be kept above 4.16V and the undershoot time is only 7.4ms when the load jumps from idle to a heavy load, which meets application requirements.

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