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H-type Structural Boost Three-Level DC-DC Converter with Wide Voltage-Gain Range for Fuel Cell Applications

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Abstract

To match the dynamic lower voltage of a fuel cell stack and the required constant higher voltage (400V) of a DC bus, an H-type structural Boost three-level DC-DC converter with a wide voltage-gain range (HS-BTL) is presented in this paper. When compared with the traditional flying-capacitor Boost three-level DC-DC converter, the proposed converter can obtain a higher voltage-gain and does not require a complicate control for the flying-capacitor voltage balance. Moreover, the proposed converter, which can draw a continuous and low-rippled current from an input source, has the advantages of a wide voltage-gain range and low voltage stress for power semiconductors. The operating principle, parameters design and a comparison with other converters are presented and analyzed. Experimental results are also given to verify the aforementioned characteristics and theoretical analysis. The proposed converter is suitable for application of fuel cell systems.

Key words: Boost three-level DC-DC converter, Fuel cell systems, H-type structural, Voltage stress, Wide voltage-gain range

I. INTRODUCTION

With the shortage of global energy and movements for environmental protection, clean energy sources such as fuel cells are becoming increasingly important worldwide [1]. Due to their low output voltage, high output current [2] and soft output characteristic [3], fuel cells need a step-up DC-DC converter with a wide range of voltage-gain to interface with a DC bus. In addition, ripples in input current of a converter must be low enough to extend the service life of a fuel cell [4]. In [5], a Nexa proton-exchange membrane (PEM) power module was used to demonstrate a wide range of changes in the fuel cell output voltage by theoretical calculations and experiments. Fig. 1 shows the relationship between the fuel cell output current I_F and the output voltage V_F. It can be seen that the output voltage V_F of a fuel cell decreases rapidly with an increase of the output current I_F. However, this characteristic is not beneficial for fuel cell systems unless the wide output voltage range of the fuel cell source can be converted by a wide input-voltage range boost DC–DC converter, obtaining a fairly constant dc bus voltage. Theoretically, the classical Boost converter can achieve a high voltage-gain as long as the duty cycle is large enough. However, the maximum duty cycle is limited due to parasitic resistances and the consideration of system stability. Nowadays, diodes and switches that are economic, efficient and high-voltage-stressed are still unavailable. Therefore, the voltage gain of the traditional boost converter is limited in practice, and cannot meet practical needs [6]-[9].

Some existing isolated converters, such as active-clamp dual boost converters and active-clamp full-bridge boost converters [10], [11], can realize high efficiency and a high voltage-gain. However, their start-up operations must be considered separately. Moreover, the cost is increased for many of the extra power components and isolated sensors or feedback controllers are required. From the viewpoint of system cost savings and improved system efficiency, a non-isolated DC-DC converter is more suitable for renewable or clean energy applications [12], [13].

A lot of the existing non-isolated topologies can achieve a high voltage-gain as stated in [14]. Coupled inductor-based converters can achieve a high voltage-gain [15]-[17]. However, the input current ripple of single-stage single-phase-coupled

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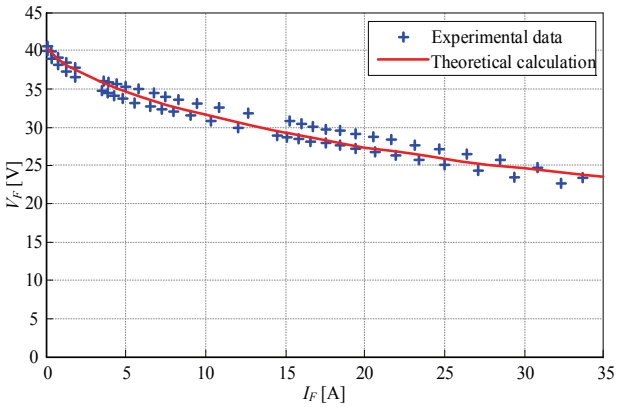


Fig. 1. Fuel cell stack polarization curve.

inductor-based converters is relatively large, which may shorten the service life of the input source [18]. The voltage stress of the power semiconductors in the Boost three-level DC-DC converter in [19] can be reduced by half the output voltage. However, its voltage-gain is limited. In addition, the output and input sides of this converter are connected by a diode, and the voltage potential difference between the two sides contains high frequency PWM signals, which may cause maintenance issues and EMI problems. The output and input sides of the Boost three-level DC-DC converter in [20] share a common ground. However, the voltage-gain of this converter is still limited. In addition, the flying-capacitor voltage requires a complex control to achieve balance. The converter in [21], which applied a switched-inductor structure, can achieve a high voltage-gain. However, a diode in the converter suffers from the high voltage stress. Similarly, high step-up DC-DC converters with switched capacitor have been proposed in [22]-[25], which can provide any voltage gain.

Z-source and quasi-Z-source networks can be applied to DC-DC power converter to protect devices in case of a short circuit [26]. A quasi-Z-source DC-DC converter with the voltage-lift technique has been proposed in [27], where a voltage-lift cell is combined with a quasi-Z-source network. The voltage gain is significantly improved. However, the range of duty cycle decreases. In [28], a common grounded Z source DC-DC converter with a high voltage-gain was presented by changing the connection method of the input source and the load. It is shown in [28] that the voltage stress of power semiconductors is reduced in the range of half of the output voltage to nearly the output voltage, when increasing the duty cycle (voltage-gain). In addition, the current stress of the power switch is several times higher than the output current while increasing the duty cycle. In [29], a Z-source DC-DC converter with a cascaded switched-capacitor was presented, where the voltage-gain can be improved by using the voltage multiplier function of the switched-capacitor. However, EMI problems can be increased since the input current is discontinuous, and the input voltage source side and the load side are not common grounded. Additional safety issues can also be induced. In [30], the advantages of a Boost three-level DC-DC converter with a diode rectification quasi-Z source are reflected in the lower voltage stress for the power semiconductors and the fact that the voltage of the flying-capacitor can be well clamped at half of the output voltage in both the static and dynamic states. However, it has disadvantages such as its narrow duty cycle range. In addition, the volume and weight of the aforementioned converter are increased for the Z-source or quasi-Z-source networks. Furthermore, it requires two or more inductors and capacitors.

The DC-DC converters just described could not provide a low input current ripple, a high voltage-gain, a low voltage stress of the power semiconductors and a simple control at the same time. In this paper, a H-type structural Boost three-level DC-DC converter with a wide voltage-gain range is proposed as a solution. This converter can reduce the voltage stresses of all the semiconductors to half of output voltage. In addition, it operates well with a high voltage-gain and a proper duty cycle ($0<d<0.5$). The output-input potential difference of this converter is a constant capacitor voltage rather than a high frequency PWM voltage. In addition, the equivalent frequency of the inductor current in this topology is double the switching frequency, with switches that are driven by two gate signals phase-shifted by 180°. These features are beneficial for improving efficiency and reducing the input current ripple.

This paper is organized as follows. In *Section II*, the topology of the HS-BTL for renewable and clean energy sources is presented and the operation principles of the converter topology are discussed. In *Section III*, the parameters for all of the components are designed, and a comparison with other converters is analyzed. Then experimental results obtained from a prototype are analyzed in *Section IV*. Finally, some conclusions are presented in *Section V*.

II. Operating Principles of the Proposed Converter

A. Configuration of the Proposed Converter

The configuration of the proposed converter is depicted in Fig. 2. With a simple structure, the proposed converter consists of an H-type structural (Q_1, Q_2, C_1, D_1 and D_2), an inductor L, two diodes D_3 and D_4, and two filter capacitors C_2 and C_3. The H-type structure is adopted at the input voltage side to reduce the input current ripple, to avoid the narrow pulse of PWM voltage waveforms, and to decrease the conduction losses of the power switches. The two filter capacitors at the output side are connected in series to obtain a high voltage-gain and to decrease the voltage stress for all of the power semiconductors and capacitors.

To simplify the analysis, the following assumptions are made.

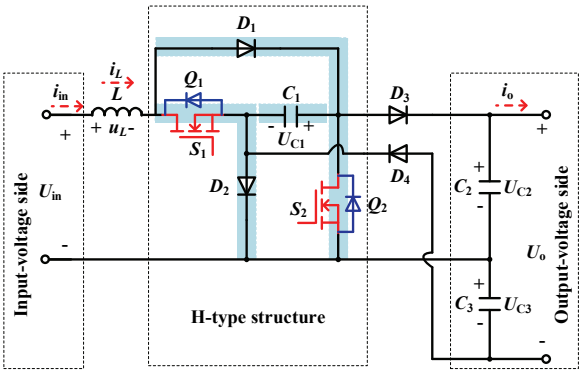


Fig. 2. Configuration of the proposed converter.

1) All of the components are ideal.
2) The capacitors in the converter are large enough so that their voltages are approximately constant, and C_1=C_2=C_3.
3) The current of L changes linearly.

B. Operating Principles

The operating principles of the proposed converter are analyzed when the input current is continuous. In this case, suppose that d_1=d_2=d, where d_1 and d_2 are the duty cycles of Q_1 and Q_2, respectively. In addition, the phase difference between their gate driving signals is 180°. According to the operation of Q_1 and Q_2, there are four switching states "S_1S_2"= {00, 01, 10, 11}, where "1" means that the power switch Q_1 or Q_2 is "*ON*", and "0" means that it is "*OFF*". It can be seen from Fig. 2 that either Q_1 or Q_2 is on for 0.5≤d<1. Therefore, the inductor L is always being charged. As a result, the duty cycle of this converter is limited to the range of 0<d<0.5. Thus, during one switching period, the converter has three switching states, and their sequence is "10-00-01-00-10". Main waveforms of the proposed converter are shown in Fig. 3, while the energy flow paths in each of the switching states of the converter are shown in Fig. 4.

When S_1S_2=10, as shown in Fig. 4(a), S_1 is in the *ON* state and S_2 is in the *OFF* state. The diodes D_2 and D_3 are directly polarized, while D_1 and D_4 are inversely polarized. The inductor L is charged with a linearly rising current i_L from the input source. The capacitor C_2 is charged by C_1. The load is supplied by C_1 and the output capacitor C_3. The switching state 10 refers to an operating stage.

The following equations can be derived in state 10:

$$\begin{cases} U_{in} = u_{L_a} = L\dfrac{di_{L_a}}{dt} \\ C_1\dfrac{du_{C_{1a}}}{dt} + C_2\dfrac{du_{C_{2a}}}{dt} = -\dfrac{u_{o_a}}{R} \\ C_3\dfrac{du_{C_{3a}}}{dt} = -\dfrac{u_{o_a}}{R} \end{cases} \tag{1}$$

$$\begin{cases} u_{o_a} = u_{C_{2a}} + u_{C_{3a}} \\ u_{C_{1a}} = u_{C_{2a}} \end{cases} \tag{2}$$

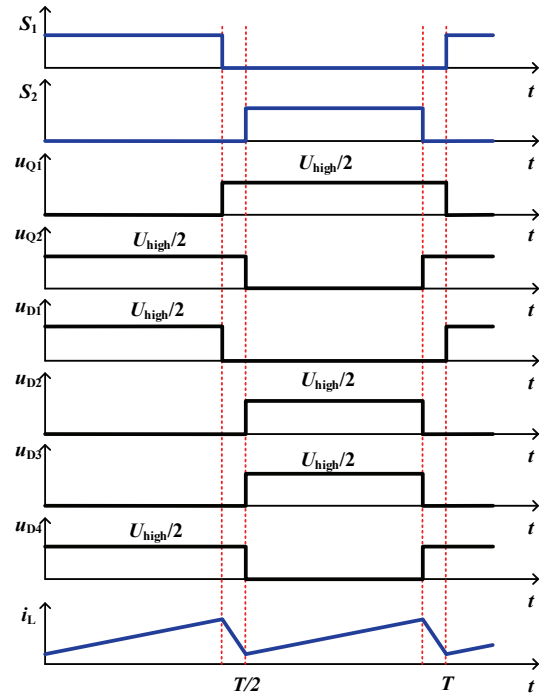


Fig. 3. Main waveforms of the proposed converter.

where U_{in} is the input voltage, u_{L_a} and i_{L_a} are the voltage and current of the inductor, and $u_{C_{1a}}$, $u_{C_{2a}}$ and $u_{C_{3a}}$ are the voltages over C_1, C_2 and C_3. In addition, u_{o_a} is the output voltage and R is the load resistor. The subscript 'a' indicates a variable in state 10.

When S_1S_2=00, as shown in Fig. 4(b), both of the switches S_1 and S_2 are *OFF*. The diodes D_1, D_2 and D_3 are directly polarized, while D_4 is inversely polarized. The current of the inductor decrease linearly, C_1 is charged from L, and the load is supplied by L and C_3. The switching state 00 refers to an operating stage.

The following equations can be derived in state 00:

$$\begin{cases} u_{L_b} = U_{in} - u_{C_{1b}} = L\dfrac{di_{L_b}}{dt} \\ i_{L_b} - C_1\dfrac{du_{C_{1b}}}{dt} - \dfrac{u_{o_b}}{R} = C_2\dfrac{du_{C_{2b}}}{dt} \\ C_3\dfrac{du_{C_{3b}}}{dt} = -\dfrac{u_{o_b}}{R} \end{cases} \tag{3}$$

$$\begin{cases} u_{o_b} = u_{C_{2b}} + u_{C_{3b}} \\ u_{C_{1b}} = u_{C_{2b}} \end{cases} \tag{4}$$

where U_{in} is the input voltage, u_{L_b} and i_{L_b} are voltage and current of the inductor, and $u_{C_{1b}}$, $u_{C_{2b}}$ and $u_{C_{3b}}$ are the voltages over C_1, C_2 and C_3. In addition, u_{o_b} is the output voltage and R is the load resistor. The subscript 'b' indicates a variable in state 00.

When S_1S_2=01, as shown in Fig. 4(c), S_1 is *OFF* and S_2 is *ON*. The diodes D_1 and D_4 are directly polarized, while D_2 and D_3 are inversely polarized. The inductor L is charged

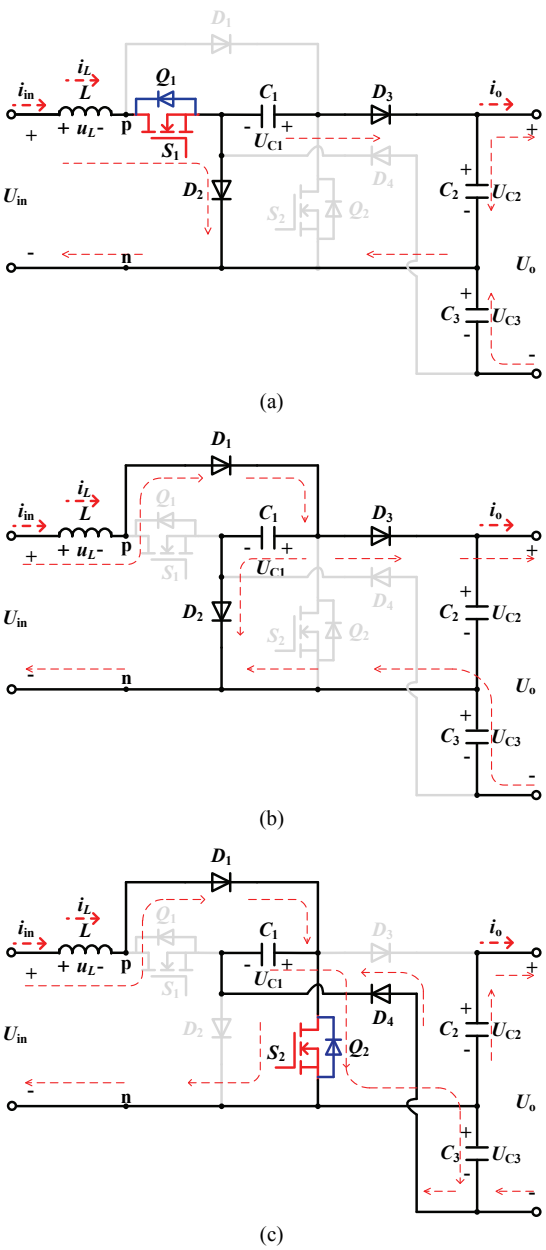


Fig. 4. Energy flow paths in each switching state: (a) S_1S_2=10, (b) S_1S_2=00, (c) S_1S_2=01.

from the input source. The current i_L rises linearly. The capacitor C_3 is charged from C_1. The current of D_4 is limited by the parasitic resistance of the converter. The load is supplied by the output capacitor C_2. Switching state 01 refers to an operating stage.

The following equations can be derived in state 01:

$$\begin{cases} U_{in} = u_{L_c} = L\dfrac{di_{L_c}}{dt} \\ C_1\dfrac{du_{C_{1c}}}{dt} + C_3\dfrac{du_{C_{3c}}}{dt} = -\dfrac{u_{o_c}}{R} \\ C_2\dfrac{du_{C_{2c}}}{dt} = -\dfrac{u_{o_c}}{R} \end{cases} \tag{5}$$

$$\begin{cases} u_{o_c} = u_{C_{2c}} + u_{C_{3c}} \\ u_{C_{1c}} = u_{C_{3c}} \end{cases} \tag{6}$$

where U_{in} is the input voltage, u_{L_c} and i_{L_c} are voltage and current of the inductor, and $u_{C_{1c}}$, $u_{C_{2c}}$, and $u_{C_{3c}}$ are the voltages over C_1, C_2 and C_3. In addition, u_{o_c} is the output voltage and R is the load resistor. The subscript 'c' indicates a variable in state 01.

C. Steady-State Analysis

1) Voltage Gain

For the sake of simplicity, the circuit performance of the proposed converter in the CCM will be analyzed with the same assumptions as stated in the previous section. The approximately constant voltages across C_1, C_2 and C_3 are denoted as U_{C1}, U_{C2} and U_{C3}, and the approximately constant output voltage is denoted as U_o. These constant voltages can be obtained from (2), (4) and (6), as follows:

$$\begin{cases} U_{C1} = U_{C2} = U_{C3} \\ U_o = 2U_{C1} = 2U_{C2} = 2U_{C3} \end{cases} \tag{7}$$

then the voltage u_{L_b} is:

$$u_{L_b} = U_{in} - \frac{1}{2}U_o \tag{8}$$

Applying the volt-second balance principle to the inductor L in the CCM yields:

$$\int_0^{dT} u_{L_a}dt + \int_{dT}^{0.5T} u_{L_b}dt + \int_{0.5T}^{(1+2d)T/2} u_{L_c}dt + \int_{(1+2d)T/2}^{T} u_{L_b}dt = 0 \tag{9}$$

From (1), (5), (8) and (9) the following is obtained:

$$U_o = \frac{2}{1\text{-}2d} \times U_{in} \tag{10}$$

Thus, the voltage-gain M of the proposed converter can be expressed as:

$$M = \frac{2}{1\text{-}2d} \tag{11}$$

where $0<d<0.5$. The proposed converter can obtain a high-voltage gain with a small duty cycle, which brings a lot of advantages:

a. If the duty cycle is varied within a wider region of 0 to 1, when a high-step-up voltage gain is required, a larger duty cycle should be used. The use of a larger duty cycle results in high conduction losses on the switches [23]. The proposed converter can obtain a high-voltage gain with a small duty cycle, which decreases the conduction losses on the power switches. During one switching period, the converter has four operating stages, and their switching state sequence is "10-00-01-00". However, during one switching period, all of the power semiconductors just make a connection and break once, which does not increase the switching losses or the reverse recovery losses.

b. The connections and breaks of power semiconductors all need a little time. Thus, the narrow pulse of an ideal PWM voltage waveform is difficult to realize. The proposed converter can obtain a higher voltage gain when the duty cycle is closer to 0.5, resulting in a closer time for all of the power semiconductors to turn on and off. This feature is beneficial for avoiding the narrow pulse of the PWM voltage waveforms when a high voltage gain is achieved.

2) The Average Inductor Current and Inductor Current Ripple

Applying the ampere-second balance principle to the capacitors C_1, C_2 and C_3 in the CCM yields:

$$\begin{cases} \int_0^{dT} C_1 \frac{du_{C_{1a}}}{dt} dt + \int_{dT}^{0.5T} C_1 \frac{du_{C_{1b}}}{dt} dt + \\ \int_{0.5T}^{(1+2d)T/2} C_1 \frac{du_{C_{1c}}}{dt} dt + \int_{(1+2d)T/2}^{T} C_1 \frac{du_{C_{1b}}}{dt} dt = 0 \\ \int_0^{dT} C_2 \frac{du_{C_{2a}}}{dt} dt + \int_{dT}^{0.5T} C_2 \frac{du_{C_{2b}}}{dt} dt + \\ \int_{0.5T}^{(1+2d)T/2} C_2 \frac{du_{C_{2c}}}{dt} dt + \int_{(1+2d)T/2}^{T} C_2 \frac{du_{C_{2b}}}{dt} dt = 0 \\ \int_0^{dT} C_3 \frac{du_{C_{3a}}}{dt} dt + \int_{dT}^{0.5T} C_3 \frac{du_{C_{3b}}}{dt} dt + \\ \int_{0.5T}^{(1+2d)T/2} C_3 \frac{du_{C_{3c}}}{dt} dt + \int_{(1+2d)T/2}^{T} C_3 \frac{du_{C_{3b}}}{dt} dt = 0 \end{cases} \tag{12}$$

From (1), (3), (5) and (12), the average inductor current I_L is given by:

$$I_L = \frac{2}{1\text{-}2d} \times \frac{U_o}{R} \tag{13}$$

In state 10, the inductor current increase linearly. Therefore:

$$\begin{aligned} & i_{L(dT)} = i_{L(0)} + \frac{1}{L}\int_0^{dT} u_L(t)dt \\ & \Rightarrow \Delta i_L = \frac{1}{L}\int_0^{dT} u_L(t)dt = \frac{1}{L}\int_0^{dT} u_{L_a} dt = \frac{1}{L}\int_0^{dT} U_{in} dt \\ & \Rightarrow \Delta i_L = \frac{d \times U_{in}}{Lf} \end{aligned} \tag{14}$$

where f is the switching frequency and Δi_L is the inductor current ripple.

From (13) and (14), the current ripple ratio r of the inductor can be obtained as:

$$r = \frac{\Delta i_L}{I_L} = \frac{d(1-2d)^2 \times R}{4Lf} \tag{15}$$

The current ripple ratio r' of the classical Boost converter is:

$$r' = \frac{d'(1-d')^2 \times R}{Lf} \tag{16}$$

where d' is the duty cycle of the converter.

If the proposed converter and the classical Boost converter have the same output power, inductor and switching frequency, it can be obtained that:

$$\frac{r}{r'} = \frac{(M-2)}{2(M-1)} \tag{17}$$

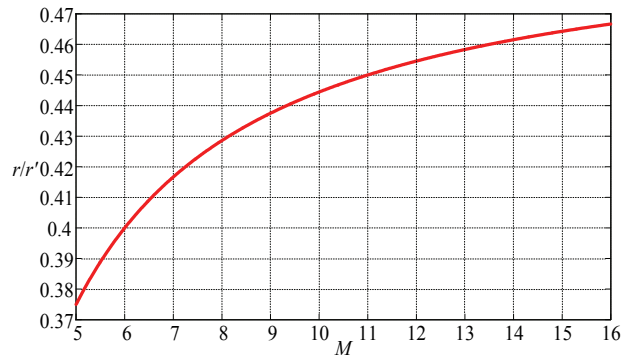


Fig. 5. Ratio of the inductor current ripple ratio versus the wider voltage-gain range from 5 to 16.

It can be seen from Fig. 5 that inductor current ripple ratio in the proposed converter is lower than that in the classical Boost converter, which means a lower input current ripple.

3) Voltage Stresses on the Semiconductor Components

From Fig. 4, the voltages of the power semiconductors are given by:

$$\begin{cases} U_{Q2} = U_{D1} = U_{C1} = \frac{1}{2}U_o \\ U_{D3} = U_{D4} = U_o - U_{C1} = \frac{1}{2}U_o \\ U_{Q1} = U_{D2} = U_{C1} = \frac{1}{2}U_o \end{cases} \tag{18}$$

It means that the voltage stress for all of the power semiconductors is only half of the output voltage.

D. Small-Signal Modeling and Voltage Mode Control

When the proposed converter operates in the range of $0<d<0.5$, the main power semiconductors Q_1 and Q_2 have three effective switching states: S_1S_2= [10, 00, 01]. u_{in}, u_o and d are the input variable, the output variable and the control variable, respectively. i_L, u_{C1}, u_{C2} and u_{C3} are the state variables. When S_1S_2=10, the converter operates in state 10 (as shown in Fig. 4(a)), and its operating time is $d\times T$. Thus, the state space average model can be obtained as follows:

$$\begin{cases} \begin{bmatrix} \dot{i}_L \\ \dot{u}_{C_1} \\ \dot{u}_{C_2} \\ \dot{u}_{C_3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1 r} & \frac{1}{C_1 r} & 0 \\ 0 & \frac{1}{C_2 r} & -\frac{1}{C_2 R} - \frac{1}{C_2 r} & -\frac{1}{C_2 R} \\ 0 & 0 & -\frac{1}{C_3 R} & -\frac{1}{C_3 R} \end{bmatrix} \begin{bmatrix} i_L \\ u_{C_1} \\ u_{C_2} \\ u_{C_3} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{in} \\ u_o = \begin{bmatrix} 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_L & u_{C_1} & u_{C2} & u_{C_3} \end{bmatrix}^T \end{cases} \tag{19}$$

When S_1S_2=00, the converter is operating in state 00 (as shown in Fig. 4(b)), and its operating time is $(1\text{-}2d)\times T$. The state space average model can be written as:

$$\begin{cases} \begin{bmatrix} \dot{i}_L \\ \dot{u}_{C_1} \\ \dot{u}_{C_2} \\ \dot{u}_{C_3} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{1}{C_1 r} & \frac{1}{C_1 r} & 0 \\ \frac{1}{C_2} & \frac{1}{C_2 r} & -\frac{1}{C_2 R}-\frac{1}{C_2 r} & -\frac{1}{C_2 R} \\ 0 & 0 & -\frac{1}{C_3 R} & -\frac{1}{C_3 R} \end{bmatrix} \begin{bmatrix} i_L \\ u_{C_1} \\ u_{C_2} \\ u_{C_3} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{in} \\ u_o = \begin{bmatrix} 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_L & u_{C_1} & u_{C2} & u_{C_3} \end{bmatrix}^T \end{cases} \tag{20}$$

When S_1S_2=01, the converter operates in state 01 (as shown in Fig. 4(c)), and its operating time is $d\times T$. The state space average model can be achieved as:

$$\begin{cases} \begin{bmatrix} \dot{i}_L \\ \dot{u}_{C_1} \\ \dot{u}_{C_2} \\ \dot{u}_{C_3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1 r} & 0 & \frac{1}{C_1 r} \\ 0 & 0 & -\frac{1}{C_2 R} & -\frac{1}{C_2 R} \\ 0 & \frac{1}{C_3 r} & -\frac{1}{C_3 r} & -\frac{1}{C_3 R}-\frac{1}{C_3 r} \end{bmatrix} \begin{bmatrix} i_L \\ u_{C_1} \\ u_{C_2} \\ u_{C_3} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{in} \\ u_o = \begin{bmatrix} 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_L & u_{C_1} & u_{C2} & u_{C_3} \end{bmatrix}^T \end{cases} \tag{21}$$

Combining (19) and (20) with (21), the average model of the converter can be obtained as:

$$\begin{cases} \begin{bmatrix} \dot{i}_L \\ \dot{u}_{C_1} \\ \dot{u}_{C_2} \\ \dot{u}_{C_3} \end{bmatrix} = \begin{bmatrix} 0 & \frac{2d-1}{L} & 0 & 0 \\ 0 & -\frac{1}{C_1 r} & \frac{1-d}{C_1 r} & \frac{d}{C_1 r} \\ \frac{1-2d}{C_2} & \frac{1-d}{C_2 r} & -\frac{1}{C_2 R}-\frac{1-d}{C_2 r} & -\frac{1}{C_2 R} \\ 0 & \frac{d}{C_3 r} & -\frac{1}{C_3 R} & -\frac{1}{C_3 R}-\frac{d}{C_3 r} \end{bmatrix} \begin{bmatrix} i_L \\ u_{C_1} \\ u_{C_2} \\ u_{C_3} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{in} \\ u_o = \begin{bmatrix} 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_L & u_{C_1} & u_{C2} & u_{C_3} \end{bmatrix}^T \end{cases} \tag{22}$$

The state variables, the input variable, the output variable and the control variable can be described by using the small-signal disturbance variables as:

$$\begin{cases} i_L = I_L + \hat{i}_L \\ u_{Cx} = U_{Cx} + \hat{u}_{Cx} \\ u_o = U_o + \hat{u}_o \\ u_{in} = U_{in} + \hat{u}_{in} \\ d = D + \hat{d} \end{cases} \tag{23}$$

where I_L, U_{Cx}, U_{in}, U_o and D are steady state components, $\hat{i}_L$, $\hat{u}_{Cx}$, $\hat{u}_{in}$, $\hat{u}_o$ and $\hat{d}$ are their corresponding small-signal disturbance variables, and r is the equivalent series resistance for C_1. The subscript 'x' indicates 1, 2 and 3.

As a result, the small-signal model of the proposed converter is:

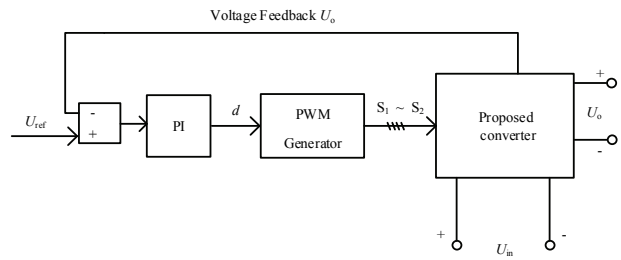


Fig. 6. Voltage mode control of the proposed converter.

$$\begin{bmatrix} \dot{\hat{i}}_L \\ \dot{\hat{u}}_{C_1} \\ \dot{\hat{u}}_{C_2} \\ \dot{\hat{u}}_{C_3} \end{bmatrix} = \begin{bmatrix} 0 & \frac{2D-1}{L} & 0 & 0 \\ 0 & -\frac{1}{C_1 r} & \frac{1-D}{C_1 r} & \frac{D}{C_1 r} \\ \frac{1-2D}{C_2} & \frac{1-D}{C_2 r} & -\frac{1}{C_2 R}-\frac{1-D}{C_2 r} & -\frac{1}{C_2 R} \\ 0 & \frac{D}{C_3 r} & -\frac{1}{C_3 R} & -\frac{1}{C_3 R}-\frac{D}{C_3 r} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{u}_{C_1} \\ \hat{u}_{C_2} \\ \hat{u}_{C_3} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{u}_{in} + \begin{bmatrix} 0 & \frac{2}{L} & 0 & 0 \\ 0 & 0 & -\frac{1}{C_1 r} & \frac{1}{C_1 r} \\ -\frac{2}{C_2} & -\frac{1}{C_2 r} & \frac{1}{C_2 r} & 0 \\ 0 & \frac{1}{C_3 r} & 0 & -\frac{1}{C_3 r} \end{bmatrix} \begin{bmatrix} I_L \\ U_{C_1} \\ U_{C_2} \\ U_{C_3} \end{bmatrix} \hat{d}$$
$$\hat{u}_o = \begin{bmatrix} 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_L & \hat{u}_{C_1} & \hat{u}_{C_2} & \hat{u}_{C_3} \end{bmatrix}^T \tag{24}$$

According to (24) and the experimental parameters in Table II, when the input voltage is U_{in}=25V, the control-to-output transfer function can be achieved from the time domain to the complex frequency domain as:

$$\begin{aligned} G_C &= \left. \frac{\hat{u}_o(s)}{\hat{d}(s)} \right|_{\hat{u}_{in}(s)=0} \\ &= \frac{-1.23\times10^5 s^3 + 2.4\times10^8 s^2 + 4.2\times10^{12} s + 6.72\times10^{15}}{s^4 + 7.7\times10^3 s^3 + 1.1\times10^7 s^2 + 7.45\times10^8 s + 10^{12}} \end{aligned} \tag{25}$$

The small-signal model derived above is helpful for the design of the controller. For a fuel cell power system, the converter must be able to provide a stable output voltage despite a varying input voltage. Therefore, a voltage mode control based on the developed small-signal model is adopted. As shown in Fig. 6, a PI regulator is used to stabilize the output voltage. According to the small-signal model, the parameters of the PI regulator can be determined.

III. PARAMETERS DESIGN

A. Parameter Design of an Inductor

As shown in Fig. 7, when the minimum value of the inductor current i_{Lmin} is greater than 0, the converter operates in the CCM. When i_{Lmin} is equal to 0, the converter operates in the boundary conduction mode (BCM). When i_{Lmin} is less than 0, the converter operates in the discontinuous conduction mode (DCM). The converter in this paper is used to interface

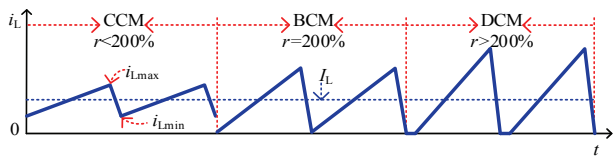


Fig. 7. Converter operating mode.

a fuel cell stack. In order to allow the fuel cell stack to output a continuous current, this converter should operate in the CCM.

The inductor current ripple ratio r can be calculated by (26).

$$r=\frac{i_{L\max}-i_{L\min}}{I_L}=\frac{\Delta i_L}{I_L} \tag{26}$$

where i_{Lmax} is the maximum value of the inductor current. When the converter operates in the BCM, r is equal to 200%.

$$r=\frac{i_{L\max}-i_{L\min}}{I_L}=\frac{i_{L\max}-0}{I_L}=\frac{2I_L}{I_L}=200\% \tag{27}$$

Therefore, when the converter operates in the CCM, r should not be more than 200%. The parameters design of the inductor depends on the permitted inductor current ripple ratio r, the nominal input voltage U_{in}, the nominal output voltage U_o, the nominal load resistor and the switching frequency f. According to (15), the inductance L can be expressed as:

$$L\geq\frac{d(1-2d)^2\times R}{8f} \tag{28}$$

When the proposed converter is operated, the input voltage is between 25-70V, the output voltage is 400V, and the output power is 400W. At this time, the corresponding duty ratio d is between 0.325 and 0.4375. According to (28), the value of L is at its maximum when d is 0.325. In other words, when the voltage gain is at its lowest, the inductance of L required by the converter is maximized. As long as the inductor current is still continuous in this case, the converters always operates in the CCM. In this case, the inductance of L is:

$$L=\frac{d(1-2d)^2\times R}{8f}=\frac{0.325(1-2\times0.325)^2\times400\Omega}{8\times20\times10^3Hz}=99.5uH \tag{29}$$

In order to avoid a large inductor current ripple at a light load of the converter as much as possible, considering a margin, the selected inductor value is 118uH.

At the rated power, according to (15), when the voltage gain is 16, the inductor current ripple ratio r is:

$$r=\frac{i_{L\max}-i_{L\min}}{I_L}=\frac{\Delta i_L}{I_L}=\frac{d(1-2d)^2\times R}{4Lf}=28.97\% \tag{30}$$

B. Parameter Design of Capacitors

Assume that the voltages of C_1, C_2 and C_3 increase or decrease linearly. From (1), (3), (5) and (12) the following is obtained:

$$\begin{cases} C_1\dfrac{du_{C_{1a}}}{dt}=-2\times\dfrac{U_o}{R}, & C_1\dfrac{du_{C_{1b}}}{dt}=\dfrac{1+2d}{1-2d}\times\dfrac{U_o}{R}, \\ C_1\dfrac{du_{C_{1c}}}{dt}=-\dfrac{1}{d}\times\dfrac{U_o}{R} & \\ C_2\dfrac{du_{C_{2a}}}{dt}=\dfrac{U_o}{R}, & C_2\dfrac{du_{C_{2b}}}{dt}=0 \\ C_2\dfrac{du_{C_{2c}}}{dt}=-\dfrac{U_o}{R} & \\ C_3\dfrac{du_{C_{3a}}}{dt}=-\dfrac{U_o}{R}, & C_3\dfrac{du_{C_{3b}}}{dt}=-\dfrac{U_o}{R}, \\ C_3\dfrac{du_{C_{3c}}}{dt}=\dfrac{1-d}{d}\times\dfrac{U_o}{R} & \end{cases} \tag{31}$$

When the current into the capacitor is positive, the capacitor voltage increases linearly, and vice versa. The capacitance mainly depends on Δu, which is the permitted fluctuation range of the capacitor voltage. Thus:

$$\begin{cases} \Delta u_1\times C_1\geq(\dfrac{1}{2}-d)\times T\times\dfrac{1+2d}{1-2d}\times\dfrac{U_o}{R} \\ \Delta u_2\times C_2\geq d\times T\times\dfrac{U_o}{R} \\ \Delta u_3\times C_3\geq d\times T\times\dfrac{1-d}{d}\times\dfrac{U_o}{R} \end{cases} \tag{32}$$

where Δu_1-Δu_3 are the voltage ripples of C_1-C_3, respectively.

The output voltage ripple Δu_o is affected by the capacitors C_2 and C_3. Therefore, the output voltage ripple can be expressed as:

$$\Delta u_o=\Delta u_2+\Delta u_3 \tag{33}$$

In order to facilitate the later maintenance, capacitors of equal capacitance are selected, that is C_1=C_2=C_3=C. From (31), it can be seen that in switching state 10, the currents flowing through the capacitors C_2 and C_3 have the same magnitude but opposite directions. The output voltage is almost constant. In switching state 00, the capacitor C_2 is neither charged nor discharged, and the capacitor C_3 is discharged. The output voltage decreases linearly. In switching state 01, C_2 is discharged and C_3 is charged. However, the charging speed of C_3 is greater than the discharging speed of C_2. Therefore, the output voltage increases linearly. The voltage ripples of C_2 and C_3 and the ripple of the output voltage are shown in Fig. 8. The output voltage ripple can be calculated in switch state 01.

$$\Delta u_o=d\times T\times(\frac{1-d}{d\times C_3}-\frac{1}{C_2})\times\frac{U_o}{R}=\frac{1-2d}{f\times C}\times\frac{U_o}{R} \tag{34}$$

Set Δu_o to 0.08V and calculate the capacitance C when the duty cycle d is between 0.325 and 0.4375. The output voltage ripple is at its maximum when d is 0.325. Similarly, the output voltage of the converter is 400V and the load resistance is 400Ω.

$$C=\frac{1-2d}{f\times\Delta u_o}\times\frac{U_o}{R}=\frac{1-2\times0.325}{20\times10^3Hz\times0.08V}\times\frac{400V}{400\Omega}=218.75uF \tag{35}$$

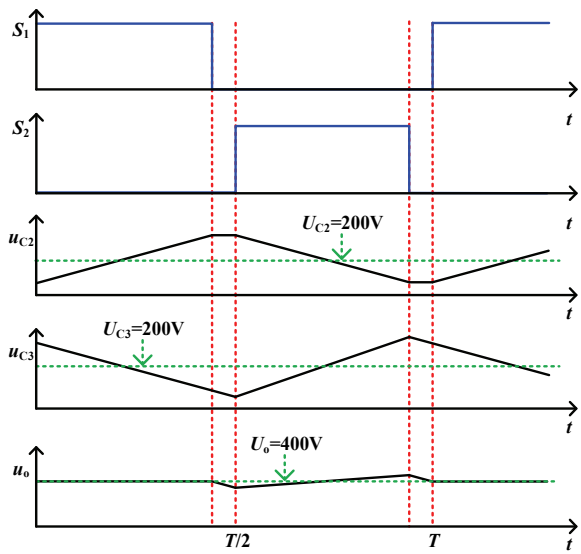


Fig. 8. Output voltage ripple of the proposed converter.

In order to avoid a large output voltage ripple at a heavy load of the converter, considering a margin, the selected capacitor value is 260uF.

When 260uF capacitors are used, the voltage ripples of C_1-C_3 can be calculated based on (32) when the duty cycle d is between 0.325 and 0.4375. When d is 0.4375, the voltage ripples of the capacitors C_1 and C_2 are at their largest, which are $\Delta u_{1\max}$ and $\Delta u_{2\max}$, respectively. When d is 0.325, the voltage ripples of the capacitor C_2 and the output voltage are at their largest, which are $\Delta u_{3\max}$ and $\Delta u_{o\max}$, respectively.

$$\begin{cases} \Delta u_{1\max} = \dfrac{1+2\times 0.4375}{2\times 20\times 10^3 Hz\times 260uF}\times\dfrac{400V}{400\Omega} = 0.180V \\ \Delta u_{2\max} = \dfrac{0.4375}{20\times 10^3 Hz\times 260uF}\times\dfrac{400V}{400\Omega} = 0.084V \\ \Delta u_{3\max} = \dfrac{1-0.325}{20\times 10^3 Hz\times 260uF}\times\dfrac{400V}{400\Omega} = 0.130V \\ \Delta u_{o\max} = \dfrac{1-2\times 0.325}{20\times 10^3 Hz\times 260uF}\times\dfrac{400V}{400\Omega} = 0.067V \end{cases} \tag{36}$$

From (36), it can be seen that when the capacitance of 260uF is selected, the voltage ripples of the capacitors C_1-C_3 and the output voltage ripple are relatively small. In addition, the largest output voltage ripple is less than the three capacitors largest voltage ripples.

C. Parameter Design of Power Switches and Diodes

For the power switches and diodes, their voltage stresses can be determined by equation (18), and their current stresses (namely the average currents in the *ON* state) can be deduced according to the energy flow paths among the voltage source, inductor and capacitors during their effective switching states as shown in Fig. 4. Therefore, from (13) and (31), the current stresses on the switches and diodes can be described as:

TABLE I
COMPARISON WITH OTHER STEP-UP SOLUTIONS

	Voltage-gain	Voltage stress for power switches	Maximum voltage stress for diodes	Inductors	Frequency
Converter in [27]	$2(1-d)/(1-2d)$	$U_o/2(1-d)$	$U_o/2(1-d)$	2	f
Converter in [28]	$(1+d)/(1-2d)$	$U_o/(1+d)$	$U_o(2-d)/(1-d)$	3	f
Converter in [29]	$2/(3-4d)$	$U_o/2$	$U_o/2$	2	$2f$
Proposed converter	$2/(1-2d)$	$U_o/2$	$U_o/2$	1	$2f$

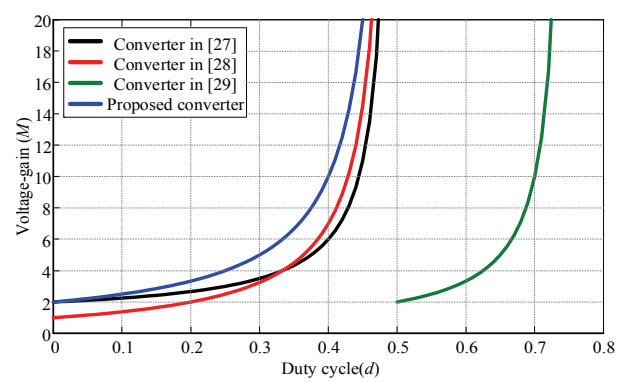


Fig. 9. Comparisons of voltage gain versus duty cycle for four types of Boost DC-DC converters.

$$\begin{cases} I_{Q1} = \dfrac{2}{1-2d}\times\dfrac{U_o}{R} \\ I_{Q2} = \dfrac{1}{d(1-2d)}\times\dfrac{U_o}{R} \\ I_{D1} = \dfrac{2}{1-2d}\times\dfrac{U_o}{R} \\ I_{D2} = (\dfrac{2}{1-2d}-\dfrac{1}{1-d})\times\dfrac{U_o}{R} \\ I_{D3} = \dfrac{1}{1-d}\times\dfrac{U_o}{R} \\ I_{D4} = \dfrac{1}{d}\times\dfrac{U_o}{R} \end{cases} \tag{37}$$

where I_{Q1}, I_{Q2}, and I_{D1}-I_{D4} are the average currents of Q_1, Q_2 and D_1-D_4 when they are in the *ON* state.

D. Comparisons with other Step-Up Solutions

The ideal voltage-gain of A three-level Boost DC-DC converter is limited due to the effects of the parasitic resistance and extreme duty cycles, where the voltage-gain is $(1/(1-d))$. Although the voltage stresses of the four semiconductors can be reduced by half the output voltage U_o, the flying-capacitor voltage requires a complex control to achieve a proper balance. Comparisons between the proposed and other step-up solutions are drawn and shown in Table I and Fig. 9. When compared with the converters in [27] and [28], the proposed converter has a higher voltage-gain. The voltage stresses of all the

semiconductors in [27] are between $U_o/2$ and U_o, e.g. $0.75U_o$, rather than $U_o/2$. The voltage stresses of all the semiconductors in [28] are also greater than $0.5U_o$. The converter in [29] presents a duty cycle limitation, since $0.5 \le d < 0.75$. The static gain variation is highly nonlinear at this operation point, where a relatively small variation in d can results in a large variation of the output voltage, which results in control problems. However, the proposed converter can simultaneously provide high voltage- gain low voltage stresses for the power semiconductors and a simple control, where the voltage-gain is $(2/(1-2d))$ with modest duty cycles in (0, 0.5), and the voltage stress is $0.5U_o$. Moreover, the equivalent frequency of the inductor current in the proposed converter is double the switching frequency, which helps reduce the volumes of the inductor and the series-connected capacitor.

IV. Experimental Results and Analyses

In order to verify the feasibility of the theoretical analysis, an experimental prototype of the proposed converter has been constructed as shown in Fig. 10. An adjustable DC source with a range of 25V-70V is used to replace the renewable and clean energy sources. The converter voltage loop is implemented by a TMS320F28335 DSP. The PWM gate signals are also generated by the DSP. The load is a resistor. The experiment parameters are shown in Table II.

With the voltage control loop, the proposed QZSS-BTL converter operates well under an output voltage of U_o =400V and an output power of P_o=400W. The output voltage U_o, the PWM voltages of the power switches Q_1 and Q_2, and the inductor current i_L with the input voltages of U_{in}=25V and U_{in}=70V are shown in Fig. 11(a) and Fig. 11(b). The inductor L is charged and discharged twice during each switching period. When the instantaneous PWM voltage of Q_1 or Q_2 is zero (S_1S_2=01 or S_1S_2=10), it is charged. When U_{Q1} and U_{Q2} stay at $U_o/2$=200V (S_1S_2=00), it is discharged. The equivalent switching frequency of the proposed converter is double the real switching frequency f. Therefore, the volumes of the series-connected capacitor and inductor can be reduced by almost half, resulting in a significant reduction in the total volume of the converter. In addition, this feature is beneficial to improve efficiency and to reduce the input current ripple.

When the converter is operated at the rated power, the PWM voltages of the power switches Q_1 and Q_2 are shown in Fig. 11, and the PWM voltages for each of the diodes with an input voltage of U_{in}=25V are shown in Fig. 12. The voltage stresses for each of the power semiconductors are slightly higher than 200V, which is about half the output voltage when the output voltage is 400V. In one switching period, the two power switches have the same duty cycle but a phase difference of 180°. The voltage stresses of the power semiconductors are concluded to be half the output voltage.

TABLE II
Experiment Parameters

Parameters	Values
Rated power P_n	400W
Series-connected capacitor C_1	260 μF
Filtering capacitors C_2 and C_3	260 μF
Inductor L	118 μH
Output voltage U_o	400 V
Input voltage U_{in}	25-70 V
Switching frequency f	20kHz
Power switches Q_1-Q_2	IXTH 88N30P (300V, 88A)
Diodes D_1-D_4	DSEC 60-03A (300V, 60A)

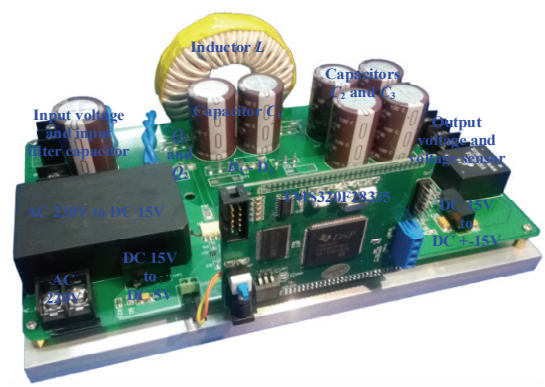


Fig. 10. Experimental prototype of the proposed converter.

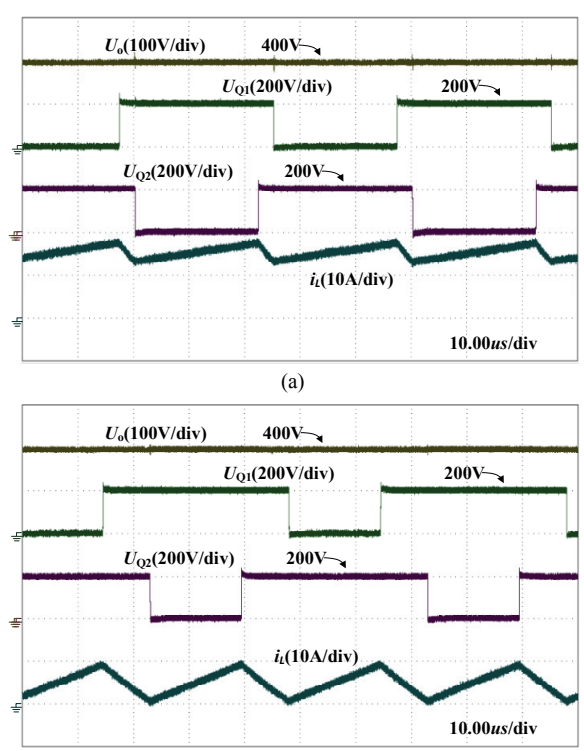
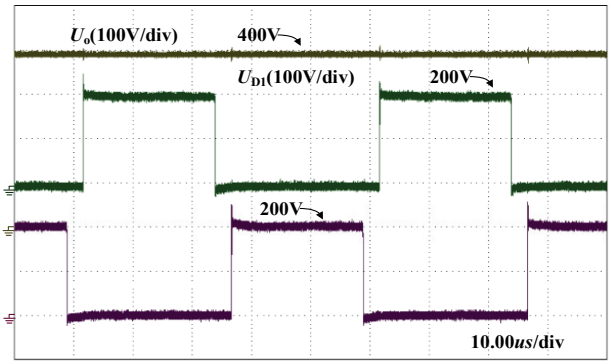
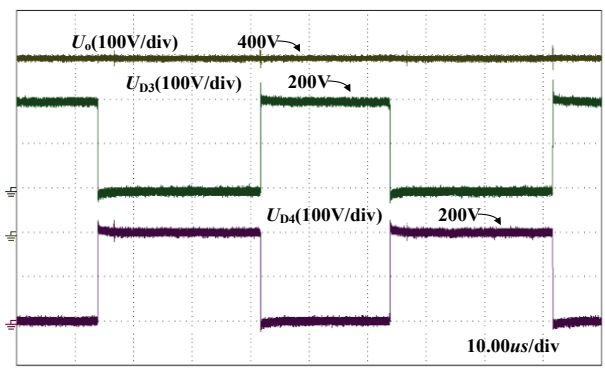


Fig. 11. Waveforms of the output voltage and PWM voltages of the power switches Q_1 and Q_2 and the inductor current: (a) Input voltage U_{in}=25V and M=16, (b) Input voltage U_{in}=70V and M=5.71.



(a)



(b)

Fig. 12. Output voltage and PWM voltages for each of the diodes with an input voltage of U_{in}=25V: (a) U_o, U_{D1} and U_{D2}, (b) U_o, U_{D3} and U_{D4}.

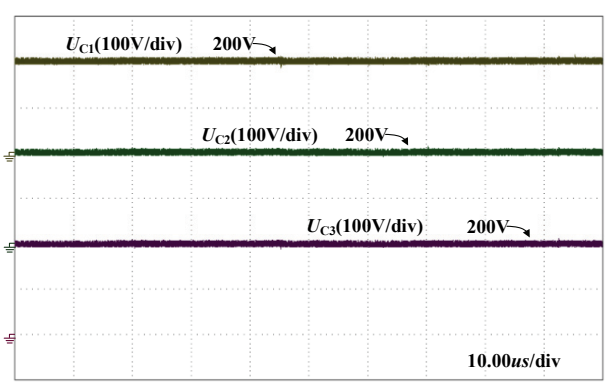


Fig. 13. Capacitors voltage stresses when U_o=400V.

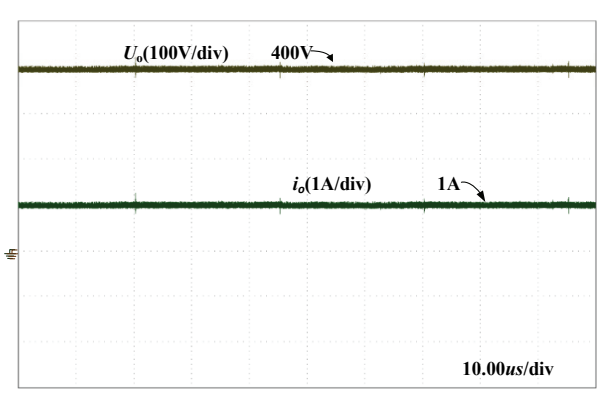


Fig. 14. Output voltage and load current.

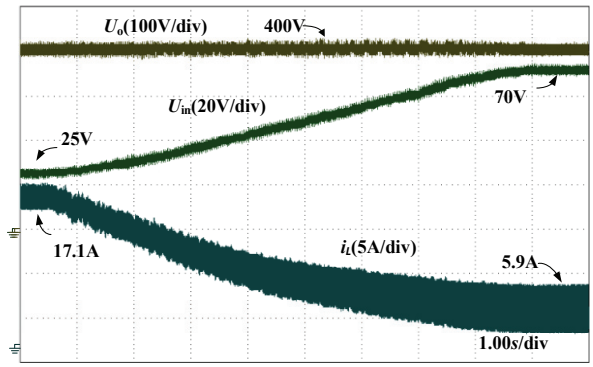


Fig. 15. Output voltage and input current with a wide-range changed input voltage from 25V to 70V in the dynamical state.

The differences between the theoretical results and the experimental results are caused by the forward voltage drop of the diodes and the ESR for each of the devices.

Fig. 13 shows voltage waveforms for all of the capacitors in the proposed converter, where the voltages across capacitors C_1, C_2 and C_3 are approximately 200V. This is consistent with the calculated values. It can be seen from Fig. 11-Fig.15 that the ripples of the capacitor voltage and output voltage are very small. This is consistent with the analysis in *Section III*.

The output voltage can stay around the reference voltage 400V with the help of a voltage control loop. The output voltage and input voltage in the dynamical state are shown in Fig. 15, where the input voltage changes gradually and widely from 25V to 70V, and the output voltage stays around 400V. As a result, the proposed converter can achieve a wide range of voltage-gain from 5.7 to 16. Correspondingly, the input current (from 17.1A to 5.9A) decreases gradually with a wide-range changed input voltage (from 25V to 70V), as shown in Fig.15. The proposed converter can operate well in a wide voltage gain range (from 5.71 to 16). Correspondingly, the duty cycles are change from 0.325 to 0.4375, which avoid extreme duty cycles.

For the wide input-voltage range operation of the proposed converter, the conversion efficiencies related to the variable input voltages (e.g. 25V, 30V, …, 55V, 60V) and the different output powers (e.g. 300W, 400W, 500W) are measured by a Power Analyzer (Yokogawa-WT3000). Then the relationship between the efficiency, the variable input voltages and the different output powers are illustrated in Fig. 16. It is noticed that the minimum efficiency is 91.80%, while the voltage-gain is 16 and the output power is 500W.

The maximum efficiency is 95.28%, while the voltage-gain is 6.67 and the output power is 500W. In addition, when the output power is constant and the input voltage declines, the efficiency also decreases. This is due to the increasing losses caused by the growing input current.

The calculated loss distribution for the experiment when U_{in}=25V and P_n=400W is shown in Fig. 17. The total loss of the converter is 30.06W, 40.91% of which is the turn-on and

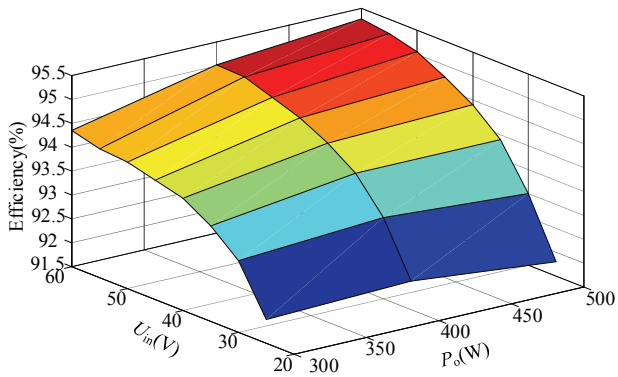


Fig. 16. Efficiencies with different output powers when the output voltage is 400V.

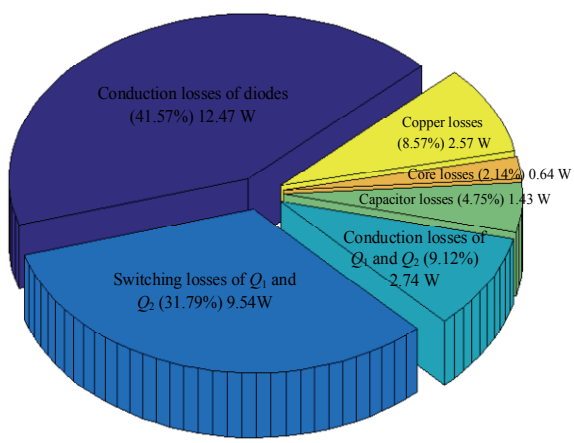


Fig. 17. Calculated loss distribution for the experiment when U_{in}=25V and P_n=400W.

turn-off (switching) losses and the conduction losses of Q_1 and Q_2. In addition, 41.57% is made up of the conduction losses for all of the diodes D_1-D_4 a little more than losses of Q_1 and Q_2.

V. Conclusion

A HS-BTL converter has been proposed in this paper. It has the advantages of a lower voltage stress (U_o/2) for the power semiconductors and capacitors, a wider range of the voltage-gain with modest duty cycles (0, 0.5) for the power switches, and the ability to avoid the narrow pulse of the PWM voltage waveforms when a high voltage gain is achieved. In addition, only three capacitors and one inductor are used in this converter, and the inductor is charged and discharged twice during each switching period. This results in a low input current ripple and a small size. In order to demonstrate the feasibility of the proposed converter, it was implemented in the laboratory with an output voltage of 400V and input voltages from 25V to 70V. A theoretical analysis and experimental results verified that the proposed DC-DC converter is able to serve as a power interface for fuel cell systems, where a wide voltage-gain range and a low input current ripple are often demanded.

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