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System Level ESD Analysis - A Comprehensive Review II on ESD Coupling Analysis Techniques

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Abstract – This study presents states-of-the art overview of the system level electrostatic discharge (ESD) analysis and testing. After brief description of ESD compliance standards and ESD coupling mechanisms, the study provides an in-depth review and comparison of the various techniques for the system level ESD coupling analysis using time and frequency domain techniques, full wave electromagnetic modeling and hybrid modeling. The methods used for improving system level ESD testing using troubleshooting and determining the root causes of soft failures, the optimization of ESD testing and the countermeasures to mitigate ESD problems are also discussed.

Keywords: Electrostatic Discharge (ESD), System level ESD testing, IEC 61000-4-2, ESD coupling, ESD generator, ESD source modeling, Circuit modeling, 3D modeling, *S*-Parameters, Frequency domain, Hybrid simulation, ESD measurements.

1. Introduction

Electrostatic discharge (ESD) is a phenomena whereby the discharge occurs between the two objects. The occurrence of an ESD event results in the discharge of high amplitude current with sharp rise time, to the product. A system level ESD event occurs when an electrical system experiences discharge of ESD noise [1-4]. The main sources of system level ESD events are charged humans holding a metallic object, such as a charger, a headset, or a USB etc., and charged metallic objects and products [5, 6].

The ESD event can be transmitted to the system by direct contact, indirect contact via the picking up of electromagnetic (EM) radiations, or by the occurrence of a secondary discharge event within the product [1, 3]. Smaller manufacturing geometries with comparatively less chip protection have increased the ESD vulnerability in the today's electronic products [1, 6, 7].

After a system level ESD event, the system may works normally without any problems, or the stressed system might experience soft failure (lockup/upset) and then work normally after rebooting with or without the intervention of the user [5, 6]. The system can also experience physical damage (referred as hard failure) either due to thermal effects or dielectric breakdown or both [8-11]. In the ESD environment, the high electric field established by the charged body collapse abruptly which can induce noise in the system [8, 10-12]. In addition, a sudden increase in the magnetic field occurs due to the discharged current. The rate of change of these electric and magnetic fields induces noise in the system. The severity of the ESD threat to the equipment under test (EUT) is dependent on the magnitude of the discharged ESD current [8, 10, 11, 13].

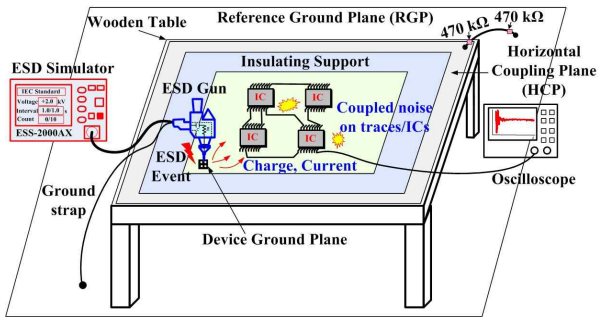

Fig. 1. System level ESD scenario

The purpose of the performing system level ESD testing is to ensure that the intended product (EUT) can work in normal operational environment during and after the stressing of the system level ESD event. System level ESD testing is performed using an ESD simulator or gun. The International Electrotechnical Commission (IEC) 61000-4-2 standard [14] describes the characteristics of the ESD simulator for the representation of particular scenario of a charged human body including a metallic object and discharging to the testing point on the EUT.

IEC 61000-4-2 [14] is the most popular standard which describes the procedure for the checking of the immunity of the system against an ESD strike. Fig. 1 depicts a typical system level ESD scenario. ESD event is created at the ground plane of the device using an ESD generator. The noise charge and current flows towards the active and passive components of device. The coupled noise on the traces and integrated circuit (ICs) can be measured using coaxial cable or optical cable with high speed digital oscilloscope.

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The induced ESD coupling on the EUT is not only dependent on the direct or in-direct stressing but also on the transient EM fields generated by ESD gun during discharge process [1, 8, 9, 12, 13, 15-17]. The ESD coupling analysis can be performed using experimental techniques [18-20], full wave numerical modeling [21-26], circuit modeling [3, 27-31] or hybrid simulation of the EUT and ESD source [20, 25, 32, 33]. However based on the current state of the art, it seems that full wave modeling has certain limitations in terms of computations resources and accuracy of modeling [11].

The uniqueness of this study lies in extensive and comprehensive review of the qualification standards of ESD, ESD coupling mechanisms, and methods being used for the system level ESD testing and analysis. Each topic has been reviewed thoroughly based on available literature and is presented and described in an attractive manner.

The structure of the study is as follows: Section 2 briefly describes the different compliance standards for ESD testing. An overview of ESD coupling mechanism is illustrated in Section 3. In Section 4, details and comparison of the various techniques for the ESD coupling analysis is given. Section 5 briefly states the suggestions for the improvement of system level ESD testing. Last Section 6 concludes the study.

2. ESD Compliance Standards

ESD compliance is required at different stages during the product design and development process. ESD conformity standards are available at both international and domestic levels to provide guidelines about immunity to ESD [14, 34-37]. The major differences in various standards relate to the voltage levels, test setups, resistor capacitor (RC) charging/discharging network values, verification of the calibrated waveform and the criteria for passing and failing [1, 38].

This section elaborates the differences between component and system level ESD testing and includes an overview of the associated standards for each.

2.1 Component level ESD standards

The component level testing for IC's is performed for un-powered EUT and is divided into Human Body Model (HBM) and Charge Device Model (CDM) [34, 39]. Component level testing is conducted as per the combined defined regulations of Electrostatic Discharge Association (ESDA) and JEDEC (ANSI/ESDA/JEDEC JS-001) [35, 36, 40] for HBM and JEDEC JESD22-C101 [37] or ANSI CDM ANSI/ESD S5.3.1 [41] for CDM.

The standard HBM current waveform has a rise time of 2-10 ns while it ranges from 50-500 ps for the CDM [34, 39]. CDM discharge waveforms have a high current value but very short settling time [41]. The discharge current value for HBM is quite low as compared to CDM and IEC, however it has long settling time compared to CDM and IEC waveforms [1, 14, 35, 36, 40, 41].

2.2 System level ESD standards

System level ESD testing is different from the component level ESD testing as it is performed for both powered and un-powered products [1, 14, 42]. Therefore each ESD testing environment has different compliance standards to follow. The main purposes of the component level ESD is to ensure the protection of the IC's against ESD during the production process and factory assembly, while system level ESD testing focuses on assuring of normal operation for end users [1, 43-45].

System level ESD compliance standards can be further categorized into five major classes: automotive, avionics, commercial electronics, medical devices and military ESD standards [1, 38]. The major associated national and international standards bodies are International Organization for Standardization (ISO), General Motors Worldwide (GMW), Society of Automotive Engineers (SAE), Ford Motor Company (FORD), and Japanese Automotive Standards Organization (JASO) for automotive, Radio Technical Commission for Aeronautics (RTCA) and Airbus for avionics, IEC, ISO, Generic Requirements (GR), and American National Standards Institute (ANSI) for commercial electronic products, and Military (MIL), JEDEC, and Standardization Agreement (STANAG) for military applications [1, 38].

Fig. 2 shows the compliance standards of different regulatory and other bodies [1, 38] for the above specified categories. The test limits for the road vehicles ESD testing [46] are higher than standard commercial electronic products. The compliance standards for the electronic products has been specified by IEC/EN, ANSI, ISO along with military as depicted in Fig. 2. However, mostly IEC 61000-4-2 is used. For the medical devices, IEC 60601-1-2 [42] is used for medical devices and employs the same testing procedure as specified in [14]. However, the failure criteria for medical equipment's as specified in [42] is different from those for general electronic products [14].

A brief description of the IEC 61000-4-2 [14] is given in the following subsection.

2.2.1 IEC 61000-4-21

The best known system level ESD testing standard are IEC 61000-4-2 [14] and ISO 10605 [46]. ISO 10605 is recommended for the ESD testing of automobiles. The ESD stressing waveform for system level ESD testing has a rise time of 0.6-1 ns which differs from the discharge waveform characteristics of HBM and CDM. IEC discharge waveform has a long decay time, similar to HBM and often termed as the composition of both HBM and CDM waveforms [1, 14, 35, 36, 40].

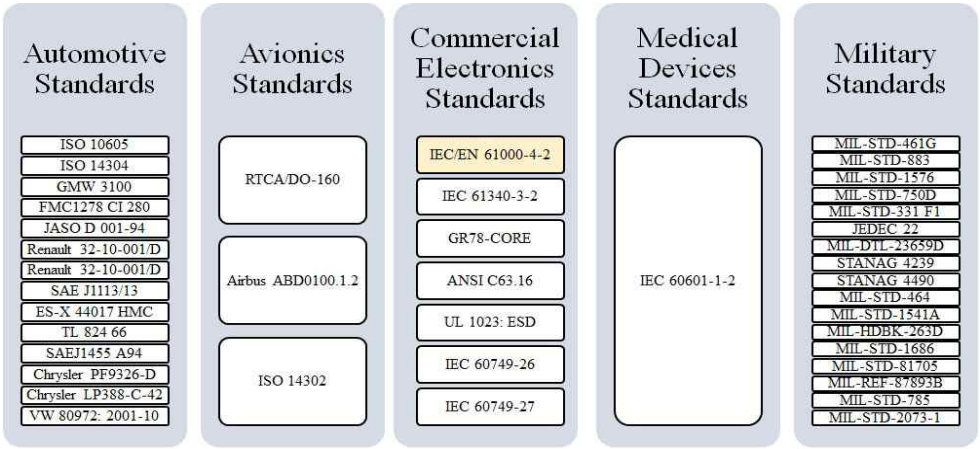

Fig. 2. ESD compliance standards for the system level ESD

Table 1. Comparison of component level (HBM) and system level ESD testing

	Component level ESD	System level ESD
Standard	JEDEC, ESDA [35]	IEC [14]
Environment	Factory assembly	End user normal operation
Test setup	Standardized	Application specific
EUT applications	IC	System (PC, cell phone, etc.)
EUT operation	Unpowered	Powered and unpowered
Discharge (R-C) network	100 pF/ 1500 Ω	150 pF/ 330 Ω
Typical test voltage (kV)	1-2	2-8
Peak current (A/kV)	0.7	3.75
Rise time (ns)	2 to10	0.6 to 1
Pulse width (ns)	150	50
Test application	IC pins	Enclosure, pins
Testing pin groups	Different pin combinations	Few special pins
Tested properties	IC protection circuits and concepts	System design
Failure	Hard	Soft and hard

IEC 61000-4-2 [14] and ISO 10605 [46] also differ from each other in terms of discharge network values, test voltage levels for contact and air discharge modes, discharge repetition rate, and the thickness of the insulating support used under the EUT and coupling plane during the actual testing [1, 34, 39, 47].

The IEC 61000-4-2 standard outlines the test procedure, pass/failure criteria for products, and the specifications of the ESD discharge waveforms at different test levels for the commercial electronic products. As per [14], ESD testing is performed for contact and air discharge modes with the standard discharge voltage levels ranging from 2 kV-15 kV. Test levels above 8 kV are used only for the specific requirements if required by the certain product developer and the intended user environment of that specific device. An ESD generator comprised of an RC discharge unit of 300 Q and 150 pF, is used for stressing of specified ESD current levels [14] on product to check its immunity to ESD noise. A summary of differences between component and system level ESD testing is elaborated in given in Table 1 [1, 43-45].

3. ESD Coupling Mechanisms

The details of different coupling mechanisms in ESD environments are outlined in this section. A coupling mechanism defines the way by which a charge or energy can be transferred to a product. It can be in the form of electric coupling (capacitive coupling) or magnetic coupling (inductive coupling), depending on the source of the noise and the coupling path [48]. The coupling mechanism for the ESD in shielded electronic equipment's or enclosures can be categorized into three main branches: direct coupling, indirect coupling and internal coupling [9, 48].

Direct coupling occurs when the ESD current is directly injected (using an ESD simulator) into an electronic product ground plane, coupling plane or enclosure. Fig. 1 illustrates the direct coupling case where the ESD signal is being injected at the device ground plane. It can also occur through the penetrating cables of the enclosure.

The EM field generated on the enclosure due to the ESD can impinge inside circuitry of the box or shielded enclosure through the apertures on the enclosure or because of non-ideal shielding of the connecting cables [13, 15, 49-51]. In this case, it is referred to as indirect coupling, as illustrated in Fig. 3. The field coupling of the high frequency signal generated at the time of the ESD event also falls into the category of indirect coupling [49]. The internal electronics within the product enclosure are usually protected by the insertion of proper suppressing devices at the aperture, cable entry levels and also at the inputs of printed circuit board (PCB) traces [1, 9]. However, the non-ideal characteristics of such suppressing and shielding components can allow residual noise to spread inside environment and cause interference [9, 15, 52].

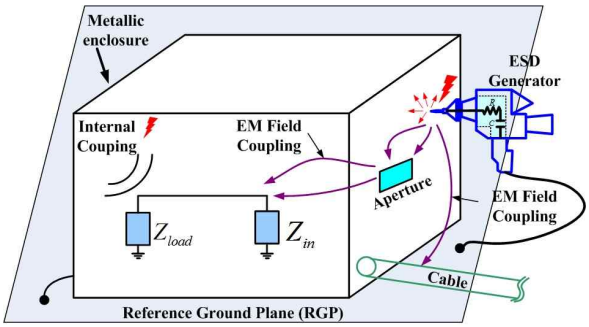

Fig. 3. Indirect and internal ESD coupling

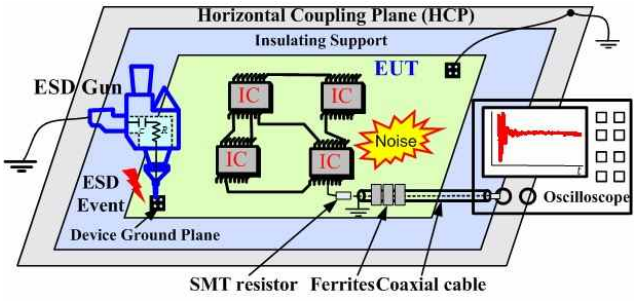

Fig. 4. Sketch of time domain ESD coupling measurement setup

Internal ESD coupling is the scenario when an ESD event occurrence inside a larger metallic box, such as a rotating spacecraft [9] (Fig. 3). The intensity of an ESD disturbance in internal coupling is depends on the resonance of the enclosure, the metallic shielding of the apertures, and the duration of the occurred disturbance. A careful analysis and determination of the major coupling mechanism is essential to make the ESD threat as small as possible for the product and for effective designing of the ESD protection modules [1, 5, 6, 8, 53].

4. System Level ESD Coupling Analysis Methods

In this section, a comprehensive review of the techniques being used for the system level ESD coupling analysis is presented. System level ESD coupling analysis techniques can be divided into two main branches: experimental analysis and 3D numerical analysis. Experimental analysis approaches can be further categorized into time domain and frequency domain analysis techniques. A brief overview of each analysis approach is given here.

4.1 Time domain analysis techniques

The time domain analysis approach involves the determination of the coupled noise at the EUT (prototype or finished product) point by zapping the EUT with an ESD gun or a TLP source [18-20]. The coupled noise voltage at the EUT location can be measured by either directly connecting the coaxial cable at the measurement point [26-29, 31, 54] or by probing using a high impedance voltage probe at that point [19, 20, 55].

A sketch of the typical time domain ESD induced voltage measurement using a high impedance probe for zapping the EUT ground is shown in Fig. 4. Typically, a semi-rigid coaxial cable with additional 470 Ω [19, 55] or 500 Ω [20] SMT resistors at the signal pin of the cable is soldered at the measurement point. With a 50 Ω coaxial cable and an additional 470 Ω /500 Ω in series for a high impedance probe, the measured voltage is approximately one tenth of the real recorded voltage ($V_{measured} = V_{real}$ x 50/520 or 550). The induced noise voltage is measured using a high speed, wide- bandwidth oscilloscope.

It is essential that the probing coax cable for measurements must be made electromagnetically invisible to minimize the effect of common mode noise on the measurement results [19, 27, 55, 56]. For this purpose, sufficient high and low frequency ferrites must be added along the sleeve of the attached coax cable [19, 27, 55, 56]. Although the installation of ferrites can reduce the common mode noise effect, the strong electric field generated during the zapping process can still couple to the signal pin of the soldered cable. To minimize direct E-field coupling, [19] proposed covering the single pin at soldering point with copper tape that is grounded at different points. The role of the gun zapping position is also very important for accurate and repeatable measurements. It has been proved that a change in the gun zapping position can cause significant variation in the induced voltage [19].

In addition to the direct soldering, the induced voltage and distributed current on the PCB of the EUT can be measured using E and H field probes in the time domain. Pommerenke's group [1, 6, 21, 53] proposed the use of a susceptibility scanning system based on the near-field electromagnetic interference scanning method in undertaking a system level root cause analysis of ESD problems (soft failure characterization). The injection tool employed in the scanning system was a TLP pulse source connected to near field probes (E/H field probes). The technique is very good because it can help to localize the affected sensitive nets and other ICs on PCBs in a systematic manner. In [57], the authors used the specially designed E and H field probes to measure current spreading on a PCB using the near field scanning method in [6, 53] with a transmission line pulse (TLP) source.

The time domain analysis approach is good for testing only. However, it might be time consuming and uneconomical because the actual measurement must be performed for every modified model of the product or EUT. Therefore, for the susceptibility testing on multiple modules of the EUT and fast estimation of induced coupling at the EUT, frequency domain analysis and the full wave numerical modeling approach might be preferable.

4.2 Frequency domain analysis techniques

The estimation of system level ESD coupling using frequency domain data has become increasingly important, recently, in ESD coupling analysis. Frequency domain measurement techniques are preferred over time-domain approaches because of the significant advantages of greater accuracy, the vast dynamic range of VNAs compared to oscilloscopes, and greater protection of the device in an ESD environment. Generally, in the frequency domain method, the recorded *S*-parameters are converted to time domain using Inverse Fast Fourier Transform (IFFT) algorithm for the analysis with step response excitation in the VNA [55] or by importing the measured *S*-parameters in data processing or the circuit simulator for induced voltage coupling analysis using an ESD circuit model or an ESD standard waveform as a source.

For the first time, to the best of our knowledge, the analysis of a penetrated fast transient electromagnetic field inside a cavity through an indirect ESD source using VNA characterization was reported in [58] in 2002. Caccavo *et al.* [58] used the internal time- domain functionality of a VNA to generate a Gaussian input pulse at the excitation port of the antenna and to record the induced voltage at the measurement port (inside the cavity) by computing the step response of the measured S21 data.

Koo *et al.* [55] described a frequency domain measurement method for the coupling analysis and validation of a standard ESD waveform and coupled voltage to traces, through a customized ESD generator with a parallel 39 Q resistor at the relay point, for the source excitation from the VNA. The induced voltage in [55] is determined by a similar strategy of [58] using the internal transformation features of VNA. Huang *et al.* [57] used a setup similar to that in [58] to estimate the ESD current spreading on a simple transmission line based PCB with a current probe installed at the measurement port with a step source injection from the VNA without the incorporation of the gun ground strap effect. The finding in [57] suggests that a better illustration of the spreaded current wavefront on the PCB was obtained with VNA measurements rather than with time domain measurements using TLP as source.

Recently, the authors of [27, 56] employed a modified ESD gun with a current transformer at the relay point for the source excitation from the VNA Nieden *et al.* [27, 56] developed a behavioral model based on the state-space representation of the frequency domain data using the vector fitting technique [59]. The proposed technique in [27, 56] had the limitations of greater approximation errors for higher frequency range data, handling of a large number of analyzing ports and convergence problems in circuit simulators due to higher order behavioral approximation models.

Park *et al.* [26, 54] used the PEEC method for the fast computation of the inductive and capacitive ESD coupling for simple victim geometries (μ-strip line PCB and loop structures). Compared to [27, 55, 56], Park employed a simple SMA connector to measure the transfer characteristics of victim geometries. The good agreement between the PEEC and measured transfer impedance results in [26, 54] depicts that a simple mocked SMA connector with a grounding cable is a good option to determine the frequency domain response, without modifying the commercial ESD simulator, as done by [27, 55, 56].

Another good study for the estimation of ESD stressing tolerance of EUT using a pre and post transmission line

Table 2. Summary of frequency domain measurement techniques

Reference	Year	Summary
Caccavo *et al.* [58]	2002	• Indirect ESD stress estimation inside cavity • Gaussian pulse from VNA as source • Induced voltage calculations inside time-domain facility of VNA
Koo *et al.* [55]	2007	• Direct ESD stress determination for loop, motherboard • Modified ESD generator for VNA step excitation • Induced voltage calculations inside VNA, as in [58]
Huang *et al.* [57]	2009	• Estimation of current spreading due to direct ESD stress • Step pulse from VNA as source • Current wavefronts computation based on measured data in data processing software
Nieden *et al.* [27, 56]	2011/2012	• Indirect ESD stress estimation for transmission line • Modified ESD generator • Induced voltage calculations in data processing environment using ESD waveform as source
Park *et al.* [26, 54]	2015	• Indirect ESD stress estimation for loop, transmission line • Mocked SMA connector • Impedance analysis for capacitive/inductive coupling determination
Yoshida *et al.* [28, 29]	2013/2015	• Indirect ESD stress determination for prototype board • Transmission line modeling using frequency-domain data • ESD stress simulation in circuit simulator using ESD waveform as source
Xiu *et al.* [30]	2015	• Test bed to estimate discharge current waveforms • Mocked gun tip to measure single port *S*-parameters • Estimation of discharge waveforms in circuit simulator
Jawad *et al.* [3]	2017	• Indirect ESD stress estimation for microstrip line PCB • Mocked SMA connector with different grounding configuration than in [26], [54] • Induced voltage estimation in circuit simulator using coupling transfer impedance function

modeling is done in [28, 29]. The authors of [28, 29] used the both measured and simulated *S*-parameters data to compute the induced voltages using the proposed method.

Xiu [30] developed a lumped circuit level ESD test bed for mobile and tethered EUTs using the single port *S*-parameter measurements through a mocked gun tip. In [31], the authors modeled the low dropout (LDO) voltage regulator and its interconnected lumped components in a SPICE environment using one port (for lumped components) and two port *S*-parameters (for LDO) and the specifications of components. Jawad *et al.* [3] also proposed an efficient and fast method for coupled voltage computation in a circuit simulator by using the coupling transfer impedance function based on recorded frequency domain measurements data using a mocked SMA connector as in [54] but with a different measurement setup that in [54]. The proposed method in [3] did not require a modified ESD generator, as proposed in [27, 55, 56].

A summary of the reviewed frequency domain measurements techniques for direct and indirect ESD stress estimations is shown in Table 2.

A performance comparison of the state-of-the-art system level ESD coupling analysis using frequency domain measurements is presented in Table 3 [3]. The criterion used for the accuracy of predicated results in Table 3, is the degree of matching between the measured results using an oscilloscope (time domain) and measured/simulated induced voltage results based on frequency domain measurements. The proposed modification of the ESD generator [27, 55, 56] allows the measurement of transfer characteristics from the relay point inside the ESD gun. However the other suggested techniques in [3, 26, 28-31, 54, 58] measured the coupling properties from the gun tip point to the sensing (measurement) point on the EUT. The coupling characteristics between the internal gun relay to the gun tip point are not covered by the suggested measurement methods in [3, 26, 28-31, 54, 58], which could affect the matching between the obtained induced voltage results using VNA characterization and the time domain using the ESD generator as the source.

The suggested characterization setups in [28, 29, 31, 57, 58] did not incorporate the effect of the ESD generator ground strap in frequency domain measurements. The effect of the ground strap cannot be ignored in frequency domain measurements because it changes the grounding configuration of time and frequency domain analysis setups. The variation in the grounding configuration could cause a significant change in the resonance of frequency domain results and could have an impact on the accuracy of obtained results. In [3, 16, 26, 30, 54], the authors suggested the inclusion of the gun ground strap effect in *S*-parameters measurements. However, care must be taken to ensure the proper ground configuration at the source point in the suggested two port measurement setups in [3, 26, 54] for the more accurate measurements as per the standard [14] requirements. The suggested setup in [3] is closer to the requirements in [14] requirements in terms of grounding requirements which is quite important in system level ESD measurements.

The review of frequency domain techniques in Table 3 suggests that the efficient iterative analysis of coupled voltage at the victim position can be done in a circuit simulation or data processing environment [3, 27-29, 31, 56] for either the change in input stressing voltage or the device termination characteristics. This can be achieved by just recording the *S*-parameters one time using measurements [3, 26-29, 31, 56] or through the full wave numerical simulation of the device [29]. The frequency

Table 3. Comparison of state-of-the-art frequency domain analysis techniques [3]

Author	Frequency Domain Measurements Technique	Requirement of Modified ESD Generator	Inclusion of Gun Ground Strap Effect	Estimation of Induced Voltage	Simulation Strategy for Induced Coupling	Accuracy of Predicated Results
Caccavo *et al.* [58]	Two port measurements using installed SMAs	No	No	Yes	Built in time-domain transformation function of VNA	Fair
Koo *et al.* [55]	Modified ESD generator	Yes	Yes	Yes	Built in time-domain transformation function of VNA	Good
Huang *et al.* [57]	Two port measurements using installed SMAs and current probe	No	No	Yes	Built in time-domain transformation function of VNA for current spreading estimation	Fair
Nieden *et al.* [27, 56]	Modified ESD generator	Yes	Yes	Yes	State space modeling using vector fitting technique	Good
Park *et al.* [26, 54]	Mocked SMA connector	No	Yes	No	Impedance analysis only	Not applicable
Yoshida *et al.* [28, 29]	Two-port measurements using installed SMAs	No	No	Yes	Transmission line modeling	Fair
Xiu *et al.* [30]	Single port *S*-parameters using a mocked gun tip	No	Yes	No	Development of test bench for discharge current/voltage	Not applicable
Zhao *et al.* [31]	Single and two port measurements using installed SMAs	No	No	Yes	SPICE modeling	Fair
Jawad *et al.* [3]	Mocked SMA connector	No	Yes	Yes	Efficient and fast estimation using developed coupling transfer impedance function	Good

domain measurements also offer the advantages of providing insight about the coupling characteristics between two points, which could help designers to design ESD protection schemes accordingly, for the minimization of the strong coupling content.

4.3 Full wave numerical analysis techniques

This section elaborates the review of the estimation of direct or indirect ESD noise at the EUT in full wave numerical environments. Full wave simulation of the device can provide information about the internal and external current densities due to indirect stressing and generated transient fields, which is very useful in determining the root cause of soft failures [22, 24, 60]. However, full wave modeling of the complex product for the susceptibility analysis is not easy [4, 11, 21, 25, 61]. The available examples of full wave numerical modeling are mostly for simplified devices or simple prototype boards [19, 22-24, 60, 62].

The use of the simplified generator model can reduce the overall computational resources and simulation time. How-ever, the simplified generator model can only be applied in susceptibility testing in the case where the effect of the injected current and magnetic field near the tip is dominant and the effect of the other components, such as electric and magnetic fields from the generator body and ground strap, is minimal [22, 25].

The effect of the other components can only be ignored in cases where the physical size of the EUT is much smaller than that of the ESD generator. If the EUT is bigger, such as the size of a laptop motherboard, then the effect of these components cannot be ignored, and complete detailed modeling of the ESD generator is required to accurately simulate the measurement setup [1, 11, 21, 25]. A very brief overview of the some examples of the ESD susceptibility in full wave numerical environments is given below.

Centola *et al.* [22] analyzed the induced voltage inside a small cavity with a slot, on a simplified mobile phone like device and on the mouse cable (transmission line) near the horizontal coupling plane (HCP) and vertical coupling plane (VCP) for the direct discharge using the developed simplified model. The induced voltage at the termination resistors of a transmission line was analyzed by [23] using the developed EM model of a NoiseKen generator. A study involving the measurement of ESD disturbance on a coaxial cable was carried out by [10] using the simple proposed Dito generator model. Caniggia *et al.* [17] also analyzed the radiated electric and magnetic fields from the simple generator model using free-space field sensors in CST MWS.

Qing *et al.* [60] analyzed the induced voltage in a semi-circular loop, induced current along a wire attached to simply modeled handheld device, and induced voltage within the 3D model of a commercial handheld device. Liu *et al.* [62] also analyzed the induced voltage in a semi-circular loop using FIT modeling. Compared to earlier modeling, both [60] and [62] used a detailed model of an ESD generator for susceptibility applications. Kim *et al.* [25] used the measured ESD waveform to analyze soft failure analysis with the detailed modeling of a mobile device. The modeling of a mobile device in [25] is more detailed than previous models [22, 60].

Lee *et al.* [24] used the proposed gun model in [60] to analyze the relationship between the PCB chassis and induced ESD field coupling for a simple PCB with a square loop trace on it in CST MWS. Recently, Park *et al.* [19] modeled a simplified prototype motherboard of mobile device and a simple ESD gun model using high frequency structure simulator (HFSS) to estimate the power ground noise voltage at the EUT point. In [21], the authors analyzed the soft- failure analysis of a two-way radio set by doing the ESD simulation in CST using simple Dito model and detailed numerical modeling of the radio-set.

A summary of the reviewed examples of full wave numerical modeling of ESD applications is given in Table 4. Full wave numerical modeling for ESD analysis is suitable for simple products. However, complex product (such as IC packages with non-linear circuitry) simulation

Table 4. Summary of ESD susceptibility testing in a full wave numerical environment

Author	Generator Model	• Susceptibility Application
Centola *et al.* [22]	Simple Dito	• Simplified metallic cavity with slot • Simplified mobile like device • A transmission line
Fujiwara *et al.* [23]	Simple NoiseKen	• Induced voltage in transmission line
Caniggia *et al.* [10, 17]	Simple Dito	• Induced voltage in coaxial cable • Estimation of radiated emissions from gun
Qing *et al.* [60]	Detailed Dito	• Induced voltage in semi-circular loop • Induced current in wire attached to handheld device • Induced voltage inside handheld device
Lee *et al.* [24]	Detailed Dito model of [106]	• Coupled field on square loop trace on simple PCB
Liu *et al.* [62]	Detailed NoiseKen	• Induced voltage in semi-circular loop
Kim *et al.* [25]	Measured ESD waveform as source	• Soft failure analysis with detailed mobile device modeling
Antong *et al.* [21]	Simple Dito	• Soft failure analysis of two-way radio set
Park *et al.* [19]	Simple Dito	• Simplified motherboard of mobile device

is quite challenging due to the very large computational resources requirements and the modeling of the system. For these reasons, hybrid simulation is preferred; whose details are given in the next section.

4.4 Hybrid simulation techniques

The time and computational resources and memory requirements for the full wave electromagnetic simulations of EUT and ESD generators as excitation sources are quite significant [11, 19, 21, 23-25, 60, 62, 63]. For this reason, hybrid simulation or co-simulation techniques are proposed [18, 20, 24, 32].

In hybrid simulation, two approaches are usually employed. The first approach involves obtaining an input ESD zapping current from the transient simulation of the circuit model or from measurements and using it as the input source in the 3D modeling of the EUT, as did by [25, 32]. As the circuit model contains the lumped elements corresponding to the major discharge process of the generator [4, 10, 17, 32, 61, 63], the associated computational cost is much lower compared to the full wave EM modeling of the gun [4, 32, 60, 61, 63].

The second approach involves the combining of two full wave modeling techniques. Here the EUT is characterized in terms of *S*-parameters in one full wave simulation environment, such as FEM [20], and then the obtained results are used in other 3D solver like based on FDTD for the injection of the input current to obtain the desired results [20]. Such approaches can result in a significant reduction of the solver computational cost compared to the complete 3D modeling of the total setup [32].

In addition, the extracted *S*-parameters by full wave simulation or by measurements can be imported to a time domain SPICE type circuit simulator [1, 3, 28, 29, 31, 64]. In a circuit simulator, input stressing ESD waveform can be applied from a circuit model of a generator and the induced coupling at the EUT can be estimated based on measured or simulated *S*-parameters [3, 28, 29]. Also the variations in the induced voltage at the EUT can be analyzed for the change in the output load, EUT characteristics, or for the designed protection circuitry in a circuit simulator quite easily and efficiently. However, the accuracy of the desired results depends on the hybridization approach. The division of the complete system into multiple sub domains and combining their results may improve the accuracy of the results compared with simple hybridization, as done by [32]. Some examples of the hybrid simulation strategy are given here.

Seoul *et al.* [33] analyzed the induced coupling to simple PCB by importing the frequency domain characteristics of PCB model (through its full wave simulation) into a circuit simulator. The circuit model of [55] was used by [33] as a source, the ESD performance of the PCB was analyzed with the additional integration of a SPICE like model of nonlinear devices. Yoshida *et al.* [28, 29] created a transmission (tx) line model of the test PCB based on its computed *S*-parameters using 3D simulation. The formed tx line model was imported into a circuit simulator to estimate the induced coupling with their own proposed circuit model [28] of an ESD generator as the source.

Lee *et al.* [20] reported a technique to estimate the induced ESD noise to the active ICs pins (FPGA, SDRAM). The authors in [20] employed a co-simulation strategy by combining a 3D numerical model and SPICE based modeling of *S*-parameters data and IBIS models (for the modeling of IC I/Os), in a CST design studio to simulate induced noise. Takada *et al.* [32] used the hybrid technique by combining the circuit and full wave EM simulation to simulate an ESD event in contact discharge mode using an FDTD solver. The authors obtained the ESD current from a circuit simulator, calculated the electrostatic field for initial field distribution, and then performed the full wave FDTD based simulation to estimate the discharge current and the surrounding electric and magnetic fields of generators. In [18], the authors first calculated the field generated by the full wave simulation of the ESD gun only using the gun model of [62]. Second, they built the SPICE model of the IC package and field coupling voltage and sources. Third, they combined the internal circuitry of IC in a SPICE like circuit simulator and estimated the induced voltage at IC due to ESD coupling fields.

After this extensive review of system level ESD coupling analysis methods, we conclude that the hybrid simulation approach in numerical tools [20, 20, 24, 28, 29, 32, 33, 62] or coupling analysis in circuit simulator/data processing software based on measured/simulated frequency domain device data [3, 28-31] are preferable for fast and efficient coupling analysis. However, full wave numerical modeling could be performed to detect major sources and paths of transient coupled field [19, 21, 24, 25, 60, 62].

5. Improvement of System Level ESD Testing

5.1 Soft-failure analysis

The determination of the root cause of failure using advanced software and hardware tools is one of the hot topics in designing an efficient system level ESD protection module [5, 6, 21]. Various techniques, such as susceptibility scanning using a 3D near field scanning system [6, 21, 53], susceptibility scanning using full wave numerical modeling [21] and systematic analysis methodology [25], new software techniques [44], and specifically designed system level test boards [44], have been adopted for this purpose

5.2 Optimization of System Level ESD Testing

Achieving test repeatability in system level ESD testing as per [14] is quite challenging. However, uncertainty regarding the test results can be reduced and more useful

information about failure mitigation can be obtained by following the steps suggested by Pommerenke in chapter six of [1]: (1) applying more than 10 pulses (40-50 pulses) at each testing point, (2) determining the failure threshold and not just conducting pass/fail qualification testing, (3) avoiding the air discharge test wherever possible, (4) identifying secondary ESD by measuring the tip and ground strap current using a current clamp, such as F-65, (5) recording the current in the air discharge mode using a current clamp at the gun tip, (6) observing and recording types of failure in detail, (7) comparing test results with different ESD generators, (8) using escalation strategy (testing for more than 10 pulses for EUT passing), as outlined in Annex F of the IEC standard [14]], and (9) understanding the information given in annexes of [14]. More details about these suggestions can be found in chapter six of [1].

5.3 Soft-failure countermeasures

The typical strategies used for the mitigation of soft failures are diverting the ESD current; filtering, shielding, or avoiding secondary ESD; improving the shielding connection of the connector cable and the enclosure for the connector junction; employing software/firmware; reducing cross talk; and reducing ESD occurrences by resisting and avoiding ESD [1].

6. Conclusion

In this study, an in-depth review of system level ESD testing is presented. The study covers the basics of ESD compliance standards (component vs. system level ESD standards); ESD coupling mechanisms; and a detailed review of analytical, circuit, and full wave modeling of ESD generators and system level ESD coupling analysis techniques, including time domain analysis, frequency domain analysis, full wave numerical simulation, and hybrid simulation approaches. Last, an overview of the suggestions for improving system level ESD qualification testing is presented.

This study is unique because it provides a comprehensive review of and basic knowledge about system level ESD testing in very attractive manner with and a detailed comparison of numerous reported techniques.

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