J Electr Eng Technol.2018; 13(5): 1986-1995
http://doi.org/10.5370/JEET.2018.13.5.1986

ISSN(Print) 1975-0102
ISSN(Online) 2093-7423

Fast Voltage-Balancing Scheme for a Carrier-Based Modulation in Three-Phase and Single-Phase NPC Three-Level Inverters

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Abstract – In this paper, a novel neutral-point voltage balancing scheme for NPC three-level inverters using carrier-based sinusoidal pulse width modulation (SPWM) method is developed. The new modulation approach, based on the obtained expressions of zero sequence voltage in all six sectors, can significantly suppress the low-frequency voltage oscillation in the neutral point at high modulation index and achieve a fast voltage-balancing dynamic performance. The implementation of the proposed method is very simple. Another attractive feature is that the scheme can stably control any voltage difference between the two dc-link capacitors within a certain range without using any extra hardware. Furthermore, the presented scheme is also applicable to the single-phase NPC three-level inverter. It can maintain the neutral-point voltage balance at full modulation index and improve the voltage-balancing dynamic performance of the single-phase NPC three-level inverter. The performance of the proposed strategy and its benefits over other previous techniques are verified experimentally.

Keywords: Sinusoidal pulse width modulation (SPWM), Neutral-point-clamped (NPC) three-level inverters, Zero sequence voltage, Voltage-balancing dynamic performance

1. Introduction

Since neutral-point-clamped three-level inverters were proposed by Nabae in 1981 [1], which have been widely employed in high- and medium-voltage and high-performance drive systems due to better quality output voltage and current waveforms compared with conventional two-level inverters [2-4]. It is well known that there are two important requirements of the implementation of an NPC three-level inverter, which are the modulation strategy and the control of the neutral-point voltage.

Most often, there are three well-established modulation methods to control the behavior of the fundamental voltage generated by the three-level inverter including SPWM, space vector pulse width modulation (SVPWM), and selective harmonic elimination (SHE) [5]. The first two methods are the preferred modulation techniques for the application in NPC three-level inverters. Compared to SPWM, SVPWM can achieve higher output phase voltage and better harmonic performance [6]. Furthermore, it has redundant switching states, which are a very important feature that can be used to maintain the dc-link capacitor voltages balance. A great deal of research has been focused on SVPWM method in the literature [4, 7-13]. For the balancing of the neutral-point voltage, controllers based on SVPWM method usually use the complicated dwelling time calculation and the switching sequence selection method, which is more complex than SPWM schemes.

Thus, the carrier-based SPWM method is also deeply studied in [14-26] because of the simplification in the modulation implementation. The PWM pulses is generated based on the comparison of a sinusoidal reference voltage with two carrier waveforms, which considerably simplifies the modulation process without sector identification, calculation for effective time and recombination. In SPWM schemes, in order to achieve the control of the neutral point voltage, zero sequence voltage as a control variable is commonly added to the PWM reference voltages [19]. A detailed study of this modulation method is carried out in [14]. The variation of the neutral-point voltage is analyzed on the basis of an averaged neutral-point current flowing out of or into the neutral point, and a carrier-based modulation method is presented. But the process of calculating zero sequence voltage is complex. It requires to deal with angles and trigonometric functions.

As an addition to [14], a simplified method is presented in [15]. However, the sign of the modified reference voltages is not certain when different zero sequence voltages are injected. A test-verify-revise algorithm is needed to address the problem, which brings additional computation cost. In [18], the relationship between the neutral-point current and zero sequence voltage is further analyzed. The zero sequence voltage is calculated by using searching-optimization or interpolation methods. Hence, its implementation is complicated.

In [19], a carrier-based modulation method is presented,

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Received: January 16, 2018; Accepted: May 12, 2018

which allows modeling of the neutral-point voltage dynamics as a continuous function of power drawn from the inverter. A proportional integral controller is designed on the basis of the continuous model. Nevertheless, the obtained transfer function of the controller strongly depends on the inverter output power. When the output power changes, the transfer function changes too.

The carrier-based implementation of the PWM method proposed in [21] is performed by adding a compensation value to the reference duty signals. However, to obtain an optimal compensation value, six cases should be discussed. Furthermore, the currents of the maximum, medium, and minimum reference voltages must be also sorted, which complicates its application.

Additionally, the modulation methods presented in [11, 16, 17, 19, 20, 24] have higher voltage distortion and increased switching losses. Since there are intervals in which the line-to-line voltages commutate among three states of the inverter, instead of two. At the same time, high *dv/dt* PWM pulses appear in the line-to-line voltage, which may induce overvoltage spikes at the terminals of the electric machine with long power cable. Such overvoltage spikes may cause the premature failure of the motor and cable insulation [27, 28].

In this paper, the relationship between the neutral-point current and zero sequence voltage is investigated in all six sectors, and the expressions of zero sequence voltage are deduced. According to the obtained zero-sequence-voltage expressions, a simple carrier-based modulation method is proposed. The method not only effectively mitigates the low-frequency neutral-point voltage oscillation, but also achieves a fast voltage-balancing dynamic performance. Moreover, the method is also applied to the single-phase NPC three-level inverter. Compared to the balancing methods developed in [29, 30], it is much easier to implement, and an excellent performance is also achieved.

This paper is organized as follows. First, a brief introduction of the three-phase NPC three-level inverter is presented in Section 2. In Section 3, the relationship between the neutral-point current and zero sequence voltage is studied, and a novel zero sequence voltage injection scheme for the neutral-point voltage balancing control in the three-phase and single-phase NPC three-level inverter is developed. Section 4 presents experimental results to show the excellent performance of the proposed approach. Finally, a conclusion is stated in Section 5.

2. Review of Three-Phase NPC Three-Level Inverters

A power circuit diagram of an NPC three-level inverter is depicted in Fig. 1. The clamping diode is used to connect the neutral point O to the midpoint of the series IGBT, which generates an additional voltage level. Thus, three switching states P, O, and N exist in each phase, and 27

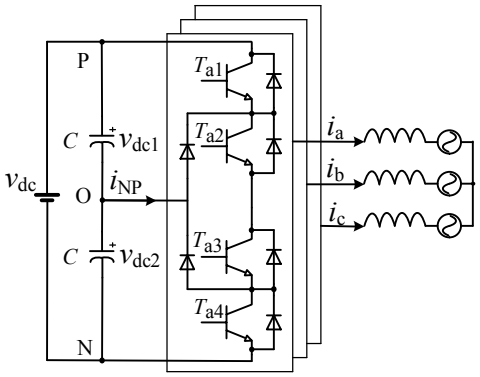


Fig. 1. Power circuit diagram of an NPC three-level inverter

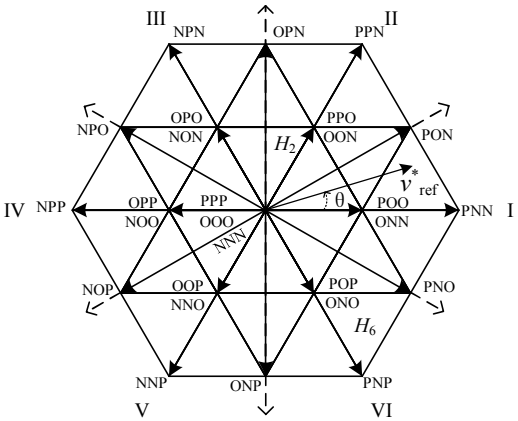


Fig. 2. Space vector diagram of an NPC three-level inverter

Table 1. Sector and reference voltage

θ (degree)	Sector	v^*_x (x=a, b, c)
-30~30	I	$v^*_a \geq 0, v^*_b \leq 0, v^*_c \leq 0$
30~90	II	$v^*_a \geq 0, v^*_b \geq 0, v^*_c \leq 0$
90~150	III	$v^*_a \leq 0, v^*_b \geq 0, v^*_c \leq 0$
150~210	IV	$v^*_a \leq 0, v^*_b \geq 0, v^*_c \geq 0$
210~270	V	$v^*_a \leq 0, v^*_b \leq 0, v^*_c \geq 0$
270~330	VI	$v^*_a \geq 0, v^*_b \leq 0, v^*_c \geq 0$

switching states in total. All these switching states define 19 voltage vectors, classified as one zero vector, six small vectors, six medium vectors, and six large vectors as shown in Fig. 2. For the small and medium vectors, one or two of the phases are connected to the neutral point, and the output currents are injected to the neutral point, which disturbs the voltage balance.

Different from the six sectors in conventional three-level space vector diagram, in Fig. 2 the space vector diagram is divided into six new sectors. The definition is given in Table 1. Additionally, from Table 1 it can be found that in all new sectors the sign of the reference voltage v^*_x remains unchanged, which is an attractive feature that is helpful to simplify the computation of the averaged neutral-point current in the three-level inverter. Since the only neutral-point current expression can be easily obtained in each new

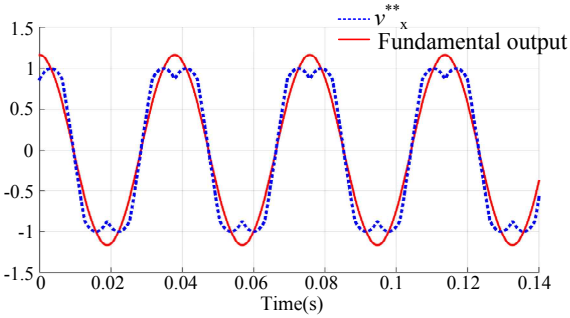


Fig. 3. Modified reference voltage v^{**}_{x} and fundamental output voltage

sector.

It is assumed that v^{*}_{a}, v^{*}_{b}, and v^{*}_{c} are the normalized per unit reference voltages given by

$$\begin{cases} v_a^* = m\cos(wt) \\ v_b^* = m\cos(wt - 2\pi/3) \\ v_c^* = m\cos(wt + 2\pi/3) \end{cases} \quad (1)$$

where m is modulation index, and $0 \le m \le 1$, and w is the angular frequency. If zero sequence voltage is injected to the three-phase reference voltages, the modified reference voltages v^{**}_{a}, v^{**}_{b}, and v^{**}_{c} are described in (2).

$$\begin{cases} v_a^{**} = \frac{2}{\sqrt{3}} v_a^* + v_{zs} \\ v_b^{**} = \frac{2}{\sqrt{3}} v_b^* + v_{zs} \\ v_c^{**} = \frac{2}{\sqrt{3}} v_c^* + v_{zs} \\ v_{zs} = -[(1-2k) + \frac{2k}{\sqrt{3}} v_{max}^* + (\frac{2}{\sqrt{3}} - \frac{2k}{\sqrt{3}}) v_{min}^*] \\ v_{max}^* = \max(v_a^*, v_b^*, v_c^*), v_{min}^* = \min(v_a^*, v_b^*, v_c^*) \end{cases} \quad (2)$$

where v_{zs} is zero sequence voltage. k is a variable factor, and [0, 1].

Using (2), the carrier-based modulation method is exactly equivalent to traditional SVPWM method in two-level inverter configurations, and the maximum modulation index achieved in the linear range is also 1.1547 as shown in Fig. 3.

Similarly, in three-level inverter configurations, the expression (2) is also applicable to the carrier-based PWM method. Moreover, zero sequence voltage as a control variable is added to the PWM reference voltages, which can be employed to accomplish the balancing control of the neutral-point voltage. Thus, a reasonable value of zero sequence voltage is very important for the balancing of the neutral-point voltage. There are two methods to obtain the value of zero sequence component. The first is changing the value of factor k in the expression (2), and the second is calculating v_{zs} directly with a certain approach. The latter is analyzed and discussed in the following section.

3. Novel Zero Sequence Voltage Injection Method for Neutral-Point Voltage-Balancing Control

3.1 Novel zero sequence voltage injection method for voltage-balancing control in three-phase NPC three-level inverters

3.1.1 Relationship between neutral-point current and zero sequence voltage

It is assumed that the capacitor voltages, the output currents, and the reference voltages are not varying in a switching period. The averaged neutral-point current i_{NP} over a switching period can be expressed by

$$i_{NP} = d_{Oa} i_a + d_{Ob} i_b + d_{Oc} i_c \quad (3)$$

where d_{Ox} denotes the duty cycle of a particular phase. Ox subscript represents that the phase is connected to the neutral point. i_a, i_b, and i_c are the three-phase currents, and $i_a + i_b + i_c = 0$ in a three-wire system.

In Fig. 4, it describes the relationship between one reference voltage and the duty cycle of the corresponding output switching function S_x. If the modified reference voltage $v^{**}_{x} \ge 0$, d_{Ox} can be given by

$$d_{Ox} = 1 - d_{Px} \quad (4)$$

The shadow region indicates the time duration of application of the neutral-point current in a switching period. For the carrier-based modulation method in Fig. 4, the duty cycles in a switching period can be depicted in (5).

$$\begin{cases} d_{Px} = v_x^{**} \\ d_{Ox} = 1 - v_x^{**} \\ d_{Nx} = 0 \end{cases} \quad (5)$$

where P_X, N_X and O_X subscripts represent that the phase is

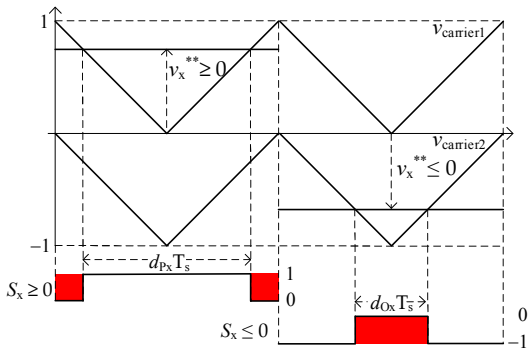


Fig. 4. PWM duty cycle generation

connected to the positive, negative and neutral point of the dc-link, respectively. If the modified reference voltage $v^{**}_{x} \le 0$, it can get

$$\begin{cases} d_{Px} = 0 \\ d_{Ox} = 1 + v^{**}_{x} \\ d_{Nx} = -v^{**}_{x} \end{cases} \tag{6}$$

When the reference vector stays at Sector I, according to Table 1, it has $v^{*}_{a} \ge 0$, $v^{*}_{b} \le 0$, and $v^{*}_{c} \le 0$. Thus, introducing (5) and (6) into (3), the averaged neutral-point current can be expressed in (7).

$$\begin{aligned} i_{NP} &= (1 - v^{**}_{a}) i_a + (1 + v^{**}_{b}) i_b + (1 + v^{**}_{c}) i_c \\ &= v^{**}_{a} (i_b + i_c) + v^{**}_{b} i_b + v^{**}_{c} i_c \\ &= (v^{**}_{a} + v^{**}_{b}) i_b + (v^{**}_{a} + v^{**}_{c}) i_c \end{aligned} \tag{7}$$

Therefore, substituting (2) in (7), the averaged neutral-point current is given by

$$\begin{aligned} i_{NP} &= (v^{**}_{a} + v^{**}_{b}) i_b + (v^{**}_{a} + v^{**}_{c}) i_c \\ &= -2[v_{zs} i_a + \frac{1}{\sqrt{3}} (v^{*}_{b} i_c + v^{*}_{c} i_b)] \end{aligned} \tag{8}$$

The above procedure is repeated for all other sectors, and the results are summarized in Table 2. It could be found that the averaged neutral-point current in a switching period in any sector can be depicted by zero sequence voltage, the original reference voltages, and the three-phase currents. It is evident that this method that only requires six expressions greatly simplifies the description of the neutral-point current, which consequently results in a great reduction of calculation effort.

Table 2. Duty cycles and the neutral-point currents in six sectors

Sector	d_{Ox}	i_{NP}
I	$d_{Oa} = 1 - v^{**}_{a}$ $d_{Ob} = 1 + v^{**}_{b}$ $d_{Oc} = 1 + v^{**}_{c}$	$-2[v_{zs} i_a + \frac{1}{\sqrt{3}} (v^{*}_{b} i_c + v^{*}_{c} i_b)]$
II	$d_{Oa} = 1 - v^{**}_{a}$ $d_{Ob} = 1 - v^{**}_{b}$ $d_{Oc} = 1 + v^{**}_{c}$	$2[v_{zs} i_c + \frac{1}{\sqrt{3}} (v^{*}_{a} i_b + v^{*}_{b} i_a)]$
III	$d_{Oa} = 1 + v^{**}_{a}$ $d_{Ob} = 1 - v^{**}_{b}$ $d_{Oc} = 1 + v^{**}_{c}$	$-2[v_{zs} i_b + \frac{1}{\sqrt{3}} (v^{*}_{a} i_c + v^{*}_{c} i_a)]$
IV	$d_{Oa} = 1 + v^{**}_{a}$ $d_{Ob} = 1 - v^{**}_{b}$ $d_{Oc} = 1 - v^{**}_{c}$	$2[v_{zs} i_a + \frac{1}{\sqrt{3}} (v^{*}_{b} i_c + v^{*}_{c} i_b)]$
V	$d_{Oa} = 1 + v^{**}_{a}$ $d_{Ob} = 1 + v^{**}_{b}$ $d_{Oc} = 1 - v^{**}_{c}$	$-2[v_{zs} i_c + \frac{1}{\sqrt{3}} (v^{*}_{a} i_b + v^{*}_{b} i_a)]$
VI	$d_{Oa} = 1 - v^{**}_{a}$ $d_{Ob} = 1 + v^{**}_{b}$ $d_{Oc} = 1 - v^{**}_{c}$	$2[v_{zs} i_b + \frac{1}{\sqrt{3}} (v^{*}_{a} i_c + v^{*}_{c} i_a)]$

3.1.2 Zero sequence voltage calculation

The equivalent circuit diagram of the dc-link is given in Fig. 5. The currents flowing through the dc-link capacitors are given by i_1 and i_2. By applying the Kirchoff's Current Law at node O, the neutral-point current can be given by (9) and (10).

$$i_{NP} = i_1 - i_2 \tag{9}$$

$$\begin{cases} i_1 = C \dfrac{dv_{dc1}}{dt} \\ i_2 = C \dfrac{dv_{dc2}}{dt} \end{cases} \tag{10}$$

Therefore, substituting (10) in (9), the neutral-point current is expressed in (11).

$$\begin{aligned} i_{NP} &\approx C \left(\frac{\Delta v_{dc1}}{T_s} - \frac{\Delta v_{dc2}}{T_s} \right) \\ &= \frac{C}{T_s} (v_{dc1} - v_{dc2}) \\ &= \frac{C}{T_s} \Delta v_{dc} \end{aligned} \tag{11}$$

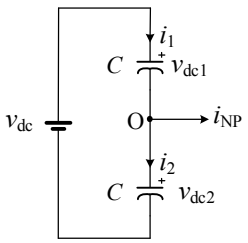


Fig. 5. Equivalent circuit diagram of the dc-link in the NPC three-level inverter

Table 3. Zero sequence voltages in six sectors

Sector	v_{zs}
I	$\frac{1}{i_a} [\frac{C \Delta v_{dc}}{2T_s} - \frac{1}{\sqrt{3}} (v^{*}_{b} i_c + v^{*}_{c} i_b)]$
II	$\frac{-1}{i_c} [\frac{C \Delta v_{dc}}{2T_s} + \frac{1}{\sqrt{3}} (v^{*}_{a} i_b + v^{*}_{b} i_a)]$
III	$\frac{1}{i_b} [\frac{C \Delta v_{dc}}{2T_s} - \frac{1}{\sqrt{3}} (v^{*}_{a} i_c + v^{*}_{c} i_a)]$
IV	$\frac{-1}{i_a} [\frac{C \Delta v_{dc}}{2T_s} + \frac{1}{\sqrt{3}} (v^{*}_{b} i_c + v^{*}_{c} i_b)]$
V	$\frac{1}{i_c} [\frac{C \Delta v_{dc}}{2T_s} - \frac{1}{\sqrt{3}} (v^{*}_{a} i_b + v^{*}_{b} i_a)]$
VI	$\frac{-1}{i_b} [\frac{C \Delta v_{dc}}{2T_s} + \frac{1}{\sqrt{3}} (v^{*}_{a} i_c + v^{*}_{c} i_a)]$

where C is the dc-link capacitance value. T_s is the switching period. v_{dc1} and v_{dc2} are the upper and lower capacitor voltages.

If the reference voltage vector stays at Sector I, the zero sequence voltage can be derived in (12).

$$v_{zs} = \frac{1}{i_a}[\frac{C\Delta v_{dc}}{2T_s} - \frac{1}{\sqrt{3}}(v_b^* i_c + v_c^* i_b)] \tag{12}$$

The mathematical expressions of zero sequence voltage in all sectors are deduced and summarized in Table 3. It is clear that the generation of zero sequence voltage for the neutral-point voltage balancing control is very simple. In particular, it does not depend on the load. Therefore, no knowledge of the load is required to implement the proposed approach. It just needs the information of the output currents, the original reference voltages, the voltage difference of the dc-link capacitors Δv_{dc}, the switching period, and the capacitance value. Thus, with this method, the zero sequence voltage is easily calculated.

Usually, the balancing control of the neutral-point voltage relies on some form of manipulation of small vectors in pairs, where the relative time duration of application of positive and negative small vectors in a pair is changed to maintain the neutral-point voltage balance. Therefore, the obtained zero sequence voltage as a control variable is added to the reference voltages, which is used to adjust the time duration of application of small vectors in a pair. It makes the voltage-balancing control much easier.

3.2 Proposed method for single-phase NPC three-level inverters

3.2.1 Review of single-phase NPC three-level inverters

The power circuit diagram of a single-phase NPC three-level inverter is described in Fig. 6. 9 switching states exist, and the space vector diagram is shown in Fig. 7.

The normalized per unit reference voltages are given by

$$\begin{cases} v_{a\_s}^* = n\cos(w_s t) \\ v_{b\_s}^* = -v_{a\_s}^* \end{cases} \tag{13}$$

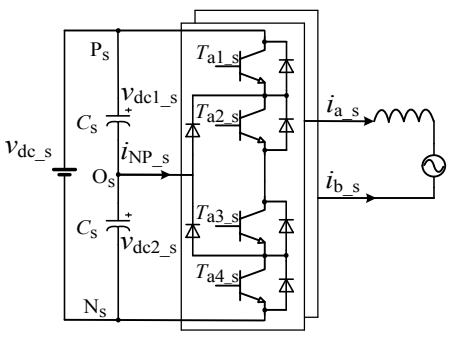


Fig. 6. Power circuit diagram of a single-phase NPC three-level inverter

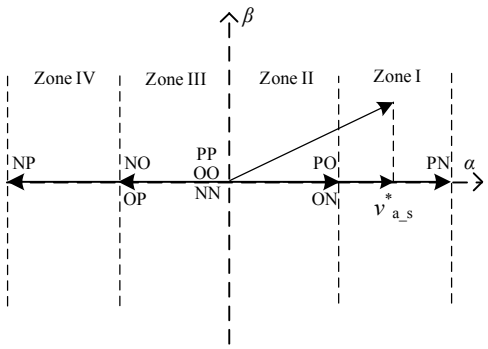


Fig. 7. Space vector diagram of a single-phase NPC three-level inverter

where n ($0 \le n \le 1$) is modulation index, and w_s is the angular frequency. It is assumed that v_{zs_s} represents zero sequence voltage. The desired output reference voltages $v^{**}_{a\_s}$ and $v^{**}_{b\_s}$ for the balancing control of the neutral-point voltage in a single-phase NPC three-level inverter are expressed in (14).

$$\begin{cases} v_{a\_s}^{**} = v_{a\_s}^* + v_{zs\_s} \\ v_{b\_s}^{**} = v_{b\_s}^* + v_{zs\_s} \end{cases} \tag{14}$$

3.2.2 Zero sequence voltage calculation for single-phase NPC three-level inverters

The averaged neutral-point current i_{NP_s} in the single-phase NPC three-level inverter can be described in (15).

$$i_{NP\_s} = d_{O_s a\_s} i_{a\_s} + d_{O_s b\_s} i_{b\_s} \tag{15}$$

where d denotes the duty cycle of a particular phase. O_sx_s subscript represents that the phase is connected to the neutral point. i_{a_s} and i_{b_s} are the output currents, and $i_{a\_s} + i_{b\_s} = 0$.

From the discussion in Section 3.1, the duty cycles are easily obtained as shown in Table 4.

Table 4. Output reference voltages and duty cycles

$v^{**}_{a\_s}$	d
$v^{**}_{a\_s} \ge 0$	$d_{P_s a\_s} = v^{**}_{a\_s}$ $d_{O_s a\_s} = 1 - v^{**}_{a\_s}$ $d_{N_s a\_s} = 0$
$v^{**}_{a\_s} \le 0$	$d_{P_s a\_s} = 0$ $d_{O_s a\_s} = 1 + v^{**}_{a\_s}$ $d_{N_s a\_s} = -v^{**}_{a\_s}$

where P_sa_s, N_sa_s and O_sa_s subscripts represent that the phase a is connected to the positive, negative, and neutral point of the dc-link, respectively. If the output reference voltage stays at Zone I in Fig. 7. Using (15) and Table 4, the averaged neutral-point current can be given by

Table 5. Neutral-point currents and zero sequence voltages in four zones

Zone	i_{NP_s}	v_{zs_s}
I II	$-2i_{a\_s}v_{zs\_s}$	$\frac{1}{i_{a\_s}}\frac{C_s\Delta v_{dc\_s}}{2T_s}$
III IV	$2i_{a\_s}v_{zs\_s}$	$\frac{-1}{i_{a\_s}}\frac{C_s\Delta v_{dc\_s}}{2T_s}$

$$\begin{aligned} i_{NP\_s} &= d_{O_sa\_s}i_{a\_s} + d_{O_sb\_s}i_{b\_s} \\ &= (1-v_{a\_s}^{**})i_{a\_s} + (1+v_{b\_s}^{**})i_{b\_s} \\ &= -i_{a\_s}(v_{a\_s}^{**} + v_{b\_s}^{**}) \\ &= -i_{a\_s}(v_{a\_s}^{*} + v_{zs\_s} - v_{a\_s}^{*} + v_{zs\_s}) \\ &= -2i_{a\_s}v_{zs\_s} \end{aligned} \tag{16}$$

The same operation is done for the other zones. The mathematical expressions of zero sequence voltage in all zones can be deduced and summarized in Table 5. It is observed that the neutral-point current is only dependent on the output current i_{a_s} and zero sequence voltage, without the need of the reference voltages. Obviously, the zero-sequence voltage expressions are very simple, and only two expressions are required. Similarly, for the balancing of the neutral-point voltage, the obtained zero sequence voltage is also added to the reference voltages. In fact, in single-phase NPC three-level inverters, the zero sequence voltage is still employed to adjust the relative time duration of application of positive and negative small vectors in a pair.

4. Experimental Results

4.1 Three-phase NPC three-level inverter experimental results

In order to illustrate the performance of the proposed PWM strategy, a prototype with a front-end diode bridge rectifier and a three-phase NPC three-level inverter has been built, and the inverter is realized using SEMMIKON diode and Infineon IGBT module. The values of the dc-link voltage and the capacitor are v_{dc} = 210V and C = 1680uF, respectively. The switching frequency is 5kHz and the modulation index is 0.88 in all results. The inverter feeds an induction motor, and it is controlled by using open-loop *v/f* control. The output currents and the dc-link voltages are measured to implement the carrier-based PWM voltage

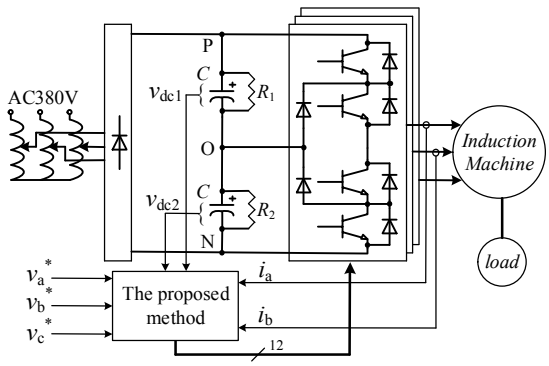


Fig. 8. Block diagram of the drive system

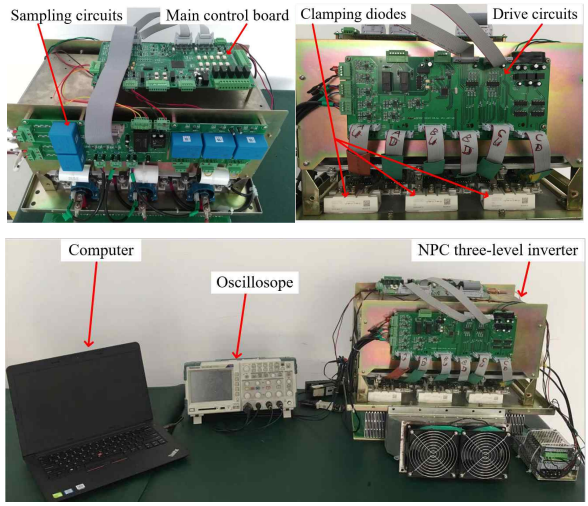
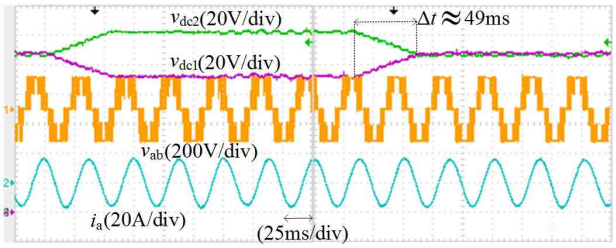
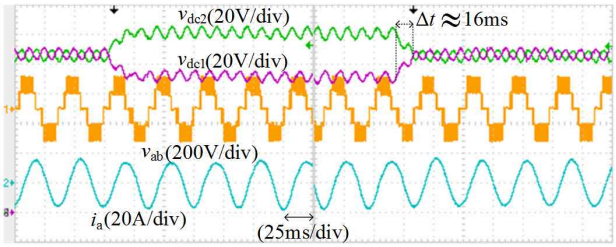


Fig. 9. Experimental platform



(a)



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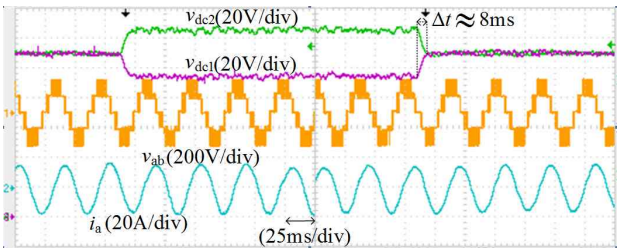


(c)

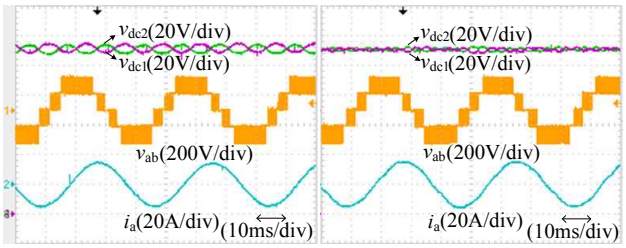
Fig. 10. Experimental results of the neutral-point voltage balancing control; (a) VSVPWM, (b) SPWM, (c) The proposed method

balancing scheme. The block diagram of the NPC three-level inverter is shown in Fig. 8, and Fig. 9 shows the experimental platform.

To show the voltage-balancing dynamic performance of the proposed scheme, some experiments are done. The dc-link capacitor voltages are intentionally unbalanced by 30V. The experimental results are shown in Fig. 10. Fig. 10(a) and (b) show the results that are obtained from the applications of virtual space vector pulse width modulation (VSVPWM) and SPWM, respectively. Fig. 10(c) describes the same results when the proposed modulation technique is applied. It can be seen that a faster response to balance the dc-link voltages is achieved by using the proposed method. The balancing time is 8ms, which is less than one sixth that of VSVPWM and one half of the balancing time of SPWM. Obviously, the presented approach significantly improves the neutral-point voltage-balancing dynamic performance. Furthermore, compared with VSVPWM, the proposed method diminishes the line-to-line voltage distortion and reduces the switching losses. Compared with SPWM, the developed scheme preserves the switching frequencies of the power devices and effectively suppresses the low-frequency voltage oscillation in the neutral point at high modulation index.

Table 6. Comparison results of the averaged execution time

Method	Execution time
VSVPWM	20.63us
SPWM	10.52us
The proposed method	7.32us



(a) (b)

Fig. 11. Experimental results: (a) Without the neutral-point voltage balancing strategy; (b) With the neutral-point voltage balancing strategy

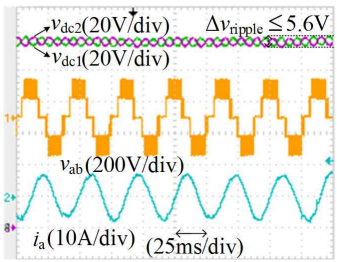


Fig. 12. Experimental results at low power factor and high modulation index

Table 6 lists the comparison results of the averaged execution time with the same digital signal processor (DSP) TMS320F28335 controller. The clock frequency is 150MHz, and the sampling period is 0.2ms. It is evident that the DSP controller consumes less time to finish the proposed algorithm. It proves that the proposed method significantly reduces the computational effort.

Fig. 11(a) shows the results without the neutral-point voltage-balancing strategy. Note that there is a significant low-frequency voltage oscillation on the dc-link capacitors. The frequency is three times the fundamental output frequency and the amplitude of the ripple is 9V. With the proposed method, the same results are shown in Fig. 11(b). In this case, the low-frequency voltage oscillation is effectively suppressed.

Besides the dc-link capacitance value, the output currents, and the control period, the power factor and the modulation index could also influence the neutral-point voltage variation [18]. Thus, a low power factor (less than 0.20) and a high modulation index (m=0.88) are selected for analysis. The experiment is conducted, and the dc-link voltages, the line-to-line voltage, and the current are shown in Fig. 12. It is obvious that the difference of the dc-link voltages Δv_{ripple} is less than 5.6V, and it is very small. Consequently, the

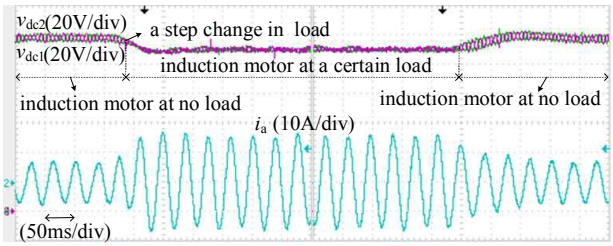
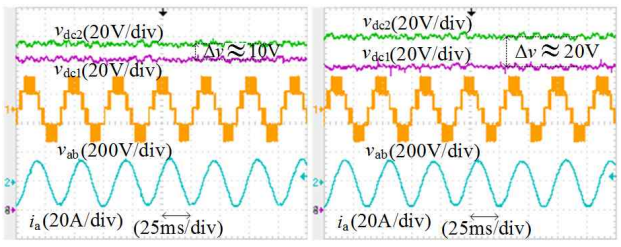
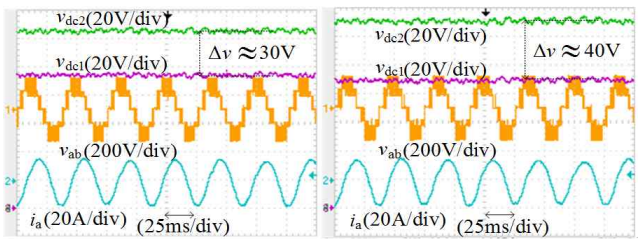


Fig. 13. Experimental results of the proposed method at the load change



(a) (b)



(c) (d)

Fig. 14. Experimental results of the method with voltage difference: (a) 10V, (b) 20V, (c) 30V, (d) 40V

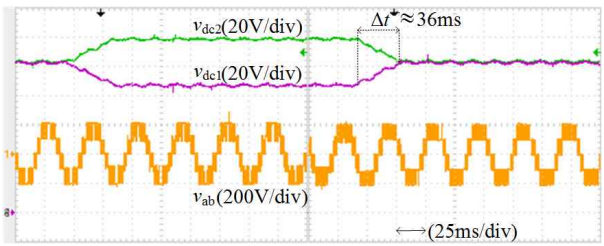
proposed method could effectively mitigate the neutral-point voltage oscillation at low power factor and high modulation index.

The transient performance of the drive is described in Fig. 13. It can be found that the balancing of the neutral-point voltage is able to be achieved by the proposed method when the induction motor load changes. In addition, the developed scheme can achieve any voltage difference between the two dc-link capacitors within a certain range without using any extra hardware. The experimental results are presented in Fig. 14, and the proposed method stably maintains the voltage difference. It can be found that the larger the voltage difference is, the higher the total harmonic distortion of the output line-to-line voltage is, which also explains why the balancing control of the neutral-point voltage in the three-phase NPC three-level inverter must be required.

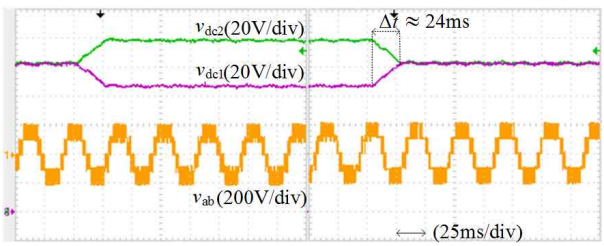
4.2 Single-phase NPC three-level inverter experimental results

The experimental platform of the single-phase NPC three-level inverter is similar to that of the three-phase inverter, and only phase a and phase b arms operate. The dc-link voltage is 210V. The switching frequency is 5kHz and the modulation index is 1. The resistive-inductive load is connected to the inverter. Its inductance and equivalent resistance are 9mH and 27Ω, respectively. The inverter is also controlled by using open-loop *v/f* control.

The voltage difference of the upper and lower capacitors is also 30V. The experimental results are given in Fig. 15. Fig. 15(a) shows the results that are obtained from the application of SPWM. Fig. 15(b) describes the same results when the proposed modulation technique is applied. It can

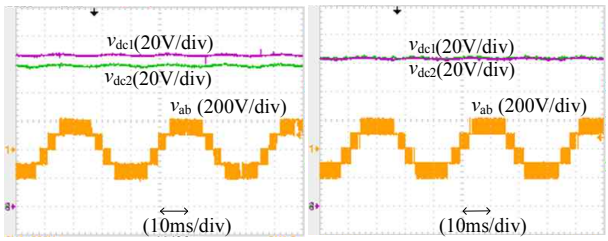


(a)



(b)

Fig. 15. Experimental results of the neutral-point voltage balancing control; (a) SPWM, (b) The proposed method



(a) (b)

Fig. 16. Experimental results; (a) Without the neutral-point voltage balancing strategy, (b) With the neutral-point voltage balancing strategy

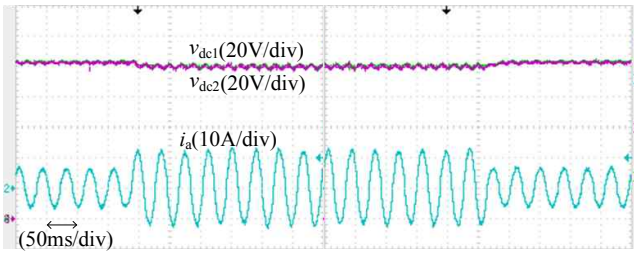


Fig. 17. Experimental results of the proposed method at the load change

be found that the proposed method achieves a faster voltage-balancing dynamic performance at full modulation index. The balancing time is significantly shorter than that of SPWM.

Fig. 16(a) describes the results without the neutral-point voltage-balancing strategy. Different from the results given in Fig. 11(a), a dc unbalance appears in the neutral point of the single-phase NPC three-level inverter. But, using the proposed approach, it not only completely removes the dc unbalance, but also eliminates the low-frequency voltage oscillation in the neutral point at full modulation index as shown in Fig. 16(b). Thus, the proposed method can achieve better neutral-point voltage-balancing performance in the single-phase NPC three-level inverter.

In order to show the transient performance of the single-phase drive system, experiments are conducted as shown in Fig. 17. It is evident that the two dc-link voltages are equal, when the load increases or decreases. Thus, the method presented can effectively maintain the neutral-point voltage balance in this case.

5. Conclusion

In this paper, a fast neutral-point voltage-balancing scheme for a carrier-based modulation in three-phase and single-phase NPC three-level inverters is developed. The following conclusions could be made.

1) A simple relationship between the neutral-point current and zero sequence voltage is established in all six sectors, and the mathematical expressions of zero

sequence voltage are derived. Based on the expressions, a novel zero sequence voltage injection scheme for the neutral-point voltage balancing control is proposed, which effectively mitigates the neutral-point voltage variation at high modulation index and provides the system with a faster voltage-balancing dynamic performance. Moreover, it is considerably less complex to implement the proposed method with greatly reduced computational effort.

2) The proposed method is also successfully applied to the single-phase NPC three-level inverter. It maintains the neutral-point voltage balance at full modulation index and achieve faster voltage-balancing dynamic performance.

Finally, the performance of the developed scheme and its benefits are verified through experimental results.

Acknowledgements

This research is supported by the National Natural Science Foundation of China under Grants No.51407080.

References

[1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518-523, Sept. 1981.

[2] J. Li, A. Q. Huang, Z. Liang, and S. Bhattacharya, "Analysis and design of active NPC (ANPC) inverters for fault-tolerant operation of high-power electrical drives," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 519-533, Feb. 2012.

[3] V. Yaramasu and B. Wu, "Predictive control of a three-level boost converter and an NPC inverter for high-power PMSG-based medium voltage wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5308-5322, Oct. 2014.

[4] Y. Jiao, F. C. Lee, and S. Lu, "Space vector modulation for three-level NPC converter with neutral point voltage balance and switching loss reduction," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5579-5591, Oct. 2014.

[5] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219-2230, Jul. 2010.

[6] F. Wang, "Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters," *IEEE Trans. Ind. Appl.*, vol. 38, no. 2, pp. 500-506, Mar./ Apr. 2002.

[7] G. I. Orfanoudakis, M. A. Yuratich, and S. M. Sharkh, "Nearest-vector modulation strategies with minimum amplitude of low-frequency neutral-point voltage oscillations for the neutral-point-clamped converter," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4485-4499, Oct. 2013.

[8] U. M. Choi, J. S. Lee, and K. B. Lee, "New modulation strategy to balance the neutral-point voltage for three-level neutral-clamped inverter systems," *IEEE Trans. Energy Convers.*, vol. 29, no. 1, pp. 91-100, Mar. 2014.

[9] J. S. Lee and K. B. Lee, "New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformerless photovoltaic systems using a three-level inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1720-1732, Apr. 2014.

[10] U. M. Choi, F. Blaabjerg, and K. B. Lee, "Method to minimize the low-frequency neutral-point voltage oscillations with time-offset injection for neutral-point-clamped inverters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1678-1691, Mar./Apr. 2015.

[11] S. Gui, Z. Lin, and S. Huang, "A varied VSVM strategy for balancing the neutral-point voltage of DC-link capacitors in three-level NPC converters," *Energies*, vol. 8, no. 3, pp. 2032-2047, Mar. 2015.

[12] A. Choudhury, P. Pillay, and S. S. Williamson, "Modified DC-bus voltage-balancing algorithm based three-level neutral-point-clamped IPMSM drive for electric vehicle applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 761-772, Feb. 2016.

[13] X. Li, S. Dusmez, B. Akin, and K. Rajashekara, "A new SVPWM for the phase current reconstruction of three-phase three-level T-type converters," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2627-2637, Mar. 2016.

[14] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," *Industry Applications Society Annual Meeting*, pp. 965-970, Oct. 1993.

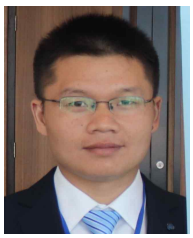
[15] Q. Song, W. Liu, Q. Yu, X. Xie, and Z. Wang, "A neutral-point potential balancing algorithm for three-level NPC inverters using analytically injected zero-sequence voltage," *Applied Power Electronics Conference and Exposition*, pp. 228-233, Feb. 2003.

[16] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Corbalan, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 305-314, Feb. 2009.

[17] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibanez, and J. L. Villate, "A comprehensive study of a hybrid modulation technique for the neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 294-304, Feb. 2009.

[18] C. Wang and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2262-2271, Jul. 2010.

[19] R. Maheshwari, S. Munk-Nielsen, and S. Busquets-Monge, "Design of neutral-point voltage controller of a three-level NPC inverter with small DC-link capacitors," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1861-1871, May 2013.
[20] W. Srirattanawichaikul, S. Premrudeepreechacharn, and Y. Kumsuwan, "Modified unipolar carrier-based PWM strategy for three-level neutral-point-clamped voltage source inverters," *J. Electr. Eng. Technol.*, vol. 9, no. 2, pp. 489-500, Mar. 2014.
[21] J. S. Lee and K. B. Lee, "Time-offset injection method for neutral-point AC ripple voltage reduction in a three-level inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1931-1941, Mar. 2016.
[22] I. Lopez, S. Ceballos, J. Pou, J. Zaragoza, J. Andreu, I. Kortabarria, and V. G. Agelidis, "Modulation strategy for multiphase neutral-point-clamped converters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 928-941, Feb. 2016.
[23] K. S. Ahn, N. S. Choi, E. C. Lee, and H. J. Kim, "A study on a carrier based PWM having constant common mode voltage and minimized switching frequency in three-level inverter," *J. Electr. Eng. Technol.*, vol. 11, no. 2, pp. 393-404, Mar. 2016.
[24] Z. Wang, F. Cui, G. Zhang, T. Shi, and C. Xia, "Novel carrier-based PWM strategy with zero-sequence voltage injected for three-level NPC inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1442-1451, Dec. 2016.
[25] W. Jiang, Y. Gao, J. Wang, and L. Wang, "A hybrid modulation strategy with reduced switching losses and neutral point potential balance for three-level NPC inverter," *J. Electr. Eng. Technol.*, vol. 12, no. 2, pp. 738-750, Mar. 2017.
[26] G. Yan, S. Duan, S. Zhao, G. Li, W. Wu, and H. Li, "Research on the mechanism of neutral-point voltage fluctuation and capacitor voltage balancing control strategy of three-phase three-level T-type inverter," *J. Electr. Eng. Technol.*, vol. 12, no. 6, pp. 2227-2236, Nov. 2017.
[27] M. C. Sousounis, J. K. H. Shek, and M. A. Mueller, "Filter design for cable overvoltage and power loss minimization in a tidal energy system with onshore converters," *IEEE Trans. Sustain. Energy*, vol. 7, no. 1, pp. 400-408, Jan. 2016.
[28] Y. Jiang, W. Wu, Y. He, H. S. H. Chung, and F. Blaabjerg, "New passive filter design method for overvoltage suppression and bearing currents mitigation in a long cable based PWM inverter-fed motor drive system," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7882-7893, Oct. 2017.
[29] W. Song, X. Feng, and K. M. Smedley, "A carrier-based PWM strategy with the offset voltage injection for single-phase three-level neutral-point-clamped converters," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1083-1095, Mar. 2013.
[30] Z. Zhang, Y. Xie, J. Le, and L. Chen, "Study of SVPWM method for single-phase three-level diode-clamped inverter," *Proceedings of the CSEE*, vol. 30, no. 27, pp. 62-68, Sep. 2010.



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