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Design and Implementation of PIC/FLC plus SMC for Positive Output Elementary Super Lift Luo Converter working in Discontinuous Conduction Mode

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Abstract – This paper proposes a confronting feedback control structure and controllers for positive output elementary super lift Luo converters (POESLLCs) working in discontinuous conduction mode (DCM). The POESLLC offers the merits like high voltage transfer gain, good efficiency, and minimized coil current and capacitor voltage ripples. The POESLLC working in DCM holds the value of not having right half pole zero (RHPZ) in their control to output transfer function unlike continuous conduction mode (CCM). Also the DCM bestows superlative dynamic response, eliminates the reverse recovery troubles of diode and retains the stability. The proposed control structure involves two controllers respectively to control the voltage (outer) loop and the current (inner) loop to confront the time-varying ON/OFF characteristics of variable structured systems (VSSs) like POESLLC. This study involves two different combination of feedback controllers viz. the proportional integral controller (PIC) plus sliding mode controller (SMC) and the fuzzy logic controller (FLC) plus SMC. The state space averaging modeling of POESLLC in DCM is reviewed first, then design of PIC, FLC and SMC are detailed. The performance of developed controller combinations is studied at different working states of the POESLLC system by MATLAB-Simulink implementation. Further the experimental corroboration is done through implementation of the developed controllers in PIC 16F877A processor. The prototype uses IRF250 MOSFET, IR2110 driver and UF5408 diodes. The results reassured the proficiency of designed FLC plus SMC combination over its counterpart PIC plus SMC.

Keywords: DC-DC converter, POESLLC, Sliding mode controller, Fuzzy logic controller, State space averaging, Proportional-integral controller.

1. Introduction

Today's industrial applications demands colossal boost-up voltage gains in DC-DC converters. In present days, it is very hard to interface applications such as battery backed uninterruptible power supply, photovoltaic energy conversion system, fuel cell, medical equipments, robot systems, renewable energy systems etc [1-3]. The traditional dc-dc converters such as the buck, boost, buck-boost, Cuk, single-ended primary inductor converter (SEPIC), Zeta converter, K-Y converter fail to offer the voltage transfer gain projected in theoretical calculations due to the upshot of power semiconductor switches, rectifier power diodes, and the equivalent series resistance (ESR) of inductors and capacitors [4-7]. Positive output elementary super lift Luo converter (POESLLC) is a one of the imperative DC-DC converter topology that gives a positive controlled output DC voltage from a positive DC input voltage. The prime connotation of this converter is higher voltage transfer gain (in geometric progression), excellent efficiency, suppressed inductor current/capacitor voltage ripples [8-9]. The above features have attracted the applications such as digital camera, lap-top computers, thin-film-transistor liquid-crystal display (TFT-LCD) bias supplies, computer mother board, mobiles etc. For all these portable applications, it is mandatory to expand the autonomy of the battery and hence the efficiency is critical even this converter operates at light load or no load conditions. The POESLLC works in two different modes. In continuous conduction mode (CCM), there is a right half plane zero (RHPZ), which is complex to be stable and not suitable for light load applications. The inductor current of this converter never zero and hence the name CCM. In contrary, when the same converter operates in the discontinuous conduction mode (DCM) has no RHPZ, improves system stability, avoid the reverse recovery

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problem of the diode and also more suitable for low power application [10-11]. The development of PIC to provide a good static and dynamic performance in POESLLC has been discussed. MATLAB based study showed the dynamic characteristics and analyzed the closed loop performances with resistive load for supply and load disturbances [12]. The state space averaging technique has been applied for positive output super lift Luo converter and the transfer function has been arrived [13]. The design of SMC for negative output elementary super lift Luo converter (NOESLLC) operated in CCM has been performed [14]. The simulation of NOESLLC with its control model is implemented in MATLAB-Simulink and suggested for applications such as computer power supplies, communication equipments and medical equipments, especially for high voltage-voltage. Three possible DCMs of positive output super-lift converters (POSLC) have been introduced. A general analysis on the elementary circuit of POSLC in the discontinuous inductor current mode (DICM) has been discussed. The steady state properties and the boundary conditions in DICM have been presented [15]. The functioning of improved negative output super lift Luo converter (INOSLC) with design of PIC have been detailed [16]. The values of K_p and T_i in PIC have been tuned using Zeigler-Nichols tuning method. The design and MATLAB simulation of a FLC controlled super lift Luo converter have been presented [17]. An adaptive SMC for DC-DC converters has been devised [18]. In the state space model of DC-DC converters, the unknown coordinate components of the desired equilibrium point (static working point), which are necessary to obtain the error vector and then build the sliding surface, are arrived through an adaptive law. Due to the time varying switched mode of operation, the dynamic characteristics of POESLLC is non-linear in nature. The conformist controllers are not able to improve the dynamic performance under the line voltage, load and component changes. Therefore, this paper proposes PIC/FLC plus SMC structure for POESLLC in DCM. The state-space average model for POESLLC in DCM is derived and then design of PIC, FLC and SMC is explained. The performance of POESLLC in DCM with designed controller is verified at different operating regions through proper selection of the controller parameters. A detailed comparison of performance of PIC plus SMC is done with FLC plus SMC. The simulation study is performed through MALTAB and experimental investigation is done through PIC 16F877A processor. The results confirm the betterment of FLC plus SMC over PIC plus SMC.

2. Analysis of DCM Operation of POESLLC

2.1 Working and voltage transfer gain of POESLLC

The power circuit of the POESLLC is pictured in Fig. 1

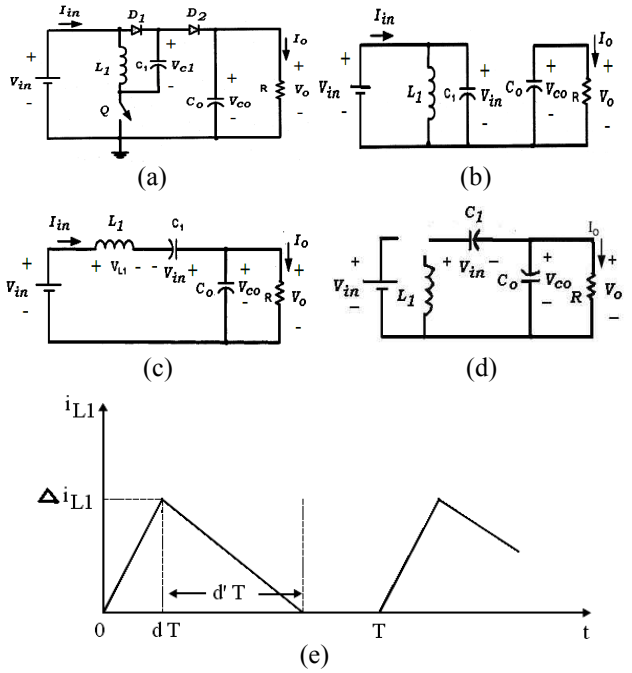


Fig. 1. POESLLC (a) Power circuit, (b) mode 1, and (c) mode 2, (d) mode 3-Inductor current becomes zero during turn-off mode and (e) Inductor current in DCM

(a). The efficient voltage step-up capability can be accomplished by controlling the power switch Q of the POESLLC. In the power circuit, V_{in} is a dc input supply voltage, Q is the power switch (n-channel MOSFET) and (D_1, D_2) are freewheeling diodes. Energy storage elements are capacitors (C_1, C_o) and inductor L_1. V_o is the output voltage and R is the load resistance. To analyze the operation of the POESLLC, the circuit can be divided in to two states, viz. the switch-closed and the switch-open. Fig.1 (b) and Fig.1(c) show the two states of operation of the POESLLC [19]. The DCM working of the POESLLC circuit is demonstrating in Fig.1(d) and in addition it's the coil (inductor) current waveform is demonstrated in Fig.1(e). The capacitor values are larger sufficient that the capacitor voltages can be assumed to be constant. From the Fig. 1(e), T is the switching time period and d is the duty cycle. During the DCM period (d+d') $T \le t \le T$, the current through the inductor is zero; switch is open state, and diodes D_1 and D_2 is off state as shown in Fig. 1 (d). From the Fig. 1(e), it is visibly demonstrated that the condition of DCM is imprinted as (1)

$$d + d' < 1 \tag{1}$$

Consider the Figs. 1(b), 1 (c) and 1(e). During $0 \le t \le dT$, i_{L1} raises with slope V_{in}/L_1. During $dT \le t \le (d+ d')T$, i_{L1} falls with slope $-(V_o - V_{in})/ L_1$. Therefore

$$\Delta_{iL1} = \frac{V_{in}}{L_1} dT = \frac{V_o - 2V_{in}}{L_1} dT \tag{2}$$

The above Eq. (2) can be simplified as

$$\Delta_{il1} = \frac{V_{in}}{L_1} dT = \frac{V_o - 2V_{in}}{L_1} dT \tag{3}$$

In the constant state condition, the average capacitor current is zero. Considering the current flowing through the output capacitor Co in Fig. 1(b), (c), (d), and it has the following relations;

$$\Delta_{il1} = \frac{V_{in}}{L_1} dT = \frac{V_o - 2V_{in}}{L_1} dT \tag{4}$$

By $\Delta i_{L1} = \frac{V_o}{L_1} dT$ from (2) $I_o = \frac{V_o}{R}$ and $T = \frac{1}{f}$ substituting in (4) and this can be expressed as (5)

$$\frac{1}{2} \frac{V_{in} d' d}{f L_1} = \frac{V_o}{R_o} \tag{5}$$

Combining (3) and (5) and it becomes

$$d' = \frac{dV_{in}}{V_o - 2V_{in}} = \frac{2fL_1 V_o}{V_{in} dR} \tag{6}$$

Next, define the voltage transfer gain G = V_o/V_{in} in Eq. (6) and then, it can be found as (7)

$$d' = \frac{d}{G-2} = \frac{2fL_1 G}{dR} \tag{7}$$

Therefore,

$$G^2 - 2G - \frac{d^2 R}{2L_1 f} = 0 \tag{8}$$

Solving the Eq. (8), then voltage transfer gain can be expressed as (9)

$$G = \left(1 + \sqrt{1 + \frac{d^2 R}{2L_1 f}} \right) \tag{9}$$

The condition of DCM of POESLLC is expressed as Eq. (1) and substituting (1) in (7). Therefore,

$$d + \frac{d}{G-2} < 1 \Rightarrow \frac{d}{G-2} < 1 - d \Rightarrow G > 2 + \frac{d}{1-d} \tag{10}$$

Substituting (9) into (10) and it can be engraved as (11) The (11) is the DCM condition of the POESLLC.

$$\left(1 + \sqrt{1 + \frac{d^2 R}{2L_1 f}} \right) > 2 + \frac{d}{1-d} \Rightarrow \sqrt{1 + \frac{d^2 R}{2L_1 f}} > 1 + \frac{d}{1-d}$$

$$\Rightarrow \frac{d^2 R}{2L_1 f} > \left(\frac{d}{1-d} \right)^2 + \frac{2d}{(1-d)} \Rightarrow \frac{R}{2L_1 f} > \frac{2-d}{(1-d)^2} \tag{11}$$

2.2 State Space Averaging Modeling of POESLLC in DCM

In state 1 operation, when the switch Q is ON, the diode D_1 conducts. The capacitor C_1 is charged by supply voltage V_{in} in short duration of time period and this capacitor voltage is assumed a steady value. The current through the inductor i_{L1} rises with V_{in}. The output capacitor, C_o provides the energy to the output load. The equivalent circuit of POESLLC in state 1 operation is shown in Fig. 1(b). The state space equation can be engraved as (12)

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{in} \\ C_o \frac{dV_o}{dt} = -\frac{V_o}{R} \end{cases} \quad \text{Switch ON} \tag{12}$$

During the state 2 operation, switch Q is in OFF state, diode D_2 conduct and hence, the inductor current decays with voltage of -(V_o-2V_{in}) to offer energy to C_o and R. The equivalent circuit of POESLLC in state 2 is shown in Fig. 1(c). The state space equation of can be written as (13)

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = 2V_{in} - V_o \\ C_o \frac{dV_o}{dt} = i_{L1} - \frac{V_o}{R} \end{cases} \quad \text{Switch OFF} \tag{13}$$

Using the capacitor charge balance rule on C_1, the Eq. (14) for whole switching time period can be written.

$$dC_1 \frac{dV_{C1}}{dt} + (1-d) i_{L1} = 0 \tag{14}$$

where, d is duty cycle.

During the DCM operation (refer the Fig. 1 (d)), the state space equation can be expressed as

$$\begin{cases} \frac{di_{L1}}{dt} = 0 \\ \frac{V_o}{R} + C_o \frac{dV_o}{dt} = 0 \end{cases} \tag{15}$$

As there are two capacitor in the POESLLC, which are $V_{C1} = V_{in}$, V_o, it is only need to choose as a state space variable except V_{in}. Jointly with inductor current i_{L1}, all state space variables of the POESLLC are selected such as the inductor current i_{L1}, and voltage V_o respectively x_1, and x_2.

Combining (12), (13), (14) and (15), the state-space average modeling of the POESLLC may be reached as

expressed by (16).

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{V}_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{d'}{L_1} \\ \frac{d'}{C_o} & -\frac{1}{RC_o} \end{bmatrix} \begin{bmatrix} i_{L1} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{d+2d'}{L_1} \\ 0 \end{bmatrix} V_{in} \quad (16)$$

From Eq. (16), it can be seen only inductor exists and the x consists of two variable, the modification matrix "W" is expressed as (17)

$$W = \begin{bmatrix} \frac{1}{d+d'} & 0 \\ 0 & 1 \end{bmatrix} \quad (17)$$

Therefore, the modified averaged model of POESLLC in DCM can be written as (18)

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{V}_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{d'}{L_1} \\ \frac{d'}{C_o} & -\frac{1}{RC_o} \end{bmatrix} W \begin{bmatrix} i_{L1} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{d+2d'}{L_1} \\ 0 \end{bmatrix} V_{in}$$

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{V}_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{d'}{L_1} \\ \frac{d'}{C_o(d+d')} & -\frac{1}{RC_o} \end{bmatrix} \begin{bmatrix} i_{L1} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{d+2d'}{L_1} \\ 0 \end{bmatrix} V_{in}$$

$$A = \begin{bmatrix} 0 & -\frac{d'}{L_1} \\ \frac{d'}{C_o(d+d')} & -\frac{1}{RC_o} \end{bmatrix}, B = \begin{bmatrix} \frac{d+2d'}{L_1} \\ 0 \end{bmatrix}, \quad (18)$$

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix}, D = 0$$

The design parameters are substituted in (18) and then A, B, C and D matrices becomes

$$A = \begin{bmatrix} 0 & 1121.76 \\ 22727.27 & -109.10 \end{bmatrix}, B = \begin{bmatrix} 33632.287 \\ 0 \end{bmatrix}, \quad (19)$$

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix}, D = \begin{bmatrix} 0 & 0 \end{bmatrix}$$

3. Proposed Control Structure for POESLLC

The main purpose of this section is to discuss about the controllers for expeditious performance of converter. The specifications of POESLLC is shown in Table 2. The two loop control scheme is the most relevant because it bestows excellent functioning under nonlinear loads, sudden load variations and transient short-circuit conditions [20-22]. The suggested PIC/FLC plus SMC combinations for a POESLLC in DCM is depicted in Fig. 2. Here, the designed controllers are earmarked for individual responsibilities into two loops namely, an inner current loop where the SMC adjusts the inductor current, and an outer voltage

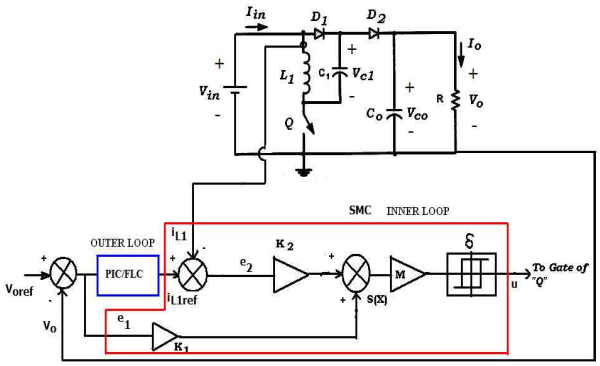


Fig. 2. POESLLC with the suggested confronting feedback control structure and controllers

control loop utilizing either PIC or FLC to maintain the output voltage constant. The input to the PIC/FLC is the output voltage error and the output establishes the mean values of reference inductor current for inner loop. The inputs to the SMC are output voltage error e1 and the inductor current error e2. The output of SMC, u, is the regulated signal, which in turn sets the new duty ratio of the switching pulse driving the power MOSFET switches of the POESLLC in DCM.

3.1 Design of SMC

Phase variable transformation technique is used to imply the POESLLC in DCM, but keeping the sliding surface $\sigma(\varepsilon,t)$, the model of the POESLLC (DCM) in phase-variable form is expressed as Eq. (20)

$$\dot{X} = AX + Bu \quad (20)$$

where

$$A = \begin{bmatrix} 0 & 1121.76 \\ 22727.27 & -109.10 \end{bmatrix}, B = \begin{bmatrix} 33632.287 \\ 0 \end{bmatrix} \quad (21)$$

The switching function of the converter is expressed as Eqs. (22) and (23)

$$\sigma = N_1\varepsilon_1 + N_2\varepsilon_2 \quad (22)$$

$$\sigma(X) = X_1 + N_1X_2 \quad (23)$$

where, ε_1 and ε_2 are the errors of the converter and it can be written as Eq. (24)

$$\varepsilon_1 = \begin{bmatrix} i_{L1ref} - i_{L1} \end{bmatrix}, \ \varepsilon_2 = \begin{bmatrix} V_{oref} - V_o \end{bmatrix} \quad (24)$$

The tracking vector of the NOESLLC is written as Eq. (25)

$$\sigma(\varepsilon,t) = \begin{bmatrix} N \end{bmatrix} \begin{bmatrix} \varepsilon \end{bmatrix} \quad (25)$$

The error vector in the sliding surface is always to

maintain for all the time $\sigma(\varepsilon,t)=0$ and also the controller co-efficient vectors $N=[N_1 N_2]$ and $N_1, N_2 > 0$

$$\sigma(\varepsilon,t)=[\,N\,][\,\varepsilon\,] \tag{26}$$

The sliding surface of the second order converter is reduced into get the first order model through the differential equations and it can be written as Eq. (27)

$$\begin{aligned}\dot{\varepsilon} &= \dot{H}-\dot{X} \\ \dot{\varepsilon} &= \dot{H}-AX+Bu\end{aligned} \tag{27}$$

Substituting (A), $X=H-\varepsilon$ in (27) and Filippov's equivalent switch control u_{eq} that pledges the $\dot{\sigma}(\varepsilon,t)=0$ and it can be symbolized as Eq. (33)

$$\dot{\sigma}=N\varepsilon=[\,N\,]\left[\,\dot{H}-AH+A\varepsilon-Bu_{eq}\,\right]=0 \tag{28}$$

The converter control signal is estimated using the Eq. (28) and it will be written as Eq. (29)

$$u_{eq}=[\,NB\,]^{-1}N\left[\,\dot{H}-AH+A\varepsilon\,\right] \tag{29}$$

By substituting Eq. (29) in Eq. (27)

$$\dot{\varepsilon}=\dot{H}-AH+A\varepsilon-B(NB)^{-1}N\left[\,\dot{H}-AH+A\varepsilon\,\right] \tag{30}$$

$$\dot{\varepsilon}=\left[\,I-B(NB)^{-1}N\,\right]\left[\,\dot{H}-AH+A\varepsilon\,\right] \tag{31}$$

Substituting $[\dot{H}-AH]=0$ (invariance conditions) in Eq. (31) the expression has been simplified as

$$\dot{\varepsilon}=\left[\,I-B(NB)^{-1}N\,\right]A\varepsilon=A_{eq}\varepsilon \tag{32}$$

If $(NB)^{-1}$ exists, the vector N is derived by choosing the eigen values of A_{eq} such that it guarantees the asymptotic convergence of error to zero at the desired value. The matrix A_{eq} is selected to satisfy Eq. (32) and it is expressed as

$$A_{eq}=\begin{bmatrix}-6.6 & 0\\ 0 & -6.2\end{bmatrix} \tag{33}$$

The values of matrix N is then found using Eq. (32) as

$$N=[\,N_1 N_2\,]=[\,1 \quad 2.2\,] \tag{34}$$

Thus, the sliding manifold σ is given by

$$\sigma=N_1\varepsilon_1+N_2\varepsilon_2 \tag{35}$$

Eq. (35) marks that if the NOESLLC works in stable mode (when σ = 0, stability condition), the dynamics of errors ε_1 and ε_2 be possible exponentially to zero with a time ratio of N_1/N_2. Even as in the step transient's period, the POESLLC in DCM is in reaching mode, and so for this exploit N_1 and N_2 are evaluated to be in 1 and 2.2, respectively. In addition, the Eq. (27) describes the error action under SMC. Once the sliding surface σ (ε, t) = N ε is designed then the control law for hitting condition is defined as

$$\begin{aligned}u &= M\,\mathrm{sgn}(\sigma)x_2 \\ &= Ux_2\end{aligned} \tag{36}$$

where,

$$\begin{aligned}U &= 1 \; for \sigma > \delta \\ U &= 0 \; for \sigma < \delta\end{aligned}$$

(U =1 when the switch is the conduction subinterval, and U = 0 when the diode is the conduction subinterval).

In this case, hysteresis bandwidth δ = 0.05 is selected by trial and error iterative method (based on the system performance). Eq. (41) is used to derive the gate pulse to drive power MOSFETs of converter, which in turn control dc output voltage, steady state error and inductor current. In this study, M is constant number and equal to unity so that σ $\dot{\sigma}$=0 (existence condition is fulfilled). The reaching condition guarantees that the tracking error phase trajectory is asymptotically involved to σ = 0 (stability condition). It is shown that the (41) does not depend on the working regions, system parameters and limited disturbances. This is achieved as long as the control input u is more enough to maintain the converter subsystem in sliding mode.

$$\sigma(X)=X_1+N_2X_2 \tag{37}$$

where, N^T = [1, N_2] is the vector of sliding surface coefficients which correspond to N in Eq. (33)

$$\dot{\sigma}(X)=\begin{cases}N^TAX+N^TBU^{+}+C^TD, for \sigma(X)>0\\ N^TAX+N^TBU^{+}+C^TD, for \sigma(X)<0\end{cases} \tag{38}$$

Then, substituting the values of A, B, and N, the above equation can be expressed by

$$\begin{aligned}S(X_1) &= 22727.27N_2X_1-11210.76N_1X_1 \\ &+109.1N_2X_2\end{aligned}$$

Equations $\sigma_1(X) = 0$ and $\sigma_2(X) = 0$ define two lines in the state plane with the same slope flowing through the origin. These equations signify the sliding surface for switch ON/OFF states regions, which are inadequate to single the sliding surface of a given converter with SMC plus FLC/PIC for N_1, N_2. The phase trajectory of SMC, it is evidently observed that the suitable value of N_2 controls the dynamic response of the system competently. Once the phase trajectory is on top of the sliding surface, the switch

is turned off state (U= 0) and when the phase trajectory is lower the sliding surface, the switch is turned on state (U=1).

3.2 Design of PI controller

A PI controller is chosen for providing the good output voltage regulation for POESLLC. In this case, the PI controller output sets the average reference inductor current for inner current loop. The PI controller parameters, proportional gain (K_p) is computed using Zeigler – Nichols tuning method. The PI controller parameter proportional gain (K_p) is obtained by using Zeigler–Nichols tuning method [23-26]. After the tuning the controller using this method, the POESLLC is providing a sustained oscillation with ultimate gain for stability can be found by K_{cr}=0.4s. Using this method the values of $K_p=K_{cr}/2=0.2$ is found.

3.3 Description of fuzzy logic controller

Perusal of fuzzy logic system in dc–dc converters is being studied by many researchers. A few of the good renowned benefactions are given concisely here, accompanied by the description of a basic fuzzy control algorithm.

3.3.1. Relevant works

In a fuzzy logic controller, the control action mechanism is extracted from the estimation of a set of simple linguistic rules. The establishment of the rules need a profound understanding of the process to be governed, but mathematical model of the system for fuzzy control is not essential. As a consequence, the technique is common and so the same control action mechanism can be given to another type of dc–dc converter. Industrialist and researchers have been examined the application areas of fuzzy logic control strategy for enhancing the control of switching-mode power converters. Despite, the execution of logic and arithmetic calculation of fuzzy logic algorithm is very hard on many micro controllers. So DSPs with complicated peripherals are used by most researchers and are still existing at the simulation state [27-30]. Fuzzy logic control has been enforced on microcontroller for exerting control over dc–dc converters in an effective manner [30] This yields the suitable techniques and recommendations in the incorporation of fuzzy logic controllers on a micro-controller. With regard to examine the possibility to execute a fuzzy control algorithm for a real-time dc–dc converter on a low-cost microcontroller, a fuzzy logic POESLLC has been implemented using a PIC16F877A microcontroller.

3.3.2. Basic fuzzy algorithm:

The fuzzy control system algorithm is detailed by dc–dc converter as a platform. Block diagram of the fuzzy logic control for a dc–dc converter is shown in Fig. 3. The arrangement is carried out which is same as to [31]. The

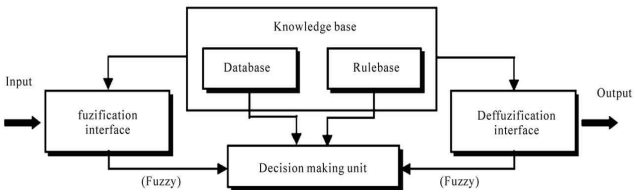


Fig. 3. fuzzy inference system

output voltage of the dc–dc converter is ranged and sampling is taken by an A/D converter. Sampled data is used by the microcontroller to set the inputs to the fuzzy control algorithm. Fuzzy inputs are the error and change in error. The fuzzy control algorithm is classified into three parts. Three parts are fuzzification, decision making and defuzzification.

3.3.3. Overview of Fuzzy Inference System

Non linear mapping has been delivered by fuzzy inference system from its input to output set. Firstly a fuzzy inference system comprises five operating blocks as shown in Fig. 3. The arrangement of the fuzzy inference model is explained as follows

1. A rule base has fuzzy if-then rules.
2. Data base decides the member functions of fuzzy set.
3. A decision-making unit produces the inference functions on the if-then rules.
4. Fuzzification interface converts the crisp inputs into degrees of match with linguistic values.
5. Transformation of the fuzzy inference output into a crisp output values is done by defuzzification interface.

Knowledge base consists rule base and data base. Fuzzy if-then rules are statements of the form as follows: If x is A Then y is B. where, x and y are input and output linguistic variables. Fuzzy values A and B are told by the membership functions. The membership functions are distinctive and problem based. The fuzzy reasoning functions are executed by Fuzzy Inference System(FIS) and are pointed as follows

1. The input variables are compared with the membership functions on the antecedent part for getting the membership values of each linguistic label. This is called fuzzification.
2. The membership values on the premise part is combined to obtain firing strength of each rule.
3. Qualified consequents of each rule are generated with respect to the firing strength.
4. Qualified consequents are aggregated to create a crisp output. This is called defuzzification.

Fuzzy reasoning methods are Mamdani and Sugeno type models [32-34]. The general dissimilarities between Mamdani-type FIS and Sugeno-type FIS is the response that the crisp output is generated from the fuzzy inputs. Mamdani-type FIS establishes the technique of defuzzifi-cation of a fuzzy output and Sugeno-type FIS establishes

weighted average to formalize the crisp output Mamdani FIS leads to hefty computational load. But Sugeno FIS is computationally competent which creates it very charming in distinctive application. Also Sugeno FIS operates optimization and adaptive techniques comfortably. Mamdani FIS has bit adaptability and responsive in design of system when it is compared to Sugeno-type FIS.

Fuzzification:

Seven fuzzy sets are selected [35] and confined by the following study of fuzzy-set values and it is mentioned as error and change in error. The selected fuzzy levels depends on the resolution of input. When the fuzzy levels are larger, the input resolution is higher. The fuzzy control is executed and brings the triangular fuzzy-set values. The triangular functions are utilized to decrease the intricacy in calculation [36] when it is comparison with trapezoidal and bell shaped functions. Henceforth, the fuzzy specification of quantified values e and ce are the fuzzy sets.

Decision making:

Decision making unit contains data base and rule base and it allies the fuzzy output to the fuzzy inputs which are developed from knowledge of the system behaviour. The FLC's fuzzy interference systems (FIS) with assigned inputs and output is shown in Fig. 4 (MATLAB). The output voltage error (e) and its change in voltage error (de) of POESLLC is applied as a input to the FLC and the output is o(mark the reference current for the inductor). For suitability, the arithmetic ranges of the inputs/output of the FLC can be normalized and expressed as pursues: e = [-0.1 -0.062 -0.036 0 0.036 0.062 0.1], ce =[-0.2 -0.14 -0.06 0 0.06 0.14 0.2] and o=[-0.1 -0.06556 -0.03334 0 0.03334 0.06556 0.1] and its related fuzzy sets are [NB, NM, NS, Z, PS, PM, PB]. The membership functions of the error (e), change in error (ce) are marked in Fig.4.

Defuzzification:

Sugeno FIS is more reliable in system design when it compares to Mamdani FIS. Time consuming defuzzification process is good in weighted average method of Sugeno FIS. The final response of the system is corroborated by weighted average method. [37]. The assortment of FLC rules completely depends on the performance characteristics of the POESLLC. In this study, 49 rules are structured (refer the Table 1). Subsequently, the weighted average method (defuzzification-method) is utilized to complete the fuzzy design which is shown as output 'o'.

Table 1. Fuzzy Rule for POESLLC in DCM

e / ce	NB	NM	NS	Z	PS	PM	PB	NB
NB	NB	NB	NB	NB	NM	NS	Z	NB
NM	NB	NB	NM	NM	NS	Z	PS	NB
NS	NB	NM	NS	NS	Z	PS	PM	NB
Z	NB	NM	NM	Z	PS	PM	PB	NB
PS	NM	NS	Z	PS	PS	PM	PB	NM
PM	NS	Z	PS	PM	PM	PM	PB	NS
PB	Z	PS	PM	PB	PM	PB	PB	Z

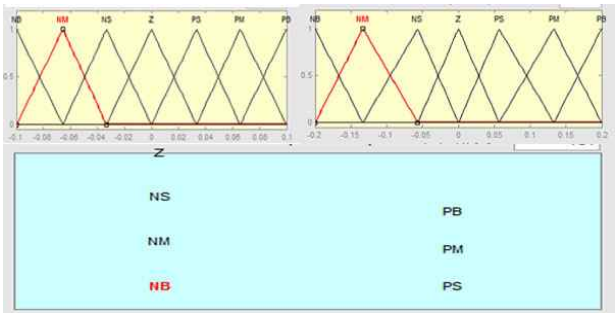


Fig. 4. Membership function for input 1, input 2 and Output variable

3.4. Implementation work

The features of PIC 16F877A are low priced, extensive usage, wide compilation of unique application materials, availability of development tools at free of cost, reprogrammable flash memory capability and serial programming.

The following points are the implementation of POESLLC using a PIC16F877A microcontroller.

1) The ADC module for the PIC16F877A captures a snapshot of the scaled output voltage and holds it for A/D conversion. Because of the limited sampling rate and computation power of the PIC16F877A, switching noise in the output voltage must be avoided or filtered out in "hardware" instead of by a digital filter. Therefore, the output voltage should be sampled during the period that has minimum switching noise. In this implementation, the PWM signal is sent back to another I/O pin to trigger an interrupt that starts an A/D conversion. As a result, the sampling moment can be controlled and the output voltage can always be captured after the switching noise has subsided. The PIC16F877A does not comprise priority levels for interrupts. For ascertaining the sampling moment, an interrupt from any other source should not be admitted. In this execution, the interrupt service routine (ISR) also keeps all logical and mathematical calculations, and the main routine simply waits for the next interrupt after all the calculations have been finished. Since the A/D conversion time is much faster than total calculation time, the controller sampling frequency is directly determined by the speed of the calculations.
2) Since the ADC module has an 8-bit resolution, the error to measure the possible full range of output voltage can be easily more than 0.12 V. For getting higher A/D resolution, a level-shift circuit has been modeled such that the A/D result comprises a "windowed" output voltage range around the nominal value. An external voltage buffer (voltage follower) is needed to ensure accurate measurement of the output voltage. Due to limited analog I/O ports PIC16F877A, the complete range of output voltage is not measured. Despite, this limitation does not reduce the function of the controller

because the output voltage variance is always kept inside the windowed range during disturbance periods. An appropriately designed voltage loop compensator can limit the overshoot during start up to a small value.

3) The DAC module inside the PIC16F877A is used to convert the output of the fuzzy logic controller into an analog signal, and its output V_c should be compatible with the sensed current signal as shown in Fig. 6. Because of the small sense resistor, the sensed current signal is very little than V_c for a preferred DAC reference voltage. For the PIC16F877A, the DAC reference voltage can be either 5 or 3.072 V. One simple and effective solution is to add a simple voltage divider made of two external resistors at the DAC output.
4) The control rule table is stored as a look-up table containing the weighted average of the output fuzzy sets. The fuzzy sets (output fuzzy sets) observe the universe of discourse as shown in Fig. 4. The range for the universe of discourse is limited, because only seven output fuzzy sets are chosen; The degree to which belongs to each fuzzy set is not stored but calculated. It takes an average of 250 µs for the microcontroller to execute the complete modified fuzzy control program, which involves sampling the output voltage, calculating the new duty cycle, and improving the PWM output. In order to ensure that, the microcontroller executes the complete program between successive samples, the sampling rate is set for 275 µs.

4. Simulation and Experimental Results

This section deals about the simulation and experimental results of POESLLC in DCM using FLC/PIC plus SMC. The POESLLC in DCM performance is verified at various conditions viz. start-up transient, line variation, load variation, and also circuit components variations. The laboratory prototype and MATLAB/SIMULINK simulation models are performed on the POESLLC in DCM with specifications listed in Table 2. The hardware model of the same converter with implemented FLC/PIC plus SMC is shown in Fig. 5. The details of the power circuits are as follows:

Q - IRFP 250 (MOSFET); D_1 & D_2- UF5408 (Diodes)
C_1, C_o–4.7µF, 22µF/100 V;L1 - 45µH/5A (Ferrite Core)
IR2110 Driver

Table 2. Details of POESLLC with PIC/FLC plus SMC

Parameters name	Symbol	Value
Input Voltage	V_{in}	12V
Output Voltage	V_o	36V
Inductor	L_1	44.6µH
Capacitor	C_1,C_0	4.7 µF and 22 µF
Switching frequency	F	20kHz
Load resistance	R	416.6 Ω
Average input current	I_{in}	0.269A
Efficiency	η	96.48%
Average output current	I_o	0.08641A
Duty ratio	D	0.5
Peak to Peak Inductor Current Ripple	Δ_{iL1}	25% of I_{in}
Capacitor Ripple Voltage	ΔV_0	12V

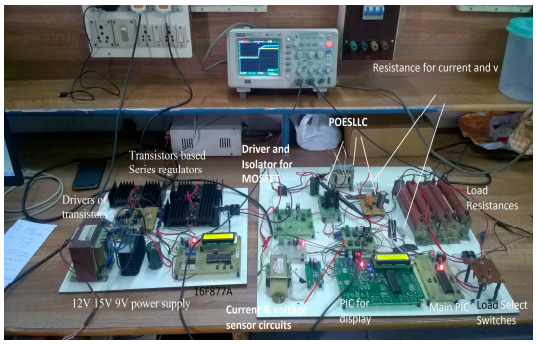


Fig. 5. Experimental model of POESLLC with PIC/FLC plus SMC system

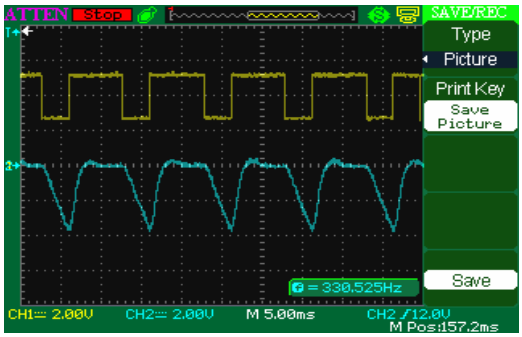


Fig. 6. Inductor current and Gate pulse

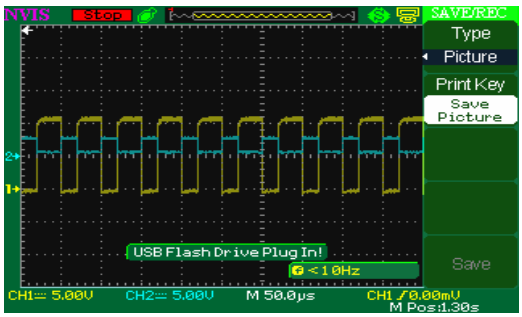


Fig. 7. Gate pulse before and after driver

The output voltage of the POESLLC is fed to analog to digital converter (ADC) of 16F877A processor via. signal conditioning circuit and isolation circuit. The PIC compares the measured output voltage and the reference output voltage. The error and change in error are processed by the SMC plus FLC/PIC algorithms in the 16F877A processor to suitably adjust the duty cycle of the PWM signal to the MOSFETs of the converter. The opto-coupler 6N137 is used for isolation between the power circuit and control unit. Driver circuit IR 2110 is used to amplify the pulses of the MOSFETs. Hardware implementation is done

using a 16F877A processor. Few waveforms resulted in implementation are demonstrated from Fig. 6 to Fig. 7.

4.1 Start-up Region

Fig. 8 shows the simulated output voltage results of POESLLC in DCM using the PIC plus SMC and FLC plus SMC in start-up transient region with nominal input voltage. From this figure, it is evident that the output voltage of the POESLLC in DCM has null overshoots, settling time of 0.0005 s using FLC plus SMC, but the same converter with PIC plus SMC has produced peak overshoots and settling time of 0.006s during start-up transient region. Fig. 9 shows the experimentally recorded start up transient. The corresponding time domain specification during start up is shown in Table 3.

4.2 Line variation

The response of output voltage for input step change from 12V to 15 V at time of 0.025s with R = 416.6Ω is provided in Fig. 10.(a) as normal view, and as an enlarged view in Fig. 10(b). Similarly, the input current and its enlarged view of inductor current are presented in Fig.

Table 3. Time domain specification during start up

Time Domain Specification	PIC plus SMC	FLC plus SMC
Delay Time	0.00071	0.0001
Rise Time	0.00086	0.0002
Peak Time	0.0009	0.0003
Settling Time	0.006	0.0005
Peak overshoot	2.3V	-

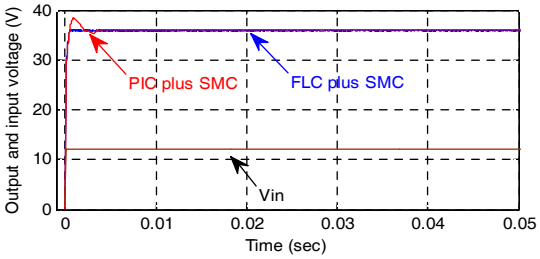


Fig. 8. Simulated output voltage responses of POESLLC in DCM using both control methods in transient region with rated input voltage (12V)

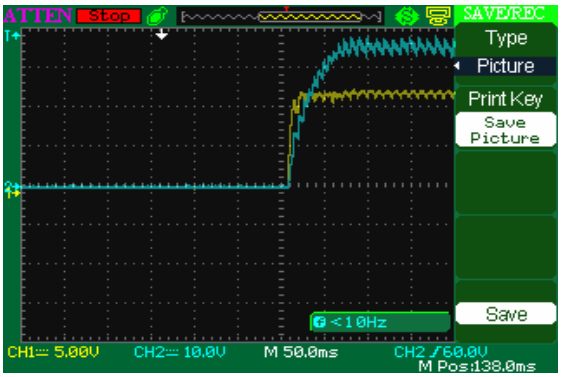
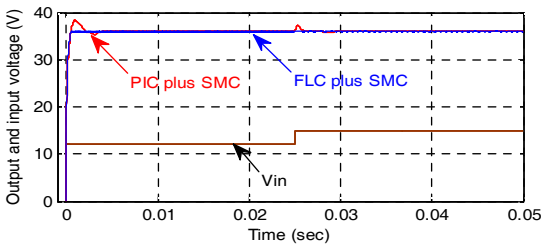


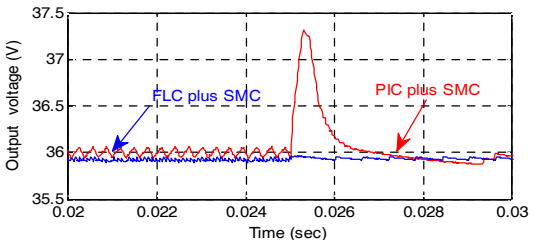
Fig. 9. Start up transients with V_{in}=12V

Table 4. Time domain specification during line disturbance 12V to 15V

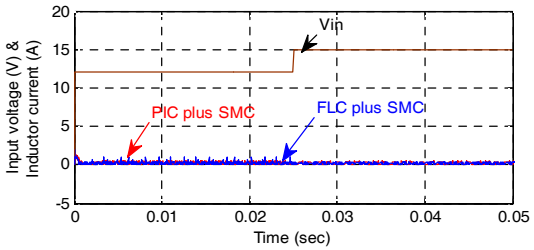
Time Domain Specification	PIC plus SMC	FLC plus SMC
Delay Time	0.00084	0.0002
Rise Time	0.0009	0.00039
Peak Time	0.00095	0.00041
Settling Time	0.007	0.00052
Peak overshoot	2.35V	-



(a)



(b)



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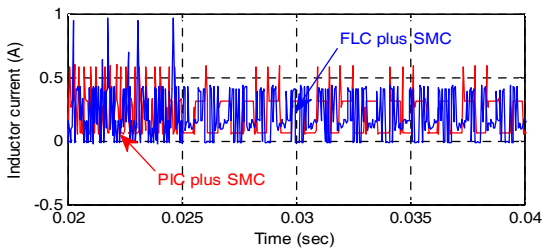


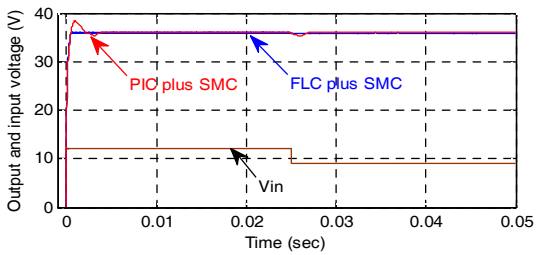
(d)

Fig. 10. Response of output voltage for input step change from 12V to 15 V at time of 0.025s with R = 416.6Ω, (a) Normal view, (b) Enlarged view (c) Input voltage and input current (d) Enlarged view of inductor current

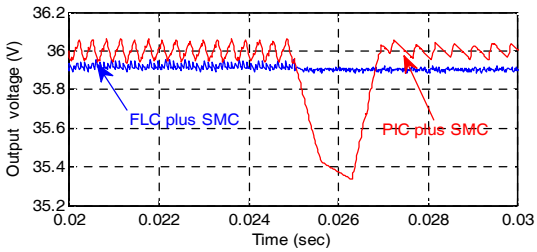
10(c) and (d) respectively. The corresponding time domain specification is tabulated in Table 4. The same kind of study for input step change from 12V to 9 V is also performed and detailed in Fig. 11(a), (b) and Table 5. The corroborated disturbance rejection property of developed feedback FLC plus SMC for input step change from 12V to 9V is also kept abreast in Fig. 12.

Table 5. Time domain specification during line disturbance 12V to 9V

Time Domain Specification	PIC plus SMC	FLC plus SMC
Delay Time	0.00068	0.00025
Rise Time	0.00079	0.00031
Peak Time	0.00085	0.00035
Settling Time	0.0068	0.00049
Peak overshoot	2.35V	-



(a)



(b)

Fig. 11. Response of output voltage for input step change from 12V to 9 V at time of 0.025s with R = 416.6Ω, (a) Normal view, (b) Enlarged view

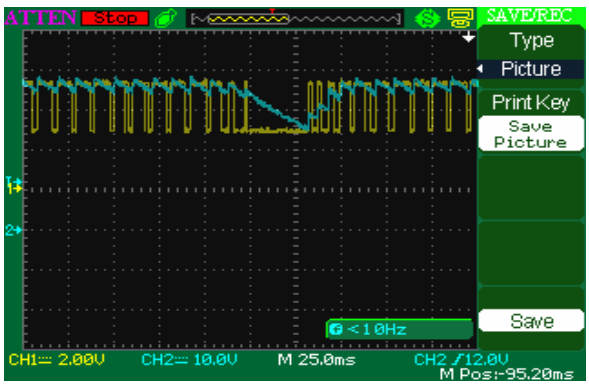


Fig. 12. Evidenced disturbance rejection property of developed feedback FLC plus SMC for input step change from 12V to 9V - Output voltage and gate pulse

4.3 Load variation

Both the step increasing and decreasing disturbances in load (Load change 416.6Ω to 516.6 Ω and 416.6 Ω to 316.6Ω) are studied. The responses of load change 416.6Ω to 516.6 Ω are given in Fig. 13(a) and (b). The responses of load change (416.6Ω to 316.6 Ω) are given in Fig. 14(a) and (b) as well as in Table 6 and Table 7.

4.4 Circuit Components variations

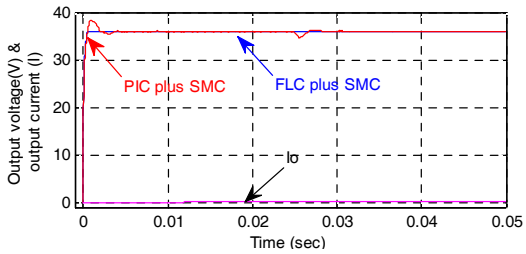
Response of output voltage and output current for inductor variation (44.6mH to 90mH) and capacitor variation (22μF to 32 μF) are shown in Fig. 15(a), (b) and 16(a), (b). Also, time domain specification for variation of

Table 6. Time domain specification during load disturbance from 416.6Ω to 516.6Ω

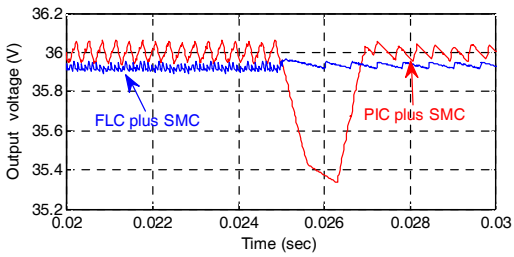
Time Domain Specification	PIC plus SMC	FLC plus SMC
Delay Time	0.00045	0.0003
Rise Time	0.00062	0.00042
Peak Time	0.00056	0.00045
Settling Time	0.0063	0.00023
Peak overshoot	2.29V	-

Table 7. Time domain specification (416.6Ω to 316.6Ω)

Time Domain Specification	PIC plus SMC	FLC plus SMC
Delay Time	0.000395	0.00026
Rise Time	0.00048	0.00039
Peak Time	0.00056	0.00044
Settling Time	0.007	0.00058
Peak overshoot	2.4V	-

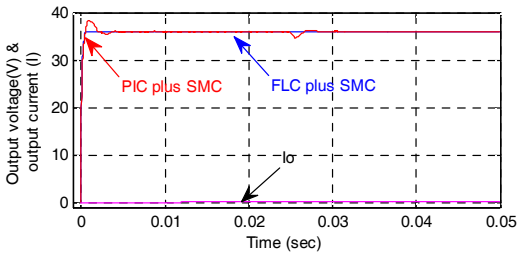


(a)

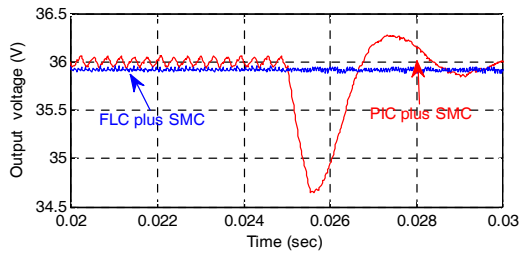


(b)

Fig. 13. Response of output voltage for Load change 416.6Ω to 516.6Ω at time of 0.025s with R = 416.6Ω, (a) Normal view, (b) Enlarged view

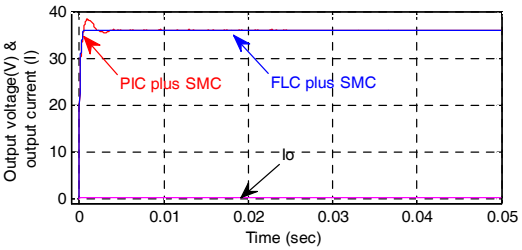


(a)

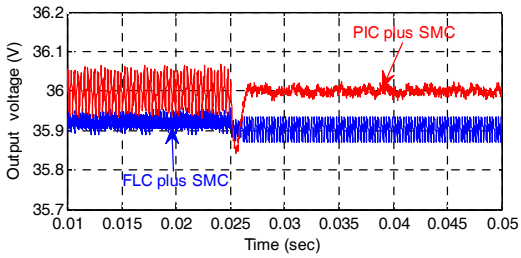


(b)

Fig. 14. Response of output voltage for Load change from 416.6Ω to 316.6Ω at time of 0.025s with R = 416.6Ω, (a) Output voltage and output current (b) Enlarged view of output voltage



(a)



(b)

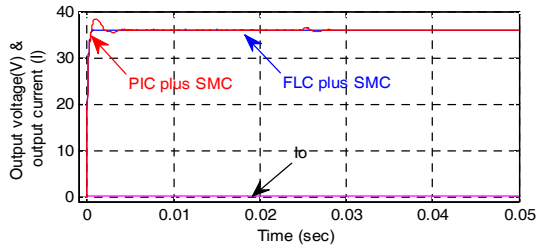
Fig. 15. Output voltage for inductor change 44.6mH to 90mH at time of 0.025s with R = 416.6Ω, (a) Output voltage and output current (b) Enlarged view of output voltage

Table 8. Time domain specification (inductor change)

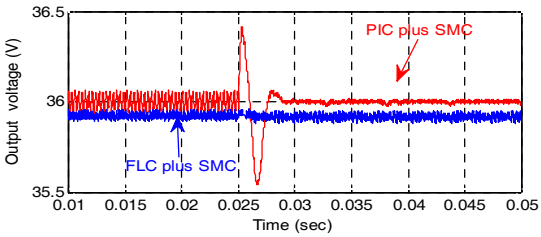
Time Specification	PIC plus SMC	FLC plus SMC
Delay Time	0.00068	0.00019
Rise Time	0.000864	0.000245
Peak Time	0.00095	0.00032
Settling Time	0.0064	0.00054
Peak overshoot	2.32V	-

Table 9. Time domain specification(capacitor change)

Time Specification	PIC plus SMC	FLC plus SMC
Delay Time	0.00028	0.00009
Rise Time	0.00032	0.00024
Peak Time	0.00044	0.00031
Settling Time	0.005	0.0004
Peak overshoot	2.5V	-

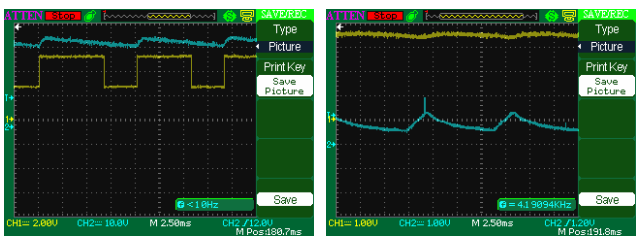


(a)



(b)

Fig. 16. Response of output voltage for capacitor change 22μF to 32μF at time of 0.025s with R = 416.6Ω, (a) Output voltage and output current (b) Enlarged view of output voltage



(a) (b)

Fig. 17. (a) Output voltage and gate pulses (b) Sensed inductor current and voltage

inductor and capacitor is shown in Tables 8 and 9. Further, output voltage, gate pulse and sensed inductor current are shown in Fig. 17(a), (b).

4.5. Comparison of POESLLC'S FLC plus SMC over PI plus SMC controller:

From the time domain specification of Tables 3 to 9. all cases are illustrated in Figs. 18 (a) to (g) respectively. From these Figs. 18(a) to (g), it can be clearly seen that the results of the designed FLC plus SMC exhibit better performance in comparison with a conventional PI

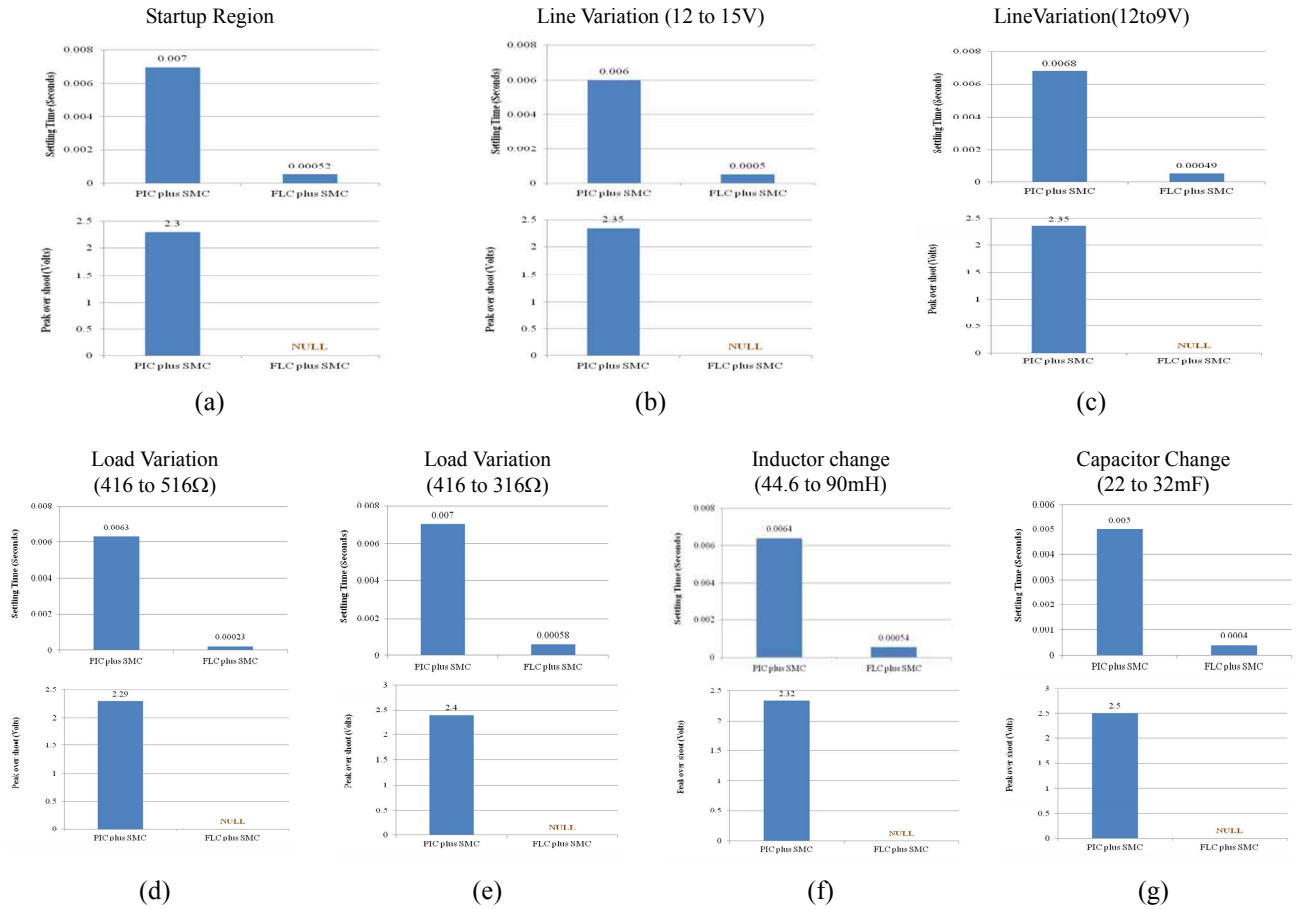


Fig. 18. Time domain performance illustration of POESLLC using PIC plus SMC and FLC plus SMC for different operating conditions. (a) Startup Region (b) Line Variation (12 to 15V) (c) Line Variation (12 to 09V) (d) Load Variation (416 to 516Ω) (e) Load Variation (416 to 316Ω) (f) Inductor change(44.6mH to 90mH) (g) Capacitor change(22mF to 32mF)

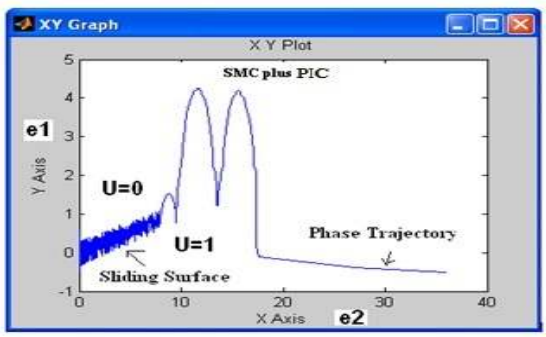


Fig. 19. (a) Performance phase trajectory of SMC plus PIC

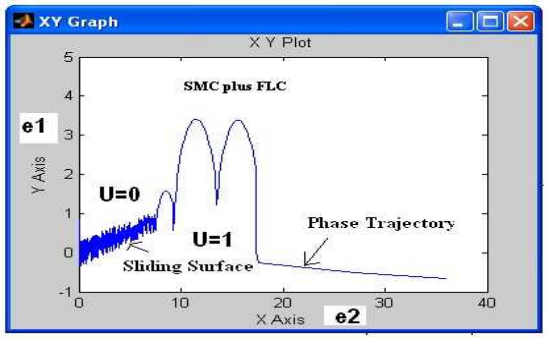


Fig. 19. (b) Performance phase trajectory of SMC plus FLC

controller (PIC) under line and load disturbances. From the Fig. 19(a) and (b), the phase trajectory of SMC is obviously understood that the appropriate value of N_2 (From Eq. (39)) governs the system dynamism efficiently. When the phase trajectory is on upper portion of the sliding surface, the switch is disconnected state (U=0) and when the phase trajectory is lower the sliding surface, the switch is connected state (U=1). Also, from the Fig. 19(b), it reveals that overshoots in the phase trajectory of the converter using the SMC plus FLC is small as compared to the SMC plus PIC. The robustness of the developed controller is affirmed for the load from 416.6Ω to 104.2Ω. i.e 75% reduction from rated value, as indicated in Fig. 20. The demerit of POESLLC by direct tracking control of the output voltage results in a non-minimum phase system and therefore it is termed as unstable controller [38]. An

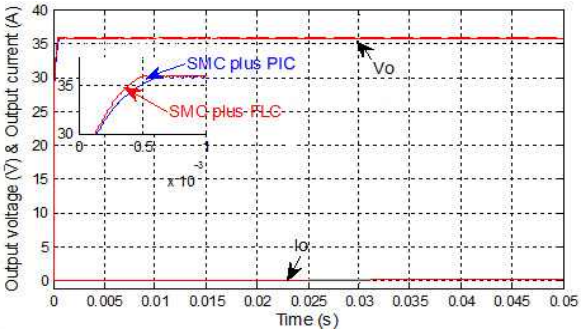


Fig. 20. Response for load change from 416.6Ω to 104.2 Ω at time of 0.025s

attempt is made to show that controlling the current can indirectly control the output voltage in converter by implementing PIC/FLC plus SMC using DCM method. The major advantages of the proposed controller in comparison with the linear controllers are robust performance against large parameter variations, possessing high-voltage transfer gain, high efficiency, minimal inductor current and capacitor voltage ripple, excellent regulation of the output voltage in different operating conditions and reduction peak overshoot, good settling time.

Further, proposed system (Designed FLC plus SMC for the POESLLC operated in DCM) expands the sovereignty of battery for all portable applications such as mobile phones, computer mother board, medical equipments, digital camera, laptop computers, and TFT-LCD bias supplies.

5. Conclusion

For high power level applications, the continuous current mode (CCM) boost-type converters are the favored due to their lower conduction loss. But, the major issues with these converters are the reverse recovery problem of the diode [39]. The diode reverse recovery not only causes extra loss in the converter, but also causes electromagnetic compatibility (EMC) problems. The EMC problem is due to the high current and voltage slew rates during the reverse recovery process. In this article, the analysis, design and implementation of high performance POESLLC is discussed in DCM. Also, the paper suggested a dual loop control structure with two different controller combinations viz. PIC/FLC plus SMC. The developed controller sliding surface coefficients and PIC/FLC rules are implemented both in MATLAB-Simulink and 16F877A processor based hardware. Experimental and simulations results are accessible to illustrate the worth of designed FLC plus SMC for the POESLLC operated in DCM reacted in rapid dynamic response, improved stability, adept regulated output voltage, non-disturbed output voltage under the circuit component disparities, small steady state error and start-up responses etc.

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