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Implementation of Multilevel Boost DC-Link Cascade based Reversing Voltage Inverter for Low THD Operation

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Abstract – In this paper, configuration of 1-ϕ seven-level boost DC-link cascade based reversing voltage multilevel inverter (BDCLCRV MLI) is proposed for uninterrupted power supply (UPS) applications. It consists of three level boost converter, level generation unit and full bridge circuit for polarity generation. When compared with conventional boost cascaded H-bridge MLI configurations, the proposed system results in reduction of DC sources, reduced power switches and gate drive requirements. Inverter switching is accomplished by providing appropriate switching angles that is generated by any optimization switching angle techniques. Here, round modulation control (RMC) method is taken as the optimization method and switching angles are derived and the same is compared with various switching angles methods i.e., equal-phase (EP) method, and half-equal-phase (HEP) method which results in improved quality of obtained AC power with lowest total harmonic distortion (THD). Reduction in DC sources and switch count makes the system more cost effective. A simulation and prototype model of 1-ϕ seven-level BDCLCRV MLI system is developed and its performance is analyzed for various operating conditions.

Keywords: Multilevel boost converter, Cascaded RV inverter, EP, HEP, RMC.

1. Introduction

Multilevel inverters (MLIs) are evolving as the innovative class of power converter alternatives for UPS applications [1]. The primary favorable circumstances of MLI's are less THD, less switching frequency and high efficiency. The THD of the output diminishes as the number of levels increase. Numerous topologies have been presented for multilevel inverters [1]. The MLIs are mainly classified as Diode clamped multilevel inverter, Flying capacitor inverter and cascaded multilevel inverters [2, 3]. These three types of MLIs require more number of components such as number of DC sources, clamping diodes, capacitors and switches. As the number of voltage levels 'm' grows, the number of active switches increase according to 2(m-1) for the conventional MLIs but it is only m+3 for the proposed cascade based reversing voltage MLI (CRV MLI) configuration [4].

MLIs have numerous configurations and several advantages. Unfortunately, the existing MLIs are unable to produce good output voltage because switching angles of the devices are not selected properly. In this paper inverter switching is accomplished by providing appropriate switching angles that is generated by any optimization switching angle techniques. Here round modulation control (RMC) method is taken as the optimization method and switching angles are derived and the same is compared with various switching angles methods i.e., EP and HEP methods, which results in good quality of output voltage with less THD [5].

On the other hand, CRV MLI requires more number of isolated DC sources to generate multiple stepped output voltage waveforms. And this kind of inverter adds to additional cost and size of the system [6]. These drawbacks can be overcome by integrating the proposed CRV MLI with the multilevel DC – DC boost converter (MBC).

Also, in order to acquire the good quality of output voltage in CRV MLI, MBC is proposed in between DC sources and level generation unit rather than the magnetic components [7]. MBCs are utilized as a part of converters where the input is DC voltage, while a higher DC voltage is required at the load, which can't be accomplished by the conventional DC – DC boost converter. Likewise, MBCs are normally utilized as interfaces between essential low-voltage DC sources. In this application, MBC is utilized for balance of DC voltages at the multilevel inverter input by a single DC source [8, 9].

In this paper, a 1-ϕ seven-level BDCLCRV MLI is simulated and developed using field programmable gate array (FPGA) for UPS applications. The Schematic diagram of proposed BDCLCRV MLI configuration based UPS system is depicted in Fig. 1. This system is characterized by its ability to supply conditioned and regulated power to a critical load during the normal and backup operations. Note that the inverter is between the

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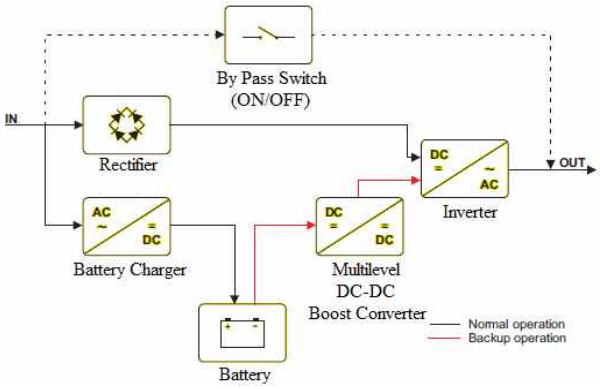


Fig. 1. Schematic diagram of BDCLCRV MLI configuration based UPS system

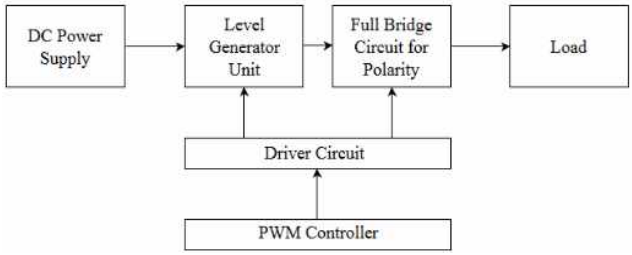


Fig. 2. Block diagram of proposed inverters using reversing voltage topology

primary source of energies (grid or battery) and the load – this system is also known as inverter-preferred or double-conversion UPS. In the case of malfunction of the inverter, the bypass switch is turned on.

2. Structure of Seven-Level BDCLCRV MLI System

The proposed BDCLCRV MLI system consists of one DC voltage source, three level boost converter and cascade based RV multilevel inverter. The block diagram and equivalent structure of BDCLCRV MLI is depicted in Fig. 2 and Fig. 3 respectively [10, 15].

Table 1 shows the required number of switches and DC sources for conventional and proposed boost DC link based RV inverter. From the analysis, it is inferred that the proposed BDCLCRV MLI system has reduced switch count and requires only single DC source than conventional boost cascade MLI systems. Therefore, reduction in DC sources and switch count makes the system more cost effective [1].

3. DC – DC Multilevel Boost Converter Configuration

The configuration of three level DC-DC boost converter is depicted in Fig. 3. It consists of conventional boost converter, (2N-1) diodes and (2N-1) capacitors. The main advantages by using the proposed topology are it can be extended to N-number of levels by adding only diodes and capacitors without modifying the main circuit, high voltage gain can be obtained without use of transformer and high duty cycle. The proposed converter consists of 3 stages which is operated at duty cycles of 0.4, 0.5 and 0.6. The operation of the three level boost converter is explained in [7].

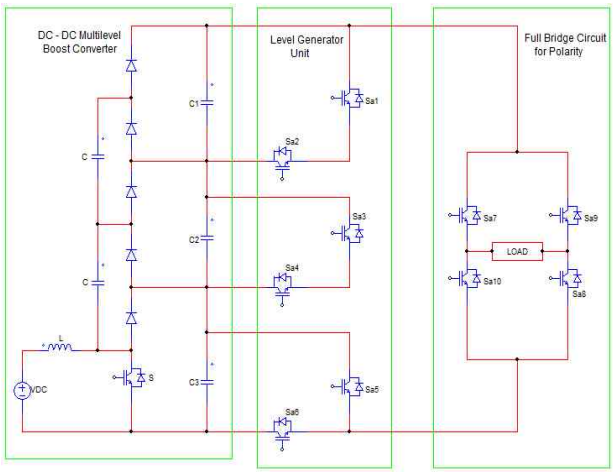


Fig. 3. Equivalent structure of BDCLCRV MLI

Table 1. Comparison of DC sources and number of switches

Number of Levels	Boost Cascade MLI (existing)		BDCLCRV MLI (proposed)	
	Number of switches	Number of DC sources	Number of switches	Number of DC sources
5	10	2	9	1
7	15	3	11	1
15	35	7	19	1
31	75	15	35	1

3.1 Analysis of DC-DC multilevel boost converter:

In this section the boost ratio will be analyzed which gives important information to designers [11]. From basic principles, the voltage gain of the conventional boost converter is given by

$$\text{Voltage gain, } \frac{V_o}{V_{dc}} = \frac{1}{1-D} \tag{1}$$

For MBC, the voltage gain is expressed as

$$\frac{V_o}{V_{dc}} = \frac{N}{1-D} \tag{2}$$

The expression for the input DC current in terms of the input-output voltage and output current is,

$$V_{dc} I_L = V_O I_O = V_O \frac{V_O}{R_O} = NV_C \frac{NV_C}{R_O} = \frac{N^2 V_C^2}{R_O} \quad (3)$$

$$\text{Therefore,} \quad I_L = \frac{V_C}{V_{dc}} . \frac{N^2 V_C}{R_O} = \frac{N^2 V_C}{(1-D) R_O} \quad (4)$$

From (4), by using duty cycle 'D' in the PWM the input current can be controlled.

Now by considering the inductor power losses, the expression of boost ratio for the MBC can be derived as follows.

$$V_L = D(V_{dc} - I_L R_L) + (1-D)(V_{dc} - V_C - I_L R_L) = 0 \quad (5)$$

$$V_{dc}(D + 1 - D) + I_L R_L(-D - 1 + D) = (1-D) V_C \quad (6)$$

$$V_{dc} = (1-D) V_C + I_L R_L \quad (7)$$

Therefore,

$$V_{dc} = (1-D) \frac{V_o}{N} + \frac{NV_O}{(1-D) R_O} R_L \quad (8)$$

$$\frac{V_{dc}}{V_O} = \frac{1}{\frac{(1-D)}{N} + \frac{NR_L}{(1-D) R_O}} \quad (9)$$

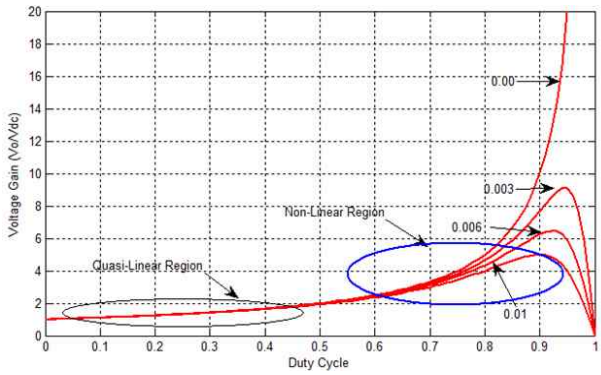


Fig. 4. Duty cycle versus voltage gain for different values of ESR/Ro (N=1)

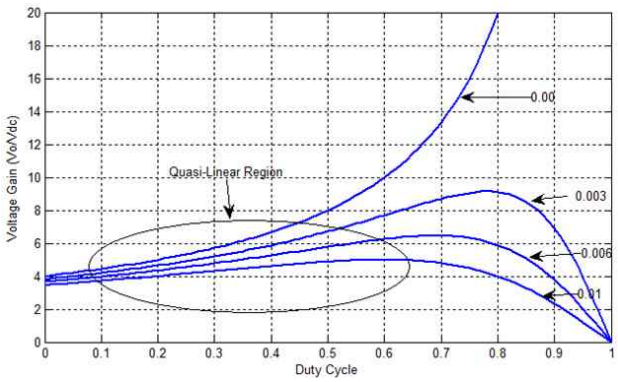


Fig. 5. Duty cycle versus voltage gain for different values of ESR/Ro in the MBC (N=3)

Eq. (9) is equal to (1) if N=1 and $R_L = 0$. From (9) it can be noticed that the boost factor attains a maximum before D=1 and then becomes 0. From (6) it can also be seen that the boost ratio is limited for the relation between the inductor's equivalent series resistance (ESR) and the output resistance. The actual boost factor or voltage gain against the duty cycle is analyzed by varying (9).

Fig. 5 depicts the voltage gain versus duty cycle for different values of ESR/Ro for the ideal case i.e., N=1 and it is noticed that the boost factor or voltage gain is quasi-linear when the duty cycle varies in between 0 to 0.5, but beyond that, the boost factor becomes non-linear, therefore the control of boost converter is complicated. Analogously to Fig. 4, Fig. 5 depicts the boost factor for N=3.

From Fig. 5, it can be noticed that the quasi-linear operative region is extended with a high voltage gain or boost factor. Thus, the proposed boost converter can operate in the high boost ratio region, this region is also around D=0.5 which is the better point to operate the multilevel strategy.

4. Proposed Reversing Voltage Inverter Topology

4.1 Cascade based reversing voltage inverter:

Fig. 6 depicts the cascade based RV inverter topology for generation of seven-level output waveform, which consists of DC sources, level generation unit and a 1–ϕ full-bridge inverter for polarity generation [10]. The dc source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two switches. Table.2 gives a comparison of components for producing 1–ϕ seven-level output voltage

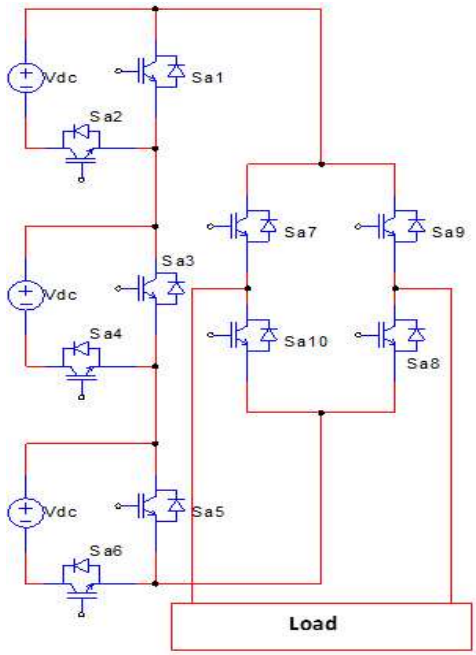


Fig. 6. 1–Φ seven-level Cascade Based RV Inverter

Table 2. Components comparison for producing 1–Φ seven-level output voltage

Components	Proposed	Existing
Switches	10	12
Clamping diodes	0	0
DC sources	3	3
Capacitors	0	0

Table 3. Switching sequence to generate the 1-ϕ seven-level output voltage for cascade based RV inverter

S. No	Cascade Phase leg		Single Phase Full Bridge		Voltage Levels
	On Switches	Off Switches	On Switches	Off Switches	
1	S_{a2}, S_{a4}, S_{a6}	S_{a1}, S_{a3}, S_{a5}	S_{a7}, S_{a8}	S_{a9}, S_{a10}	+3 V_{dc}
2	S_{a1}, S_{a4}, S_{a6}	S_{a2}, S_{a3}, S_{a5}	S_{a7}, S_{a8}	S_{a9}, S_{a10}	+2 V_{dc}
3	S_{a1}, S_{a3}, S_{a6}	S_{a2}, S_{a4}, S_{a5}	S_{a7}, S_{a8}	S_{a9}, S_{a10}	+ V_{dc}
4	S_{a1}, S_{a3}, S_{a5}	S_{a2}, S_{a4}, S_{a6}	S_{a7}, S_{a8}	S_{a9}, S_{a10}	0
5	S_{a1}, S_{a3}, S_{a6}	S_{a2}, S_{a4}, S_{a5}	S_{a9}, S_{a10}	S_{a7}, S_{a8}	- V_{dc}
6	S_{a1}, S_{a4}, S_{a6}	S_{a2}, S_{a3}, S_{a5}	S_{a9}, S_{a10}	S_{a7}, S_{a8}	-2 V_{dc}
7	S_{a2}, S_{a4}, S_{a6}	S_{a1}, S_{a3}, S_{a5}	S_{a9}, S_{a10}	S_{a7}, S_{a8}	-3 V_{dc}

for the proposed and existing cascaded based inverters and it clearly shows substantial component reduction with the proposed structure [12]. For a 1–ϕ seven-level cascade based RV inverter, the switching sequence to generate the required levels are given in Table 3. The operation of the CBRVI is explained in [4].

In this configuration, all the magnitudes of voltage sources are equal ($V_{dc1} = V_{dc2} = V_{dc3}$).

i.e., $V_{dci} = V_{dc}$, where i = 1, 2 and 3

The maximum output phase voltage is the sum of all the dc source voltages, and is given in (10).

$$V_{o,max} = \sum_{i=1}^{S} V_{dci} \tag{10}$$

Therefore, in this method, to generate 7-level output it requires 3 dc sources and 1 H-bridge circuit. However, in practice only one dc voltage source is essential to generate required number of levels with the integration of proposed high-gain DC-DC converter.

Eqs. (10) illustrate the output level of the proposed RV inverter. By using the polarity generation unit the positive and negative levels are synthesized. The synthesized stepped output phase voltage level will be obtained using (11) and (12).

$$V_0,\ max = \sum_{i=1}^{n} +V_i,\ \ If\ S_{a7},\ S_{a8} = 1 \tag{11}$$

$$V_0,\ max = \sum_{i=1}^{n} -V_i,\ \ If\ S_{a9}, S_{a10} = 1 \tag{12}$$

The number of output phase voltage levels can be obtained by the following equation:

$$N_{Levels,\ 1} = (2S + 1)^{H} \tag{13}$$

where 'S' is the number of voltage sources and

'H' is the number of H-bridge circuits

The number of switches for the proposed symmetrical RV inverter can be estimated as follows:

$$N_S = 2\ (S_1+S_2+\ldots\ldots S_n) + 4\ H \tag{14}$$

5. Proposed Modulation Strategies

Modulations techniques are the crucial part for the inverter because it is directly related to the overall efficiency of the entire system [4, 10]. It is used to control the proposed RV MLI output voltage / current and also calculation of two main parameters of MLI such as %THD and form factor (FF). In this paper round modulation control technique has been implemented to trigger the commutating switches of proposed RV MLI and the same is compared with existing switching angle technique i.e., equal-phase (EP) method and half equal – phase method (HEP).

In the EP and HEP switching angle techniques, for an m-level waveform in the period of 0 to 90º, 2(m-1)/2 switching angles need to be determined. Referring to Fig.7, for a seven-level waveform in the period of first quadrant i.e. 0 to 90º, there are three switching angles which need to be determined. We define them as α_1, α_2 and α_3 by the time-sequence. From the Fig. 7, it can be noticed that we need to determine the main switching angles only in the first quadrant. The other switching angles can be derived from the main switching angles. The solution of α_1, α_2 and α_3 must satisfy the following condition.

$$0 \le \alpha_1 \le \alpha_2 \le \alpha_3 \le \frac{\pi}{2} \tag{15}$$

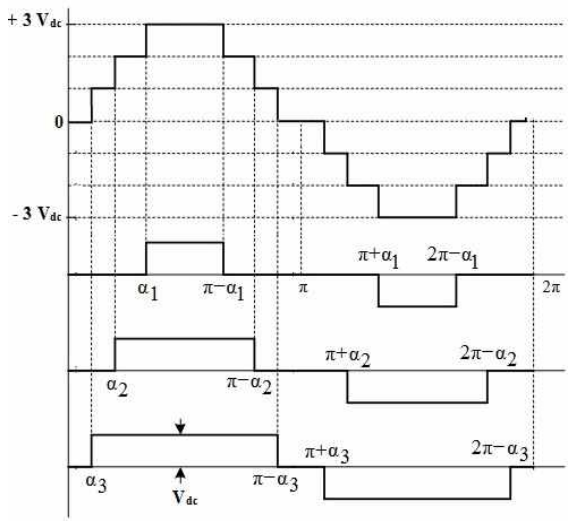


Fig. 7. Generation of phase voltage waveform for seven-level inverter using modulation techniques

5.1 Equal – Phase method (EP):

The EP method is derived from an average distribution of the switching angles in the range 0–180º. In this method, the main switching angles are determined by using (16).

$$\alpha_i = i\left(\frac{180^0}{m}\right) \tag{16}$$

where $i = 1, 2, \ldots \left(\frac{m-1}{2}\right)$, $m = number\ of\ levels$

For seven-level i.e., m=7, we have three main switching angles α_1, α_2 and α_3 and their values are 25.71^0, 51.43^0 and 77.14^0 respectively.

5.2 Half – Equal – Phase method (HEP):

Since the multilevel waveform obtained by the EP switching angle technique looks very narrow and similar to a triangular waveform, another approach called the HEP switching angle technique is used to arrange the switching angles which can acquire a more extensive and better output waveform. The main switching angles are in the range 0 to 90º, which are obtained by using (17).

$$\alpha_i = i\left(\frac{90^0}{\left(\frac{m+1}{2}\right)}\right) \tag{17}$$

where $i = 1, 2, \ldots \left(\frac{m-1}{2}\right)$, $m = number\ of\ levels$

For seven-level i.e., m=7, we have three main switching angles α_1, α_2 and α_3 and their values are 22.5^0, 45^0 and 67.5^0 respectively.

5.3 Round Modulation Control (RMC):

The Round Modulation control (RMC) technique is also known as nearest level control (NLC) technique. RMC generates the nearest staircase voltage which reduces the %THD and improves the waveform quality. In this method, the selection of a nearest voltage level is generated by comparing the desired sinusoidal reference with corresponding inverter output voltage level. The control diagram and waveform synthesis for generating switching signals for the level generation unit by RMC selection control is shown in Fig. 8(a)-(b) and its graphical representation of pulse generation for RMC selection control using the state-to-decoder switching control logic is illustrated in Fig.9 for the proposed RV MLI. The main advantage using RMC is that it can be easily extended to any number of levels [13, 14].

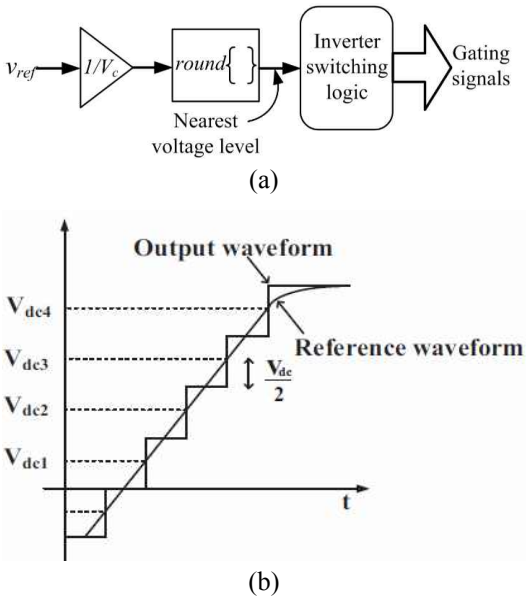


Fig. 8. RMC selection (a) Control diagram and (b) Waveform synthesis

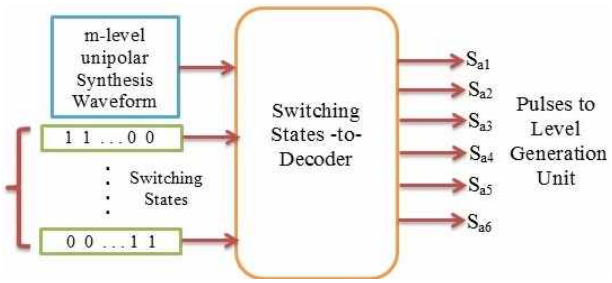


Fig. 9. Graphical representation of pulse generation using switching states for RMC

5.4 Pulse generation for H-Bridge:

Switches of H-Bridge, for positive and negative levels of seven-level output voltage appearance across the load, are triggered by using time based pulse generator. The pulse generator is set with amplitude '1' and operated with fundamental frequency of 50 Hz. The switches S_{a7} and S_{a8} are triggered at the same instant initially with zero degree delay using pulse generator and switches S_{a9} and S_{a10} are triggered with delay of 180 degree with pulse generator. When switches S_{a7} and S_{a8} are turned ON, the positive levels of seven-level output will appear across the load while the operation of switches S_{a9} and S_{a10} ON will give out negative levels of seven-level output to present across the load. When the switches S_{a7} and S_{a8} are turned ON, the switches S_{a9} and S_{a10} are turned OFF and vice-versa.

5.5 Phase voltage THD calculation for the proposed RV inverter

The general THD expression for periodic output phase

voltage waveform for a proposed RV inverter can be written as:

$$THD = \sqrt{\left(\frac{V_{rms}}{V_1}\right)^2 - 1} \tag{18}$$

Where V_1 is the RMS (root mean square) value of the fundamental component and V_{rms} is the RMS value of the output phase voltage. For the proposed seven-level RV MLI V_{rms} and V_1 can be obtained by using (19) and (20).

$$V_{rms} = V_{dc}\sqrt{\left[\frac{2}{\pi}.\begin{pmatrix}(\alpha_2-\alpha_1)+4(\alpha_3-\alpha_2)+\\ 9(\alpha_3-\alpha_2)\end{pmatrix}\right]} \tag{19}$$

$$V_1 = \frac{4V_{dc}}{\pi\sqrt{2}}\left[(Cos\,\alpha_1 + Cos\,\alpha_2 + Cos\,\alpha_3)\right] \tag{20}$$

The output phase voltage THD expression for the proposed seven-level RV inverter can be obtained by substituting (19) and (20) in (18) is given by:

$$THD = \sqrt{\left[\frac{\pi}{4}.\frac{\begin{matrix}(\alpha_2-\alpha_1)+4(\alpha_3-\alpha_2)\\ +9\left(\frac{\pi}{2}-\alpha_3\right)\end{matrix}}{(\cos\alpha_1 + Cos\,\alpha_2 + Cos\,\alpha_3)^2}\right]} - 1 \tag{21}$$

Theoretical values of phase voltage THD for the proposed seven-level inverter using EP, HEP and the proposed RMC modulating techniques with corresponding switching angles are given in Table 4.

Table 4. Switching angles, theoretical phase voltage THD and V_{rms} values for 7-level BDCLCRV (m = 7)

Modulating Technique	Switching angle (degrees)			THD (Theoretical)	V_{rms} (Volts)
	α_1	α_2	α_3		
EP	25.71	51.43	77.14	31.05	165.8
HEP	22.5	45	67.5	25.28	187.9
RMC	9.60	30	56.44	11.97	218.05

6. Simulation And Experimentation of BDCLCRV MLI

6.1 Simulation results:

The simulation of the proposed 1-ϕ seven-level BDCLCRV MLI is carried out and analyzed using MATLAB by considering the input DC source voltage Vdc of 50 V, which is boosted to a total dc link voltage of 250 V, 300 V and 375 V for the duty cycles of 0.4, 0.5 and 0.6 respectively and the voltage across the individual capacitors

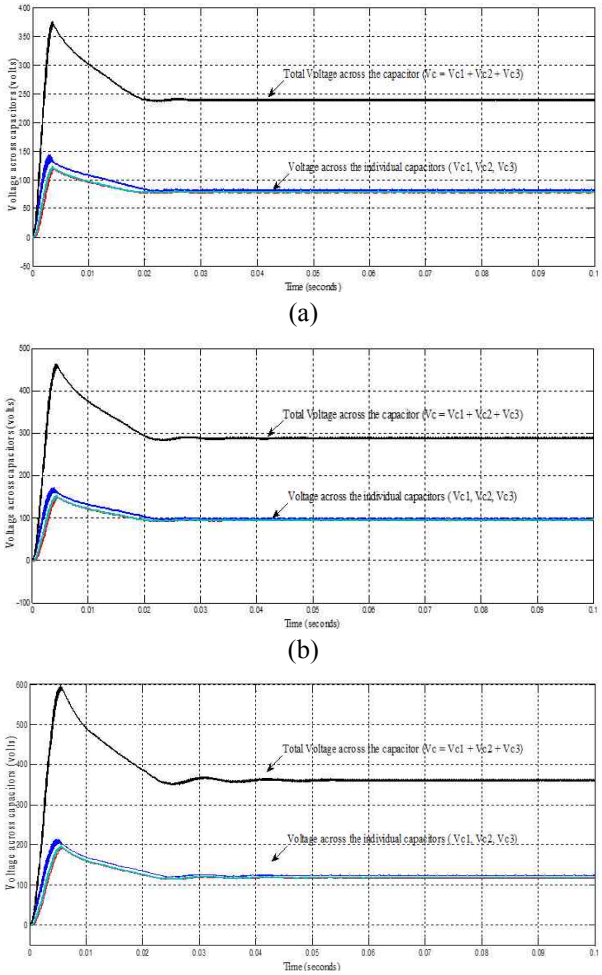


Fig. 10. Boost converter output voltage(V_o) and voltage across the individual capacitors V_{c1}, V_{c2} and V_{c3} for duty cycles (a) D=0.4 (b) D=0.5 and (c) D = 0.6

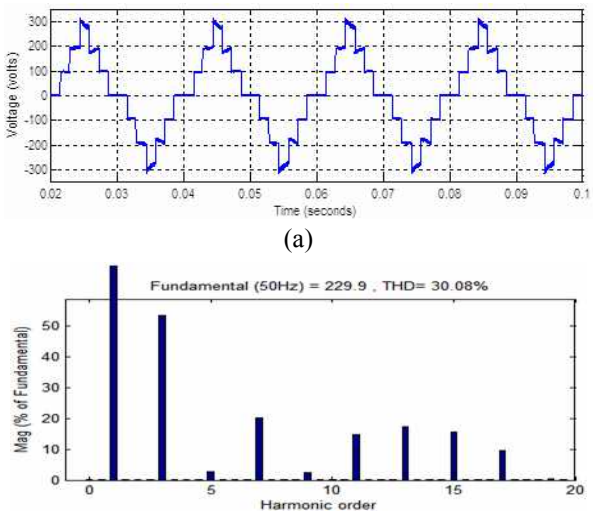
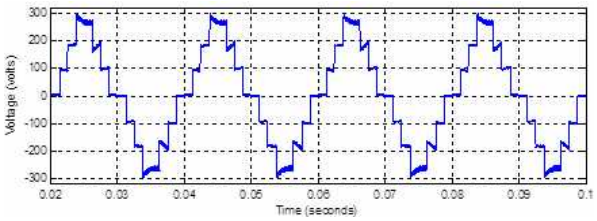
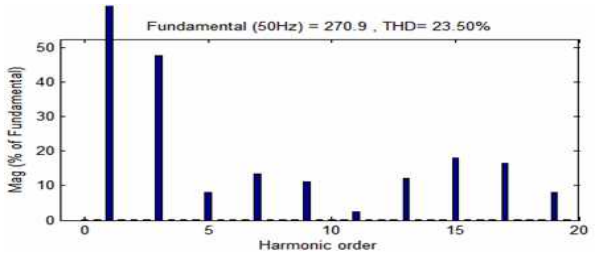


Fig. 11. (a) 1-ϕ seven-level BDCLCRV inverter output voltage using EP method for D=0.5 (b) Corresponding THD analysis

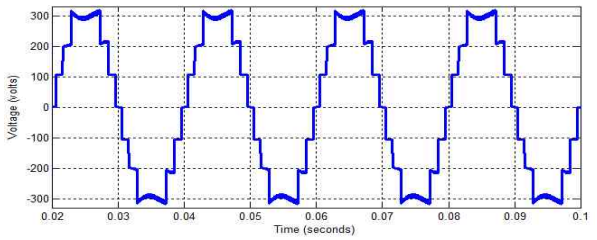


(a)

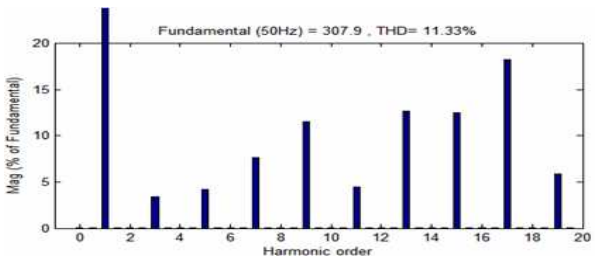


(b)

Fig. 12. (a) 1-ϕ seven-level BDCLCRV inverter output voltage using HEP method for D=0.5 (b) Corresponding THD analysis



(a)



(b)

Fig. 13. (a) 1-ϕ seven-level BDCLCRV inverter output voltage using RMC method for D = 0.5 (b) Corresponding THD analysis

are boosted to 83.33 V, 100 V and 125 V for the duty cycles of 0.4, 0.5 and 0.6 respectively as shown in figs. 10(a), 10(b) and 10(c).

Fig. 11 depicts the output voltage and corresponding THD analysis using EP switching angle technique for the 1-ϕ seven-level BDCLCRV MLI. With respect to Fig. 11, it is found that the crest value of the output voltage is 229.9 V and its RMS value is 162.6 V. From this it can be perceived that the THD on the output voltage is 30.08%.

Fig. 12 depicts the output voltage and corresponding THD analysis using HEP switching angle technique for the 1-ϕ seven-level BDCLCRV MLI. With respect to Fig. 12, it is found that the crest value of the output voltage is 270.9 V and its RMS value is 191.5 V. From this it can be perceived that the THD on the output voltage is 23.50%.

Fig. 13 depicts the output voltage and corresponding THD analysis using RMC modulation technique for the 1-ϕ seven-level BDCLCRV MLI. With respect to Fig. 13, it is found that the crest value of the output voltage is 307.9 V and its RMS value is 217.7 V. From this it can be perceived that the THD on the output voltage is 11.33%.

Fig. 14. Hardware implementation of 1-ϕ seven-level BDCLCRV MLI using FPGA processor

Fig. 15. 1-ϕ seven-level BDCLCRV MLI output voltage for R-Load

Fig. 16. Voltage across the individual capacitor (CH1) and Total voltage across the capacitor (CH2) for D=0.5

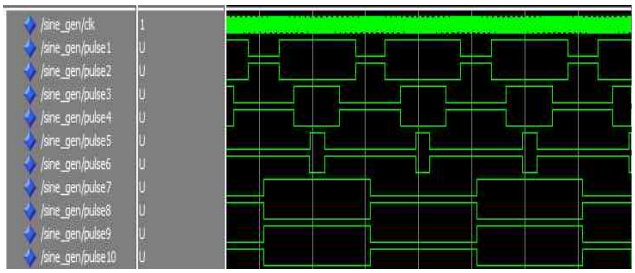


Fig. 17. Pulse generation using EPF method through Xilinx ISE

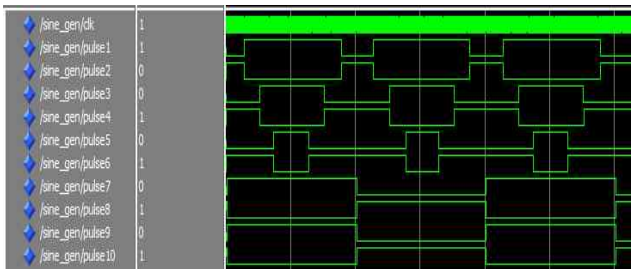


Fig. 18. Pulse generation using HEP method through Xilinx ISE

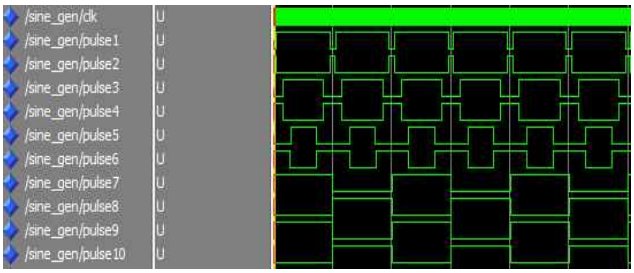


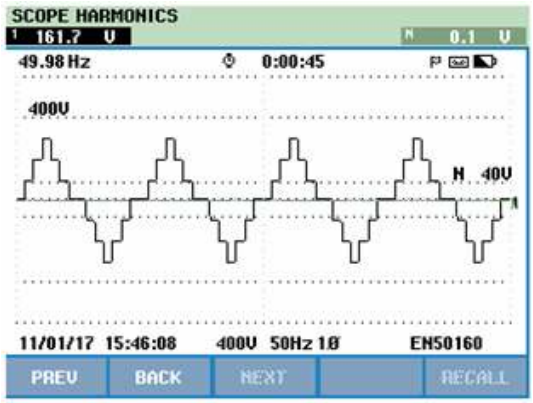
Fig. 19. Pulse generation using RMC method through Xilinx ISE

6.2 Experimental results

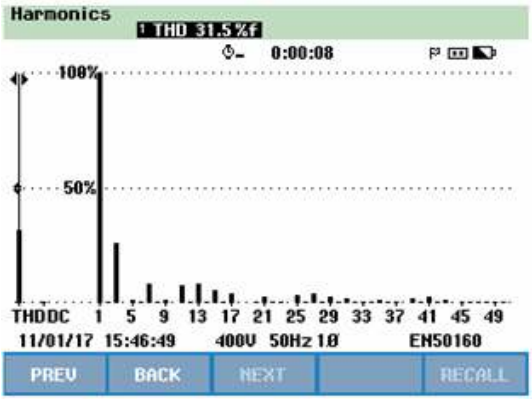
The prototype model of proposed BDCLCRV MLI is implemented using Xilinx Spartan FPGA [16, 17] to validate the simulation results. The hardware realization circuit of the proposed system fed R-load is depicted in Fig. 14. The prototype model consists of three level boost converter, 7-level cascade based RV inverter, resistive load, FPGA controller, PC, buffer circuit, opto isolator and driver circuit. 1-ϕ 7-level BDCLCRV inverter output voltage and voltage across the capacitors for D= 0.5 are shown in Fig. 15 and 16 respectively.

Generation of pulses using EP, HEP and RMC switching angle techniques through Xilinx ISE are depicted in Figs 17, 18 and 19 respectively.

Fig. 20 depicts the experimental output voltage and corresponding THD analysis using EP switching angle technique for the 1-ϕ seven-level BDCLCRV MLI. With respect to Fig. 20, it is found that the RMS value of the output voltage is 161.7 V. It can be perceived that the THD on the output voltage is about 31.5 %.



(a)



(b)

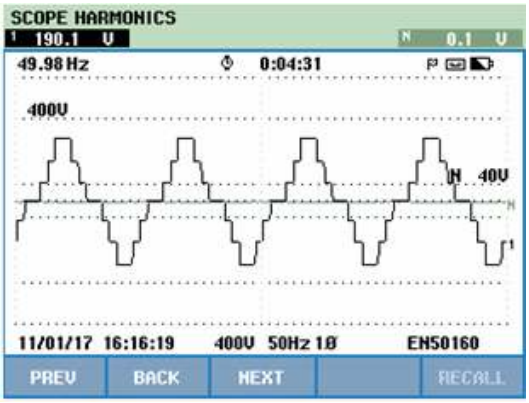
Fig. 20. (a) 1-ϕ seven-level BDCLCRV inverter output voltage using EP method for D=0.5 (b) Corresponding THD analysis

Fig. 21 depicts the experimental output voltage and corresponding harmonic spectrum using HEP switching angle technique for the 1-ϕ seven-level BDCLCRV MLI. With respect to Fig. 21, it is found that the RMS value of the output voltage is 190.1 V. It can be perceived that the THD on the output voltage is about 26.7 %.

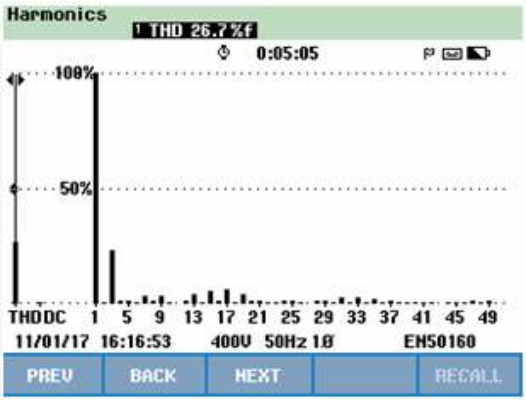
Fig. 22 depicts the experimental output voltage and corresponding harmonic spectrum using RMC switching angle technique for the 1-ϕ seven-level BDCLCRV MLI. With respect to Fig. 22, it is found that the RMS value of the output voltage is 216.0 V. It can be perceived that the THD on the output voltage is about 11.5 %.

6.3 Analysis and comparison of methods

In this study, simulation and experimental output phase voltage waveforms and corresponding THD spectrum of proposed 1-ϕ seven-level BDCLCRV inverter system are depicted in figs. 10 to 22 for the EP, HEP and RMC modulation techniques respectively. Tables 4 and 5 shows the output phase voltage (V_{rms}) and harmonic content of BDCLCRV inverter system for various duty cycles i.e., D = 0.4, 0.5 and 0.6.

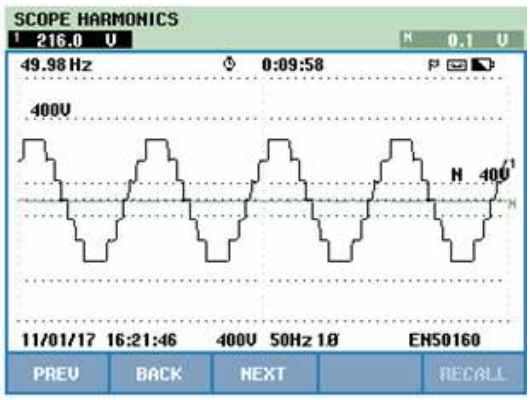


(a)

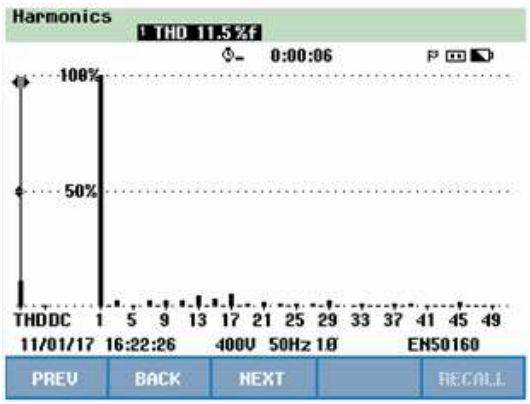


(b)

Fig. 21. (a) 1-ϕ seven-level BDCLCRV inverter output voltage using HEP method for D=0.5 (b) Corresponding THD analysis



(a)



(b)

Fig. 22. (a) Single phase seven level BDCLCRV inverter output voltage using RMC method for D = 0.5 Corresponding harmonic spectrum

Table 5. Simulation comparison of output voltage (V_{rms}) and THD for 7-level (m = 7)

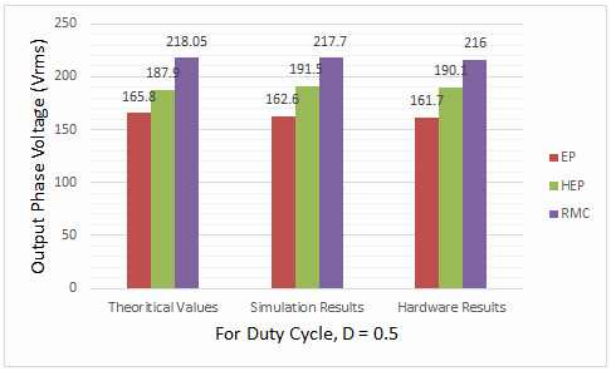
Methods	Fundamental output voltage (Vrms)			THD		
	D = 0.4	D = 0.5	D = 0.6	D = 0.4	D = 0.5	D = 0.6
EP	135.7	162.6	203.6	29.71	30.08	29.90
HEP	159.3	191.5	229.4	23.25	23.50	23.52
RMC	185.1	217.7	271	11.5	11.33	11.4

Table 6. Experimental comparison of output voltage (Vrms) and THD for 7-level (m = 7)

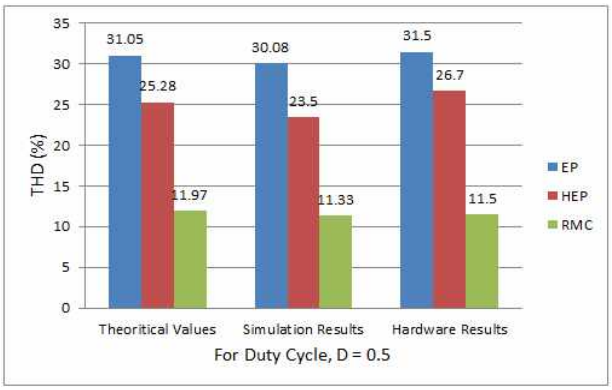
Methods	Fundamental output voltage (Vrms)			THD		
	D = 0.4	D = 0.5	D = 0.6	D = 0.4	D = 0.5	D = 0.6
EP	134.8	161.7	202.2	31.8	31.5	31.5
HEP	157.2	190.1	227	26.6	26.7	26.7
RMC	184.3	216	270.1	11.6	11.5	11.5

From the theoretical, simulation and experimental analysis of output phase voltage and harmonic content, it is inferred that the maximum output phase voltage and lower THD is achieved by using RMC modulation technique. From the theoretical harmonic spectral analysis, it is evaluated that the output phase voltage THD of the proposed 1-ϕ seven-level BDCLCRV inverter system using EP, HEP, and RMC modulation techniques are 31.05 %, 25.28 % and 11.97 % respectively for the duty cycle of 0.5. From the simulation harmonic spectral analysis, it is perceived that the output voltage THD of the proposed 1-ϕ seven-level BDCLCRV inverter system using EP, HEP, and RMC modulation techniques are 30.08%, 23.50% and 11.33% respectively for the duty cycle of 0.5. Harmonic spectrum of the prototype system for the proposed modulation techniques are carried using Fluke 435 power quality analyzer and the results are presented in Figs 18-20 for EP, HEP and RMC modulation techniques respectively. It is perceived that the THD of output voltages are 31.5%, 26.7% and 11.5% respectively for the duty cycle of 0.5. Therefore the theoretical values of phase voltage THD shown in table 4 are validating with the simulation and experimental results with an acceptable error of ± 2%. From the analysis, it is noticed that the magnitude of output voltage varies for different duty cycle values. It can also be noticed that there is no much variation in THD by varying the duty cycles from 0.4 to 0.6.

Comparison of theoretical, simulation and experimental results of output phase voltage and THD are depicted in



(a)



(b)

Fig. 23. Analysis of simulation and hardware results of various switching angle techniques (a) Output phase Voltage (Vrms) (b) % Voltage THD

Fig. 23 for the proposed 1-ϕ seven-level BDCLCRV inverter using EP, HEP and RMC switching angle techniques, it discloses that the simulation and hardware results are closely agreed with that of theoretical calculation. Hence, it is concluded that the proposed BDCLCRV MLI with improved harmonic spectrum using RMC modulation technique is a prominent converter for all industrial applications.

7. Conclusion

In this paper, a structure of 1-ϕ seven-level boost DC-link cascade based reversing voltage multilevel inverter (BDCLCRV MLI) is proposed. Compared with conventional systems, the proposed system is employed with reduced number of switches and it uses only one DC source for the whole converter to synthesize 7-level AC output, which is main constraint of the proposed system and it is inferred that the proposed structure can be an appropriate aspirant for power converters used in UPS and drive applications. The proposed BDCLCRV MLI requires reduced number of components which promises reliability, better performance, efficiency and reduction in cost and size of the inverter.

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