J Electr Eng Technol.2018; 13(4): 1425-1437
http://doi.org/10.5370/JEET.2018.13.4.1425

ISSN(Print) 1975-0102
ISSN(Online) 2093-7423

A Study on the Effective Downscaling Methodology for Design of a Micro Smart Grid Simulator

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Abstract – In this paper, a methodology was proposed to reduce the electrical level and spatial size of the smart grid with distributed generations (DGs) to a scale in which the electrical phenomena and control strategies for disturbances on the smart grid could be safely and freely experimented and observed. Based on the design methodology, a micro smart grid simulator with a substation transformer capacity of 190VA, voltage level of 19V, maximum breaking current of 20A and size of 2×2 m^2 was designed by reducing the substation transformer capacity of 45MVA, voltage level of 23kV and area of 2×2 km^2 of the smart grid to over one thousandth, and also reducing the maximum breaking current of 12kA of the smart grid to 1/600. It was verified that the proposed design methodology and designed micro smart grid simulator were very effective by identifying how all of the fault currents are limited to within the maximum breaking current of 20A, and by confirming that the maximum error between the fault currents obtained from the fault analysis method and the simulation method is within 1.8% through the EMTP-RV simulation results to the micro smart grid simulator model.

Keywords: Smart grid, Micro smart grid simulator, Distribution system, MEMS

1. Introduction

Electrical phenomena and control methods on power grids have been studied for decades. As a result, various fault detection methods, service restoration methods [1-2] and feeder reconfiguration methods [3-4] have been proposed in order to improve the reliability of power supply and the efficiency of power grid operations. In particular, in references [5-7], some new distributed autonomous and adaptive control algorithms have been proposed for a smart grid. However, the proposed methodologies are rarely applied to actual distribution automation systems because of problems with reliability and stability. In addition, a smart grid with distributed generations (DGs) has a mixed structure in which a radial line and a loop line are mixed; this structure raises new problems such as protection coordination due to new electric phenomena arising from the new structure, making the existing problems more difficult to resolve [8-11].

In order for the proposed strategies to be successfully utilized, reliability and stability must be proved through application to a real distribution system. But, this is accompanied by a considerable number of uncertainties and risks because it is not possible to predict when a fault will occur; in the event of a real fault, it can cause severe outages due to inaccurate operation. Therefore, before applying the proposed algorithms to the real system, the basic performance is typically verified using a demonstration test center. However, the configuration and size of a demonstration test center is very limited unlike the real smart grid, construction of which requires considerable economic costs and space cost of several km^2 or more. This makes it difficult to observe the electrical phenomena of other distribution lines (DLs) in large scale systems when a single fault occurs. This difficulty has become a major challenge in recent years. Also, it takes considerable time to prepare and is followed by great danger due to the fault current of maximum 12kA occurring from fault tests carried out at a substation transformer capacity of 45MVA and voltage level of 23kV. This problem, in reality, makes it difficult for engineers and researchers to gain experimental access, and renders it difficult to apply and evaluate the proposed algorithms. In order to overcome this issue, a new paradigm is required such that researchers can freely configure the smart grid in laboratories, observe the electric phenomena of the smart grid and evaluate the experiment results easily and safely. To meet these new requirements, a micro smart grid (SG) simulator that downscales the smart grid electrically and spatially is needed.

The development of the proposed micro SG simulator is planned in three stages, as it involves the design, making and application evaluation of each component as well as the micro SG simulator. The first stage is the design of the micro SG simulator's specifications. The second stage is the prototype making of the micro SG simulator with the bidirectional communication capability.

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Received: October 17, 2017; Accepted: April 3, 2018

In the third stage, application studies including a sophisticated fault detection algorithm and a distributed, autonomous and adaptive control algorithm are performed. This paper presents the design of the micro SG simulator's specifications as the first step. So far, the miniaturization problem of systems and devices has been studied with MEMS technology in several fields [12-14]. However, no systematic method has been proposed to downscale the electrical level and size of the smart grid to the desired electrical level and space size.

Accordingly, in this paper, a methodology is proposed to reduce the electrical level and space size of the smart grid to a predetermined scale to design a micro SG simulator that can safely and freely experiment and observe the electrical phenomena and strategies to control disturbances on a smart grid with DGs. The maximum breaking current (MBC) of the protective devices (PDs) must be reduced as much as possible, since it plays an important role in downscaling the size of the power facilities such as PDs on the smart grid simulator. To solve this problem, in this paper, a fault current limiter (FCL) design method is proposed in which the target impedance value of the FCL is determined by simultaneously and repeatedly considering not only the impedance of FCLs but also the maximum voltage drop of the distribution line for the smart grid with FCL unlike the existing FCL application methods [15-17]. This will help to reduce the MBC values of PDs to the required level. Based on this FCL design methodology, an effective design methodology is developed to miniaturize the electrical level and space size of the smart grid, and then a micro SG simulator is designed using the design methodology. In order to verify the effectiveness of the proposed design methodology, it is checked whether the EMTP-RV fault simulation results for the micro SG simulator model are all within the predefined MBC of the PDs and the artificial fault generator (AFG). Also, the fault currents obtained from the fault analysis method are compared with those obtained from EMTP-RV simulation work for the micro SG simulator model.

2. FCL Design Methodology of Smart Grid

Generally, a smart grid consists of n DLs that receive electricity from one substation transformer, based on the configuration of the actual distribution system, and each DL comprises Q_n line sections, as shown in Fig. 1. Assume that the predetermined DG capacity, P[kVA] is allocated to each DL of the smart grid. At this time, r small capacity DGs with the same capacity (P/r)[kVA] and % impedance can be concentrated at one position or distributed at several positions of the DL. Because the former case has a greater

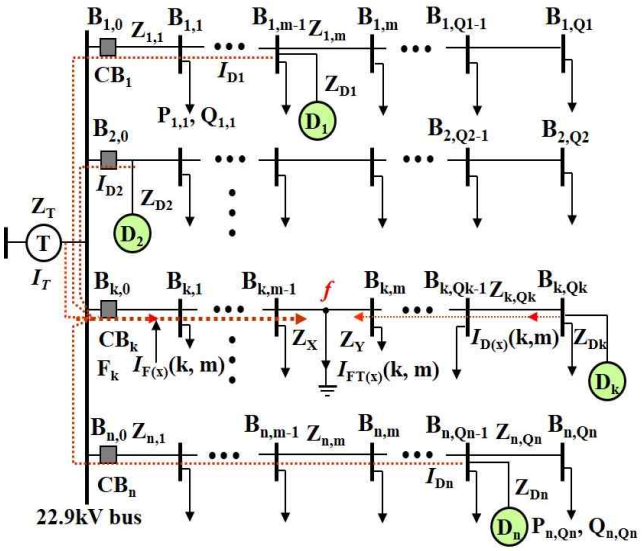

Fig. 1. The smart grid configuration with DGs

effect on the maximum fault current and minimum fault current of the DLs of the smart grid and simplifies the fault current calculation equation, it is appropriate to model the former case to determine the MBC values of PDs on the DLs. Accordingly, one large capacity DG is modeled as being connected to one DL as shown in Fig. 1. In Fig. 1, T and D_i are the substation transformer and the ith DG, respectively, and I_T and I_{Di} are the secondary currents of T and the current of D_i. Further, Z_T and Z_{Di} are % impedances of T and D_i. F_i is the ith feeder, and CB_i is the circuit breaker of F_i. $B_{i,j}$ is the jth line bus of F_i and $Z_{i,j}$ is the % impedance of the jth line section of F_i. $P_{i,j}$ and $Q_{i,j}$ are the active power and reactive power of the jth line section of F_i, respectively. If an arbitrary fault occurs at point *f* of the mth section of the kth line (F_k) then the configuration of the fault impedance is determined by the location of the DG, as shown by the dashed line in Fig. 1.

The dashed line represents the current that flows from the substation transformer and DGs to the fault point *f*. In particular, $I_{F(x)}(k, m)$ and $I_{D(x)}(k, m)$ are the fault currents flowing from CB_k and D_k to *f*, respectively, and $I_{FT(x)}(k, m)$ is the total fault current flowing into *f*, which is equal to the sum of $I_{F(x)}(k, m)$ and $I_{D(x)}(k, m)$. Here, the subscript x is expressed as s for a three phase short circuit fault and g for a single phase ground fault. The paths from DGs connected to lines except F_k, and substation transformer T to the 23kV bus, consist of parallel circuits. On the other hand, the fault circuit on the path from the 23kV bus to the faulty feeder depends on the location of the DG. In particular, the fault impedance is composed differently depending on whether DG is on an upstream position or on downstream position from *f*. Finally it can be represented as a variable resistor that has different impedance values according to the location of DG. In this paper, FCLs are introduced to reduce the fault current in the smart grid with DGs as

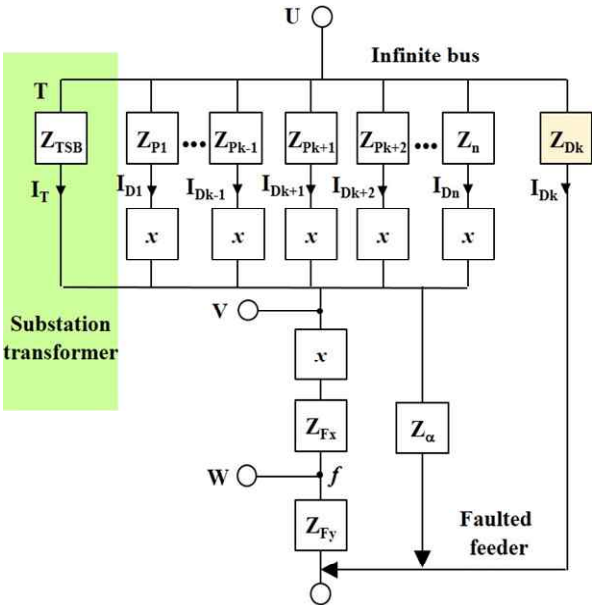

Fig. 2. Total impedance map of the smart grid

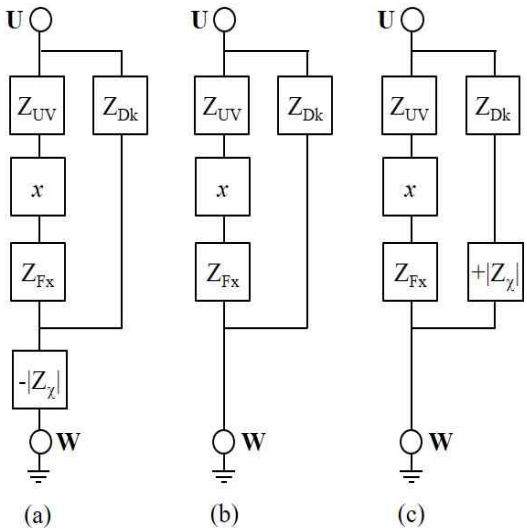

Fig. 3. Equivalent circuit for the total fault impedance circuit of the smart grid

shown in Fig. 1. FCLs play a major role in reducing the maximum fault current and the MBC of the PDs on a micro SG simulator within a target level. When applying the concept of infinite bus method in [18-19, 24] to a smart grid with n DLs, n FCLs and n DGs, the total impedance map of the smart grid can be represented as shown in Fig. 2.

In Fig. 2, Z_{TSB} is the path % impedance from power grid to secondary bus of T, Z_{Pi} is the path % impedance from D_i to secondary bus of T, and *f* is the fault location on the faulty feeder. Z_{Fx} and Z_{Fy} are upstream % line impedance and downstream % line impedance from *f* on the faulty feeder, respectively. Z_α is the % line impedance from the 23 kV bus to the position of D_k on the faulty line F_k, and *x* is % impedance of FCL.

2.1 Computation of fault currents

The fault currents for a smart grid can be obtained by applying a symmetric coordinate method [18] to the total fault impedance circuit of Fig. 2. In Fig. 1, D_k is on the downstream line of the fault point *f*, but may be on the fault point or on the upstream line of fault point. Fig. 3 shows the equivalent circuit for the fault impedance circuit of a smart grid. In Fig. 3, (a) shows the equivalent circuit when DG is on the upstream line of the fault point *f*, (b) shows the equivalent circuit when DG is on the fault point *f,* and (c) shows the equivalent circuit when DG is on the downstream line of the fault point *f*, respectively. Here, Z_χ is Z_α minus Z_{Fx}.

Initially, the fault impedance Z_{UV} [%] obtained by the paths from DGs of adjacent feeders and the substation transformer T to the bus bar can be represented as Eq. (1).

$$Z_{UV} = \frac{1}{\sum_{i=1, i\neq k}^{n} \frac{1}{Z_{Pi}+x} + \frac{1}{Z_{TSB}}} \tag{1}$$

The total impedance of the fault impedance circuit, Z_{UW} [%] can be represented as Eq. (2). In Eq. (2), β has a different value depending on whether the fault location *f* is an upstream location or a downstream location with respect to the DG on the DL experiencing the fault. If Z_α is less than or equal to $Z_{Fx,}$ then β is 0; otherwise β is 1.

$$Z_{UW} = \frac{(Z_{UV}+x+Z_\alpha-\beta Z_\chi)(Z_{Dk}+\beta Z_\chi)}{Z_{UV}+x+Z_\alpha+Z_{Dk}} + (\beta-1)Z_\chi \tag{2}$$

I_{UV} can be represented as Eq. (3). In Eq. (3), I_{UV} is the fault current flowing from CB_k to fault location *f*.

$$I_{UV} = \frac{(Z_{Dk}+\beta\gamma)}{Z_{UV}+x+Z_\alpha+Z_{Dk}} \times I_{UW} \tag{3}$$

I_{Dk} can be represented as Eq. (4). In Eq. (4), I_{Dk} is the fault current flowing from D_k to fault location *f*.

$$I_{Dk} = \frac{Z_{UV}+x+Z_\alpha-\beta\gamma}{Z_{UV}+x+Z_\alpha+Z_{Dk}} \times I_{UW} \tag{4}$$

And, I_{UW} is the total fault current I_{FTk} flowing into the fault location *f* which is the sum of I_{UV} and I_{Dk}. I_{Di} (except for I_{Dk}) and I_T can be computed through Eq. (5) and (6), respectively.

$$I_{Di(i\neq k)} = [Z_{UV}/(Z_{Pi}+x)] \times I_{UV} \tag{5}$$

$$I_T = (Z_{UV}/Z_{TSB}) \times I_{UV} \tag{6}$$

In the case of a three phase short circuit fault, Z_{Pi}, Z_{TSB}, Z_{UV}, Z_{α}, Z_{Dk}, Z_{UW}, I_{UW}, I_{UV} and I_{Dk} of Eq. (1)-(6) should be represented as Z_{Pi1}, Z_{TSB1}, Z_{UV1}, $Z_{\alpha 1}$, Z_{Dk1}, Z_{UW1}, I_{UW1}, I_{UV1} and $I_{Dk1,}$ which are the % positive sequence impedances and the % positive sequence currents respectively. At this time, I_{UV1}, I_{Dk1} and I_{UW1} are $I_{F(s)}$(k, m) and $I_{D(s)}$(k, m) $I_{FT(s)}$(k, m), respectively. In Eq. (5)-(6), $I_{Di(i\neq k)}$ and I_T should be represented as $I_{Di1(i\neq k)}$ and $I_{T1,}$ which are the corresponding positive sequence currents. Further, I_{UW1} becomes the three phase short fault current $I_{s,}$ which is computed using Eq. (7) based on the symmetrical coordinate method.

$$I_s = \frac{100}{Z_{UW1}} \times \frac{P}{\sqrt{3}V} \tag{7}$$

In Eq. (7), V is base voltage [kV] and P is base capacity [MVA]. The currents in the substation transformer T and each D_i in case of the the three phase short circuit fault are I_{T1}, I_{Dk1} and $I_{Di1(i\neq k).}$

In the case of a single phase ground fault, Z_{Pi}, Z_{TSB}, Z_{UV}, Z_{α}, Z_{Dk}, Z_{UW}, I_{UW}, I_{UV} and I_{Dk} of Eq. (1) - (6) should be represented as Z_{Pi0}, Z_{TSB0}, Z_{UV0}, $Z_{\alpha 0}$, Z_{Dk0}, Z_{UW0}, I_{UW0}, I_{UV0} and I_{Dk0} which are the corresponding % zero sequence impedances and zero sequence currents, respectively. If the % neutral ground resistance Z_{NGR} exists, Z_{TSB0} is $Z_{TSB} + 3Z_{NGR}$. In Eq. (5)-(6), $I_{Di\ (i\neq k)}$ and I_T should be represented as $I_{Di0\ (i\neq k)}$ and $I_{T0,}$ which are the corresponding zero sequence currents. I_{UW0} becomes the single phase ground fault current $I_{g,}$ which is computed using Eq. (8) based on the symmetrical coordinate method.

$$I_g = \frac{3\times 100}{Z_{UW0} + Z_{UW1} + Z_{UW2}} \frac{P}{\sqrt{3}V} \tag{8}$$

In Eq. (8), Z_{UW2} represents the % negative sequence impedance of Z_{UW}. The currents in the substation transformer T and each D_i in the single phase ground fault are obtained by Eq. (9), (10) and (11). Here, I_{UVg}, I_{Dkg} and I_{UW0} become $I_{F(g)}$(k, m), $I_{D(g)}$(k, m) and $I_{FT(g)}$(k, m) for the single phase ground fault, respectively.

$$I_{UVg} = I_{UV0} + 2\times I_{UV1} \tag{9}$$

$$I_{Tg} = I_{T0} + 2\times I_{T1} \tag{10}$$

$$I_{Dig} = I_{Di0} + 2\times I_{Di1} \tag{11}$$

2.2 Determination of FCL

When a three phase short fault occurs at point *f* in the jth line section of the ith distribution line, the fault currents $I_{F(s)}$(i, j), $I_{D(s)}$(i, i) and $I_{FT(s)}$(i, j) are obtained from Eq. (3), (4), and (7), respectively. On the other hand, when a single phase ground fault occurs at point *f* in the jth line section of the ith distribution line, the fault currents $I_{F(g)}$(i, j), $I_{D(g)}$(i, j) and $I_{FT(g)}$(i, j) are obtained from Eq. (9), (11) and (8), respectively. Therefore, FCL design is a matter of determining *x* such that the maximum value × λ of fault currents $I_{F(s)}$(i, j) and $I_{F(g)}$(i, j) obtained from fault cases of all line buses $B_{i,j}$ is less than I_{Pmbc} and the minimum value of fault currents $I_{F(s)}$(i, j) and $I_{F(g)}$(i, j) obtained from fault cases of all line buses $B_{i,j}$ are equal to or greater than $\delta \times I_{Pmoc}$ for $i\in U$, $j\in V_i$. Here, I_{Pmbc} is the predefined maximum breaking current (MBC) of PDs of DLs, I_{Pmoc} is the predefined minimum operating current (MOC) of PDs of DLs, U is the set of all DLs of smart grid and V_i is the set of all line buses of the ith DL. V_i is defined as a set of all line buses because the fault point must be a line bus instead of a line section in order to obtain more accurate the maximum fault current value and minimum fault current value. Also, the maximum value I_{dmax}, and minimum value I_{dmin} of fault currents $I_{D(s)}$(i, j) and $I_{D(g)}$(i, j) obtained from fault cases of all line buses $B_{i,j}$ for $i\in U$, $j\in V_i$ are utilized to determine I_{Dmbc} and I_{Dmoc} of DGs in Fig. 5. Here, I_{Dmbc} is the predefined maximum breaking current (MBC) of PDs of DGs, I_{Dmoc} is the predefined minimum operating current (MOC) of PDs of DGs, λ is the safety factor that is considered to ensure so that PDs have sufficient fault current blocking capability, and δ is safety factor that is introduced in order for the PD to work clearly.

Unfortunately, since Z_{UV} is the nth order equation for *x* as shown in Eq. (1), it is impossible to obtain an equation for directly determining *x* from Eq. (3). Accordingly, it is necessary to determine *x* according to the following design procedure. The overall design procedure of FCL is shown in Fig. 4.

Step 1 Determine the I_{Pmbc} and I_{Pmoc} of PD for the DLs on the smart grid. Where, I_{Pmoc} is τ times the rated current of the distribution line, generally τ is 2.

Step 2 Set the initial value of *x*, which is the impedance value of FCL, to 0, the value of Δ to 0.1, and the value of DM to 0. Here DM stands for design mode. If DM is 0, it is a FCL design mode based on the change of *x*, whereas if DM is 1, it is a DL design mode that solves the problem based on the change of V_{MVD} when problem-solving is difficult with *x* only. Here, V_{MVD} is the maximum allowable voltage drop which is the management goal for voltage drop of DL in an electric power company.

Step 3 Compute $\{I_{FT(s)}(i, j)\}$ by applying Eq. (7) and then $\{I_{F(s)}(i, j)\}$ and $\{I_{D(s)}(i, j)\}$ by applying Eq. (3) and Eq. (4) to fault cases of $B_{i,j}$ for $i\in U$, $j\in V_i$. Go to step 4.

Step 4 Determine $v_0=\max\{I_{FT(s)}(i, j)\}$, $v_1=\max\{I_{F(s)}(i, j)\}$, $v_2=\min\{I_{F(s)}(i, j)\}$, $v_3=\max\{I_{D(s)}(i, j)\}$ and $v_4=\min\{I_{D(s)}(i, j)\}$. Go to Step 5.

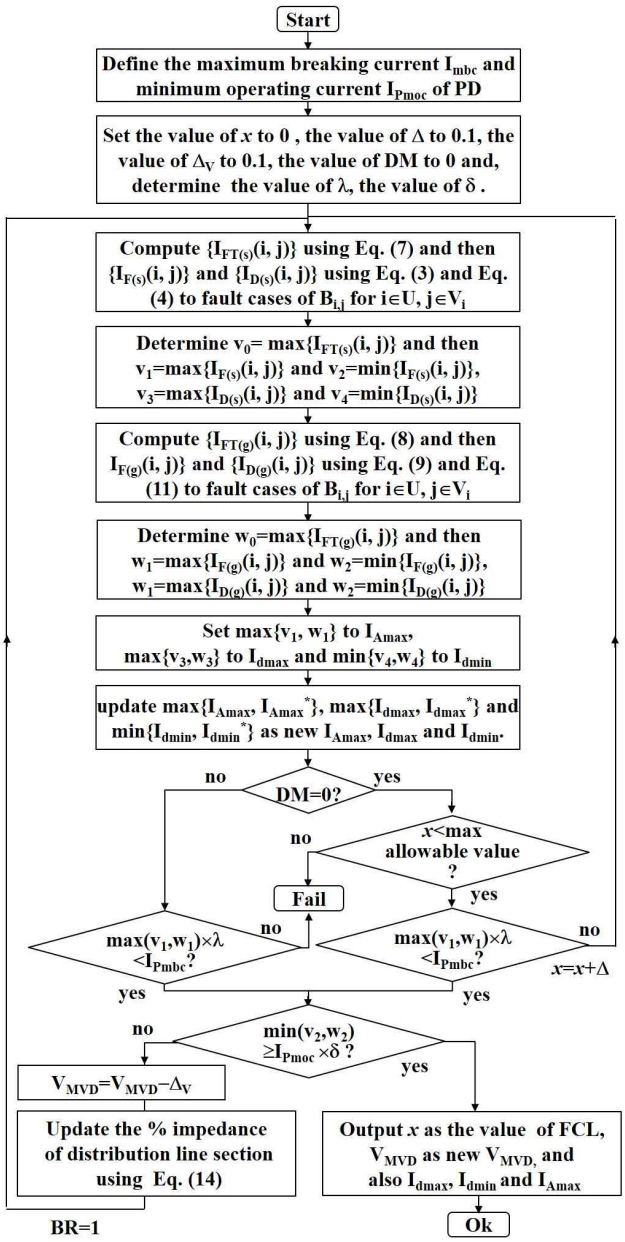

Fig. 4. The design procedure of FCL

Step 5 Compute $\{I_{FT(g)}(i, j)\}$ by applying Eq. (8) and then $\{I_{F(g)}(i, j)\}$ and $\{I_{D(g)}(i, j)\}$ by applying Eq. (9) and Eq. (11) to the fault cases of line bus $B_{i,j}$ for $i \in U$, $j \in V_i$. And then go to step 6

Step 6 Determine $w_0 = \max\{I_{FT(g)}(i, j)\}$, $w_1 = \max\{I_{F(g)}(i, j)\}$, $w_2 = \min\{I_{F(g)}(i, j)\}$, $w_3 = \max\{I_{D(g)}(i, j)\}$, $w_4 = \min\{I_{D(g)}(i, j)\}$. Go to step 7.

Step 7 Set max $\{v_0, w_0\}$ to I_{Amax}, max $\{v_3, w_3\}$ to I_{dmax} and min $\{v_4, w_4\}$ to I_{dmin}. Here, I_{Amax} is introduced in Fig. 5 to determine I_{AFG} which is the maximum allowable current (MAC) of the AFG.

Step 8 Update max $\{I_{Amax}, I_{Amax}^*\}$, max $\{I_{dmax}, I_{dmax}^*\}$ and min $\{I_{dmin}, I_{dmin}^*\}$ as new I_{Amax}, I_{dmax} and I_{dmin}, and then go to step 9. Here, * means the previous values.

Step 9 If DM is 0, go to step 10 to solve the problem in FCL design mode, otherwise go to step 12 to solve the problem in DL design mode.

Step 10 If x is less than the maximum allowable value 2.0, go to step 11, otherwise output Fail.

Step 11 If max $\{v_1, w_1\}\times\lambda$ is less than $I_{Pmbc,}$ then go to step 13, otherwise $x = x+\Delta$ and go to step 3.

Step 12 If max $\{v_1, w_1\}\times\lambda$ is less than $I_{Pmbc,}$ then go to step 13, otherwise output Fail.

Step 13 If min $\{v_2, w_2\}$ is greater than $I_{Pmoc}\times\delta$ then go to Step 14, otherwise set V_{MVD} to V_{MVD}-Δ_V, update the % impedance of distribution line sections to the newly calculated impedance value using Eq. (14), set BR to 1, and go to step 3. Here, the value of Δ_V is 0.1.

Step 14 Determine x as the design value of FCL, V_{MVD} as new V_{MVD}, and output I_{dmax}, I_{dmin}, and I_{Amax} to determine I_{Dmbc} and I_{Dmoc} of DGs and I_{AFG} of AFG in Fig. 5, and then output Ok.

3. Design of Micro Smart Grid Simulator

Here, a methodology for designing a micro SG simulator is developed based on the configuration of the real smart grid, the empirical knowledge obtained from the design experts of the power distribution system and the operating experts of automated distribution system, and [20].

3.1 Modelling of the micro ST

Generally, the substation transformer (ST) is a three phase three-winding transformer, and uses the wiring method of Y_g- Y_g-Δ or Y-Y_g-Δ depending on whether the primary side is grounded or not. However, the three-winding transformer is costly, and difficult to construct and downsize because of its complicated structure. Therefore, through the fault impedance analysis, an easy-to-build two-winding transformer is adopted for this study. Table 1 shows the equivalent impedance circuit of the power grid viewed from secondary bus of the substation transformer by wiring method. In Table 1, Z_{G1} and Z_{G0} are the % positive sequence impedance and the % zero sequence impedance of the source power grid, respectively. Z_P, Z_S and Z_T represent the % impedance of the primary winding, the % impedances of the secondary winding and the tertiary winding respectively. Also, Z_{G0P} is the sum of Z_{G0} and Z_P, and $Z_{G0P}//Z_T$ is the parallel impedance of Z_{G0P} and Z_T.

Table 1. Equivalent impedance circuit by wiring method

Sym. circuit	Primary ground	Equivalent impedance circuit	
		Y_g-Y_g-Δ	Δ-Y_g
Positive sequence	yes/no	Z_{G1} Z_P Z_S	Z_{G1} Z_P Z_S
Zero sequence	No	Z_T Z_S $3Z_{NGR}$	Z_T Z_S $3Z_{NGR}$
	Yes	Z_{G0P}, Z_T, Z_S, $3Z_{NGR}$	Z_T, Z_S, $3Z_{NGR}$, $3Z_{COM}$

In Table 1, although the zero sequence component of the equivalent impedance circuit of Y_g-Y_g-Δ wiring is different from that of Δ-Y_g wiring, it can be compensated for by introducing Z_{COM} in parallel to Z_{NGR}. However, Z_{COM} is not considered in this paper. It is because it offers more severe test conditions by reducing the ground fault current.

Accordingly, Δ-Y_g wiring is adopted which is the three phase, two-winding transformer. The secondary rated voltage V_2 of the micro substation transformer is determined to be 19V, based on the iterative design results of micro SG simulator shown in Fig. 5. This is intended to achieve the target MBC in the range of 20 to 15V. In general, a substation transformer supplies electric power to six DLs. Based on this configuration of the smart grid, six micro DLs supplied by one micro substation transformer are designed on the micro SG simulator.

3.2 Modelling of the micro DL

The micro DL adopted an electric supply method of the 3-phase 4-wire type, which is the standard electric supply method of overhead lines on a smart grid. In particular, it is designed such that all micro DLs are made up of 5 line sections and 3 tie connections equally, based on the distribution system design standard. First of all, the rated current I_{FR} of the micro DL is designed to be safe enough to handle. Here, the I_{FR} is designed to be 0.76A. The maximum allowable current I_{EC} of micro DL can be set as 1A which is 1.4 times the rated current I_{FR} of the micro DL. If the loads of all line sections of all micro DLs are designed equally, based on V_2 and I_{FR}, each section load P_L can be set at 4.75W+j1.56VAR by Eq. (12) with the load factor 0. 95, which is the management goal of power factor in an electric power company.

$$P_L = \frac{1}{Q}\sqrt{3}V_2 I_{FR} \tag{12}$$

In Eq. (12), Q is the number of line sections. The

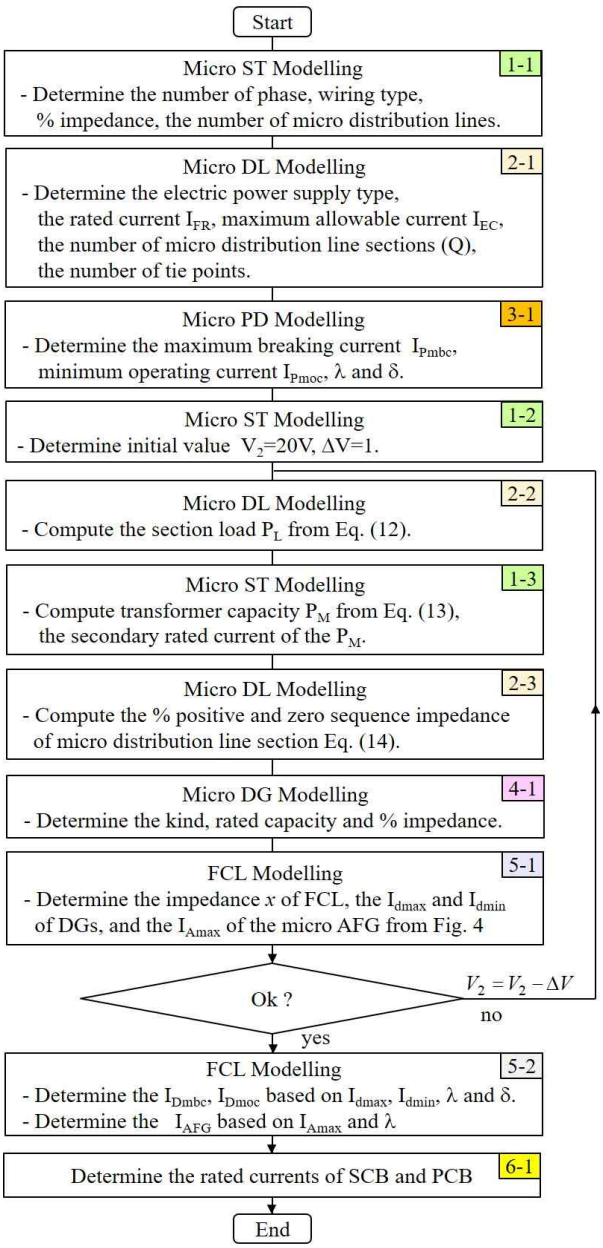

Fig. 5. Design procedure of the micro smart grid simulator

capacity P_M of the micro substation transformer is designed as 190VA by Eq. (13). In Eq. (13), n is the number of micro DLs and α is the safety factor of micro substation transformer. The α value of the smart grid is about 1.3, but the α value of the micro SG simulator is defined as 1.25. This is because the maximum load of a micro substation transformer is constant unlike that of the smart grid.

$$P_M = n\sqrt{3}V_2 I_{FR} \times \alpha \tag{13}$$

If the positive sequence impedance Z_{LS1} of all line sections are designed to be the same, it can be computed by Eq. (14).

$$Z_{LS1} = V_{MVD} \Big/ \left(\frac{P_L}{\sqrt{3} V_2} \sum_{k=1}^{Q} Q - k + 1 \right) \quad (14)$$

In Eq. (14), because V_{MVD} is designed as 3%, the % impedance of Z_{LS1} based on 190VA is determined as 5.06 + j10.11. The zero sequence impedance values Z_{LS0} of all line sections are designed to be the same as Z_{LS1}.

3.3 Modelling of the micro DG

Based on [8, 21-25], the fault current of PV inverter system connected to the power system is limited to 1.5 times the rated current of the PV system. The PV inverter system will be disconnected from the grid within half a cycle to protect the inverter components if a fault causes flow of more than 1.5 times the rated current. On the other hand, in the case of a wind turbine generator with a synchronous generator, a fault current of 5 to 8 times the rated current flows due to the effect of transient reactance. Therefore, the wind turbine system is selected as a micro DG since the wind turbine system has a greater influence on determining the MBC and total fault current of the PD. The capacity of the micro DG is determined to be 7.5VA, which is 30% of the micro DL capacity 0.76A as a power company aims to reach 30% of the line capacity in order to increase the efficiency of power utilization. Because the purpose of this paper is to determine the MBC of DGs rather than to observe the transient characteristics, the wind turbine generators are modeled with the % impedance. In particular, in order to obtain the maximum fault current at 8 times the rated current as shown in [21], the 7.5VA based % impedance Z_1 (Z_0) is determined as j12.5 by 100/8. Here, $Z_1$and Z_0 are the % positive sequence impedance and % zero sequence impedance, respectively.

3.4 Modelling of the micro PD

PDs in the smart grid include CBs, reclosers, a section switch and a tie switch. In designing and making these PDs, the determination of the MBC is very important in determining the electrical level and size of the micro SG simulator. The I_{Pmbc} of PDs on the micro SG simulator is designed to be 20A to reduce the size of the PDs to 13x13cm^2 by applying the relay as a switching device. This way, the system can be tested safely and freely in the laboratory, and it also reduces the space size of the smart grid to 4x4m^2. Further, I_{Pmoc} of the micro PDs on the micro DL is designed as 1.5A which is 2 times the rated current I_{FR}, 1.5 times the maximum allowable current $I_{EC,}$ and sufficiently smaller than the MBC target value. Accordingly, the micro PDs should be able to operate at 1.5A and break the maximum current 20A when an artificial fault is generated on the micro SG simulator. Furthermore, the values of λ and δ are both set to 1.5 to ensure that PDs have sufficient fault current breaking capability and at the same time allow those PDs to work efficiently. Fig. 5 shows the overall design procedure of the micro SG simulator.

3.5 Determination of FCL

The maximum fault current of the micro DLs on a micro SG simulator is hundreds of A. The FCLs are designed to make this fault current smaller than I_{Pmax} and greater than δ times I_{Popc} of the PDs mentioned above. The design procedure shown in Fig. 5 is implemented as an Excel program. Further, using the Excel program, the FCLs are designed as 0. 9Ω, and the I_{Dmbc} and I_{Dmoc} of DGs are designed as 5A and 0.5A, respectively. Also, the maximum allowed current I_{AFG} of AFG is designed as 30A. Here, I_{Dmbc}, I_{Dmoc} and I_{AFG} are designed with the same

Table 2. Specifications of the micro smart grid simulator

Power facility		Smart grid	Micro smart grid simulator	
Ob.	Attributes			
ST	Num. of phases	3 phase	3 phase	20x20 cm^2
	Wiring method	Y-Y_g-Δ Y_g-Y_g-Δ	Δ-Y_g	
	Capacity	45 MVA	190VA	
	% impedance	j15.9	j2	
	Ω based Z_{NGR}	j0.6Ω	j0.05Ω	
	Rated voltage	22.9 kV	19V	
	Rated current	1,512 A	5.77A	
	Num. of feeders	6	6	
DL	Supply type	3p 4w	3p 4w	
	Rated current	252A	0.76A	
	Max current	352.8A	1A	
	Num.of sections	5	5	
	Num. of ties	≥3	3~6	
	Section load	0.316MVA	5VA	13x5cm^2
	Section% imp.	6.95+j14.92	5.06+j10.11	13x5cm^2
	V_{MVD} (%)	≤ 5%	3 %	
	Power factor	0.95	0.95	
DG	Rated capacity	1MVA	7.5VA	13x20 cm^2
	Rated current	75.6A	19V 0.228A	
	% impedance	-	j12.5	
	MBC (I_{Dmbc})		19V 5A	
	MOC (I_{Dmoc})		19V 0.5A	
PD	MBC (I_{Pmbc})	2,521A	19V 20A	13x13 cm^2
	MOC (I_{Pmoc})	500A	19V 1.5A	
FCL	Ω based *x*	-	j0.9Ω	13x5cm^2
AFG	MAC (I_{AFG})	-	19V 30A	8x8cm^2
SCB	MOC (I_{SCB})	-	19V 30A	8x8cm^2
PCB	MOC (I_{PCB})	-	380V 10A	8x8cm^2
	Space size	2x2km^2		2x2m^2

λ and δ values as in the PD design. The AFG is introduced to generate fault on the micro SG simulator. Table 2 shows the specifications of the micro SG simulator. The facilities attributes of the smart grid are obtained by [11].

3.6 Modeling of the power source

The fault current of the micro SG simulator does not affect the smart grid at all because it is very small compared to the load current of smart grid. On the other hand, the load current of smart grid on the power supply circuit will have an impact on the fault current of a micro SG simulator without an automatic voltage regulator. For a micro SG simulator without the automatic voltage regulator, as the line load of the smart grid is heavier and the installation location of the micro SG simulator is closer to the end of the line of the smart grid, the voltage drop of the smart grid will have more impact on the fault current of the micro SG simulator. Therefore, an automatic voltage regulator (AVR) is designed in front of the power source of the micro SG so that the fault test can be independently performed without being influenced by the voltage drop of the smart grid.

3.7 Determination of SCB and PCB

In order to protect the micro SG simulator and engineer when an artificial fault is generated by AFG, a secondary circuit breaker (SCB) with I_{SCB} of 30A is installed on the secondary side of the micro substation transformer. Here, I_{SCB} is a minimum operating current (MOC) of SCB.

In a normal state, when an artificial fault is generated on the micro SG simulator, SCB with MOC of 30A is not activated since the fault current is limited within the I_{Pmax} 20A of micro PD. On the other hand, because micro PDs are operated to protect the micro SG simulator, it is possible to observe the fault phenomenon and test the control strategy using these micro PDs. However, if the fault current exceeds 20A due to a physical fault on the micro SG simulator, micro PDs may be damaged or the operator injured. If the fault cannot be completely eliminated due to this problem, it can lead to a very dangerous situation, in which the in-built SCB protects the micro SG simulator and the operator. Also, a PCB with I_{PCB} of 10A is designed on the primary side of the micro substation transformer to protect the circuit when the SCB does not work or when a fault occurs in a micro substation transformer. Here, IPCB is a minimum operating current (MOC) of PCB. Fig. 6 shows the overall configuration of the micro SG simulator designed by specifications shown in Table 2.

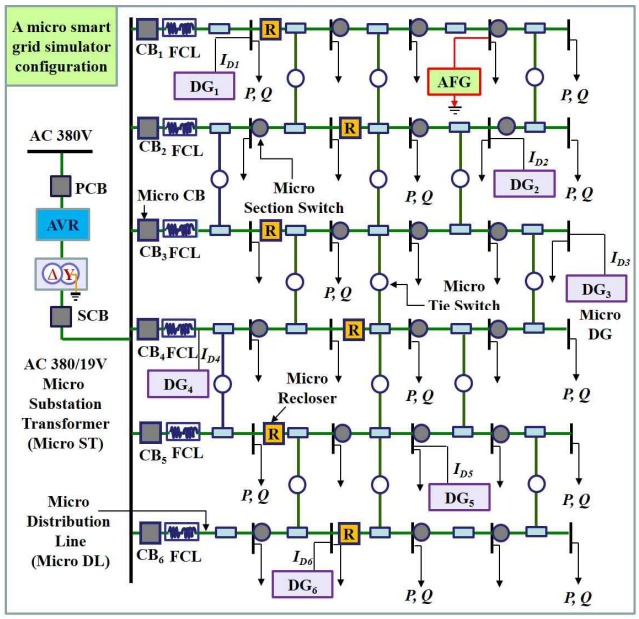

Fig. 6. Configuration of the micro smart grid simulator

4. Validation of the Design Methodology

The validity of the proposed design methodology can be verified by confirming the effectiveness of the designed micro SG simulator model using it. For this purpose, the micro SG simulator model based on Table 2 and Fig. 2 is developed as an EMTP model [26], and the fault currents from the EMTP-RV simulation work are compared with the fault currents obtained from the design methodology.

4.1 Effectiveness of the micro SG simulator model

The effectiveness of the micro SG simulator can be verified by generating faults in all buses on the micro SG simulator model and then checking whether the fault currents met the design conditions of the micro PD, the design conditions of the micro DGs, and the design conditions of the AFG. First, the micro PDs were designed with I_{Pmbc} of 20A and I_{Pmoc} of 1.5A.

The effectiveness of the micro SG simulator can be verified by simulating faults in all buses $B_{i,j}$ of the micro SG simulator and confirming that 1.5 times of fault currents $I_{F(x)}(i, j)$ are less than 20A and that $I_{F(x)}(i, j)$ are equal to or greater than 1.5 times 1.5A. In Table 3, for all cases, 1.5 times $I_{F(x)}(i, j)$ is less than 20A and $I_{F(x)}(i, j)$ is greater than 2.25A. From these results, the validity of the proposed design methodology can be verified.

Second, the PDs of the micro DGs have the I_{Dmbc} of 5A and I_{Dmoc} of 0.5A. The effectiveness of the micro SG simulator can be verified by simulating faults in all buses $B_{i,j}$ of the micro SG simulator and confirming that 1.5 times of fault currents $I_{D(x)}(i, j)$ are less than 5A and that

Table 3. The fault currents $I_{F(x)}(i, j)$

i	x	$I_{F(x)}(i, j)$					
		$B_{i,0}$	$B_{i,1}$	$B_{i,2}$	$B_{i,3}$	$B_{i,4}$	$B_{i,5}$
1	s	11.73	9.65	7.96	6.76	5.89	5.22
2	s	11.72	9.64	8.18	7.09	6.27	5.47
3	s	11.68	9.64	8.18	7.09	6.26	5.62
4	s	11.69	9.39	7.81	6.68	5.84	5.19
5	s	11.68	9.64	8.18	7.10	6.10	5.35
6	s	11.68	9.64	8.18	6.91	5.97	5.27
1	g	11.30	9.39	7.78	6.64	5.78	5.13
2	g	11.31	9.39	8.00	6.97	6.17	5.39
3	g	11.29	9.39	8.00	6.97	6.17	5.54
4	g	11.30	9.13	7.63	6.55	5.74	5.11
5	g	11.30	9.39	8.00	6.96	6.00	5.27
6	g	11.30	9.39	8.00	6.77	5.87	5.19

Table 4. The fault currents $I_{D(x)}(i, j)$

i	x	$I_{D(x)}(i, j)$					
		$B_{i,0}$	$B_{i,1}$	$B_{i,2}$	$B_{i,3}$	$B_{i,4}$	$B_{i,5}$
1	s	1.77	1.82	1.51	1.28	1.12	0.99
2	s	1.61	1.65	1.71	1.76	1.83	1.58
3	s	1.57	1.60	1.65	1.71	1.76	1.83
4	s	1.82	1.47	1.22	1.05	0.92	0.82
5	s	1.66	1.71	1.76	1.83	1.56	1.37
6	s	1.71	1.76	1.82	1.53	1.33	1.17
1	g	1.77	1.82	1.52	1.29	1.13	1.00
2	g	1.62	1.66	1.71	1.76	1.83	1.59
3	g	1.57	1.62	1.66	1.71	1.76	1.82
4	g	1.82	1.48	1.24	1.06	0.93	0.83
5	g	1.67	1.71	1.77	1.82	1.57	1.37
6	g	1.71	1.77	1.82	1.54	1.34	1.18

Table 5. The total fault currents $I_{FT(x)}(i, j)$

i	x	$I_{FT(x)}(i, j)$					
		$B_{i,0}$	$B_{i,1}$	$B_{i,2}$	$B_{i,3}$	$B_{i,4}$	$B_{i,5}$
1	s	13.48	11.50	9.46	8.05	6.97	6.11
2	s	13.31	11.31	9.89	8.79	8.04	6.93
3	s	13.21	11.27	9.84	8.78	7.98	7.33
4	s	13.52	10.89	9.05	7.72	6.72	5.92
5	s	13.31	11.36	9.94	8.91	7.59	6.60
6	s	13.37	11.42	10.02	8.42	7.25	6.33
1	g	13.05	11.16	9.24	7.84	6.79	5.97
2	g	12.87	10.99	9.64	8.63	7.85	6.80
3	g	12.83	10.95	9.59	8.58	7.80	7.19
4	g	13.11	10.58	8.81	7.52	6.52	5.78
5	g	12.92	11.05	9.70	8.69	7.43	6.47
6	g	12.98	11.11	9.76	8.23	7.08	6.20

$I_{D(x)}(i, j)$ are equal to or greater than 1.5 times 0.5A. In Table 4, for all cases, 1.5 times $I_{D(x)}(i, j)$ is less than 5A and the $I_{D(x)}(i, j)$ is greater than 0.75A. Also, all fault currents from the DGs are in the range of 3.5 to 8 times the rated currents of the DGs.

Third, a micro AFG with I_{AFG} of 30A was designed to generate an artificial fault on the micro SG simulator.

Its validity can be verified that 1.5 times of total fault currents $I_{FT(x)}(i, j)$, obtained from the fault simulations in all line buses $B_{i,j}$ of the micro SG simulator, are less than the predefined I_{AFG} of 30A. In Table 5, for all cases, it can be seen that the 1.5 times of max $\{I_{FT(x)}(i, j)\}$ is 20.22A and less than 30A. These results further verify the validity of the proposed design methodology.

4.2 Effectiveness of the fault analysis method

The micro SG simulator design requires repetitive fault current computations to determine specifications that meet the design conditions of micro PDs and to get the fault current information. This is necessary to determine the specifications of micro AFG and PDs of micro DGs. Only $I_{F(x)}(i, j)$, $I_{D(x)}(i, j)$ and $I_{FT(x)}(i, j)$ among the fault currents are directly utilized in the design procedure. Therefore, the effectiveness of the fault analysis method can be verified by comparing $I_{F(x)}(i, j)$, $I_{D(x)}(i, j)$ and $I_{FT(x)}(i, j)$, obtained by applying the fault analysis method and EMTP-RV to the micro smart grid simulator model shown in Table 2.

Fig. 7 shows the percent values ε of the differences between the fault current values obtained by the fault analysis method and the fault current values obtained by EMTP-RV simulation in the cases of a three phase short fault and a single phase ground fault at fault location $B_{i,j}$ on the micro SG simulator model. In Fig. 7, $\varepsilon_{F(s)}(i, j)$ and $\varepsilon_{F(g)}(i, j)$ indicate the ε values obtained from the three phase short fault and the single phase ground fault for the line bus $B_{i,j}$, respectively. The EMTP-RV simulation results are already given in Table 3. The ε value is represented in Eq. (15). In Eq. (15), I_{EMTP} and I_{FAM} represent the fault current value obtained by the EMTP-RV simulation, and the fault current value obtained by the fault analysis method, respectively.

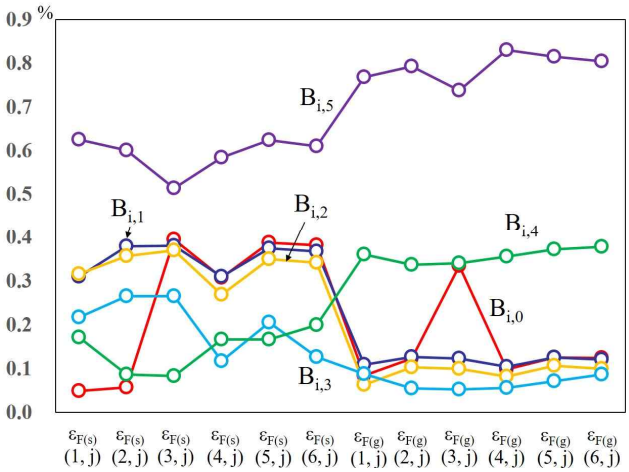

Fig. 7. The $\varepsilon_{F(x)}(i, j)$ values obtained from the fault analysis method and EMTP-RV simulation

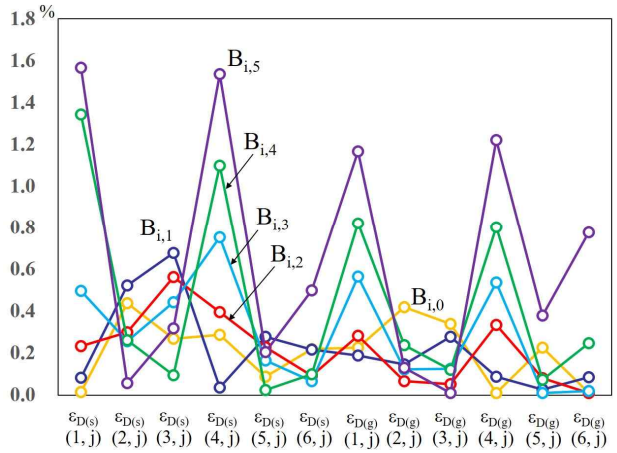

Fig. 8. The $\varepsilon_{D(x)}(i, j)$ values obtained from the fault analysis method and the EMTP-RV simulation

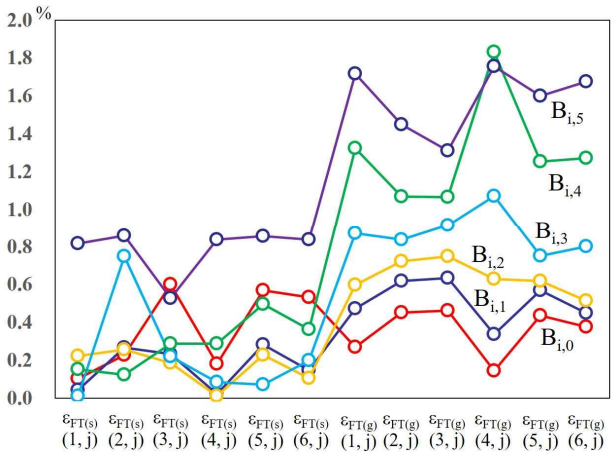

Fig. 9. The $\varepsilon_{FT(x)}(i, j)$ values obtained from the fault analysis method and EMTP-RV simulation

$$\varepsilon = \frac{I_{EMTP} - I_{FAM}}{I_{EMTP}} \times 100 \quad (15)$$

The most important point in the micro SG simulator design process is to determine the MBC of the PDs that plays the most crucial role in downsizing the micro SG simulator. That is, the accuracy of the $I_{F(x)}(i, j)$ among the fault currents is very important. From Table 6, it is proved that the $I_{F(x)}(i, j)$ values by the fault analysis method can be accurately calculated since ε values are all within 1%.

Fig. 8 shows the percent values ε of the differences between the $I_{D(x)}(i, j)$ obtained by the fault analysis method and the fault current obtained by EMTP-RV simulation, in cases of a three phase short fault, and a single phase ground fault at fault location $B_{i,j,}$ on the micro SG simulator model.

In Fig. 8, $\varepsilon_{D(s)}(i, j)$ and $\varepsilon_{D(g)}(i, j)$ indicate the ε values between $I_{D(s)}(i, j)$ for the three phase short fault, and between $I_{D(g)}(i, j)$ the single phase ground fault on the fault location $B_{i,j}$, respectively. The EMTP-RV simulation results are already presented in Table 4. When the DG is located near the CB and a fault occurs at the end of the line (bus $B_{i,5}$), ε for the $I_{D(x)}(i, j)$ increases but it remains within 1.6% and the δ value of I_{Dopc} of DGs is 2, which has no effect on the design results. This proves that the proposed fault analysis method is very effective for the fault analysis of the micro smart grid simulator model.

Fig. 9 shows the % values ε of the differences between the $I_{FT(x)}(i, j)$ obtained by the fault analysis method and the $I_{FT(x)}(i, j)$ obtained by EMTP-RV simulation in the case of a three phase short fault, and in the case of a single phase ground fault of fault location $B_{i,j}$ on the micro SG simulator. In Fig. 9, $\varepsilon_{FT(s)}(i, j)$ and $\varepsilon_{FT(g)}(i, j)$ indicate the ε values between $I_{FT(x)}(i, j)$ for the three phase short fault, and for the single phase ground fault on the ith micro DL, respectively. The EMTP-RV simulation results are already presented in Table 5. It can be seen that, as in the first micro DL F_1 and the fourth micro DL F_4, when the DG is on the starting location of the line and the fault occurs at the end of the DL, the error ε can be slightly higher compared to other cases. This is because the $I_{FT(x)}(i, j)$ obtained from EMTP-RV can be smaller than that calculated by the fault analysis method due to currents flowing into the load from the $I_{F(x)}(i, j)$.

However, fault current values calculated from the fault analysis method are greater than those of EMTP-RV for all fault cases and the ε values are less than 1.8%, which has no effect on the design result of the I_{AFG} of micro AFG.

5. Conclusions

In this study, a methodology was proposed to reduce the electrical level and space size of the smart grid to a predetermined scale, and based on the design methodology a miniaturized micro SG simulator that can safely and freely observe the electrical phenomena was designed. This new design can aid to test control strategies for disturbances on the smart grid under safe electrical levels with minimum economic and spatial costs. The micro SG simulator has the same configuration as the actual smart grid except that a substation transformer has the wiring of Δ-Y_g instead the wiring of Y_g-Y_g-Δ and has a substation transformer capacity of 190VA, voltage level of 19V, area of $4m^2$ and I_{Pmbc} of 20A, which are obtained by downscaling the substation transformer capacity of 45MVA, voltage level of 23kV and area of several km^2. Thus it was possible to downsize the smart grid to over one thousandth and also reduced the 12kA MBC of the smart grid to 1/600 based on the design methodology proposed in this paper. Through the EMTP-RV simulation verification process, the effectiveness of the proposed design methodology and the micro SG

simulator developed using the proposed design methodology was verified by showing that the all fault currents were within I_{Pmbc} (20A) of the micro PD, I_{Dmbc} (5A) of the micro DG and I_{AFG} (30A) of the micro AFG, and by identifying error between the fault analysis results and EMTP-RV simulation results were within the maximum 1.8% for all fault cases on the micro SG simulator.

As mentioned above, the purpose of this paper is to design the specifications of the micro smart grid simulator. Therefore, additional research on designing and manufacturing micro power facilities such as a micro ST, micro PDs, micro DLs and micro DGs will continue based on the design specifications obtained in this paper.

Acknowledgments

This work was supported by the National Research Foundation of Korea Grant funded by the Korean Government (NRF-2016R1D1A1B01013749).

Nomenclature

Variable	Definition
Z_T	The % impedance of substation transformer T
F_i	The ith distribution line of smart grid
CB_i	Circuit breaker of distribution line F_i
$B_{i,j}$	The ith line bus of distribution line F_i
$Z_{i,j}$	The % impedance of the jth line section of F_i
D_i	The ith distributed generation, which is connected to F_i
Z_{Di}	The % impedance of D_i
(x)	(s) : three phase short circuit fault or (g) : single phase ground fault
f	Fault location on the faulty distribution line
I_T	Fault current flowing from T to *f*
I_{Di}	Fault current flowing from D_i to *f*
$I_{F(x)}(i, j)$	Fault current flowing from CB_i to *f* when any fault with fault type x occurs at the jth line section of F_i
$I_{D(x)}(i, j)$	Fault current flowing from D_i to *f* when any fault with fault type x occurs at the jth line section of F_i
$I_{FT(x)}(i,j)$	Total fault current when any fault with fault type x occurs at the jth line section of F_i
Z_{TSB}	The % impedance of power grid viewed from the secondary bus of T
r_j	The number of line sections from D_i to the secondary bus of T
Z_{pi}	Path % impedance from D_i to secondary bus of T $Z_{Pi} = \sum_{j=1}^{r_i} Z_{i,j} + Z_{Di}$
Z_{Fx}	The % line impedance from the secondary bus of T to *f* on the faulty distribution line
Z_{Fy}	The % line impedance from *f* to DG connected to the faulty distribution line
Z_α	The % line impedance from the secondary bus of T to the position of D_k
x	The % impedance of fault current limiter
Z_χ	Z_α minus Z_{Fx}.
Z_{UV}	Total % impedance considering the power grid, and all distributed generations except D_k viewed at the secondary bus of T
Z_{UW}	Total % fault impedance
I_s	Three phase short circuit fault current
I_g	Single phase ground fault current
V_{MVD}	Maximum allowable voltage drop
I_{FR}	Rated current of distribution line
I_{EC}	Maximum allowable current of distribution line
P_L	Line section load
P_M	Substation transformer capacity
Z_{LS1}	The % positive sequence impedance of line section
I_{Pmbc}	Maximum breaking current of protective device
I_{Pmoc}	Minimum operating current of protective device
I_{Dmbc}	Maximum breaking current of distributed generation
I_{Dmoc}	Minimum operating current of distributed generation
I_{AFG}	Maximum allowable current of artificial fault generator
λ	Safety factor that protective devices have sufficient fault current blocking capability
δ	Safety factor that is introduced in order for the protective devices to work clearly.
$\varepsilon_{F(x)}(i, j)$	Error rate (ε) value between $I_{F(x)}(i, j)$s obtained from fault analysis and EMTP-RV simulation when a fault with fault type x occurs on the line bus $B_{i,j}$.
$\varepsilon_{D(x)}(i, j)$	Error rate (ε) value between $I_{D(x)}(i, j)$s obtained from fault analysis and EMTP-RV simulation when a fault with fault type x occurs on the line bus $B_{i,j}$.
$\varepsilon_{FT(x)}(i,j)$	Error rate (ε) value between $I_{FT(x)}(i, j)$s obtained from fault analysis and EMTP-RV simulation when a fault with fault type x occurs on the line bus $B_{i,j}$.

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