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Implementation and Evaluation of Interleaved Boundary Conduction Mode Boost PFC Converter with Wide Band-Gap Switching Devices

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Abstract

The implementation and performance evaluation of an interleaved boundary conduction mode (BCM) boost power factor correction (PFC) converter is presented in this paper by employing three wide band-gap switching devices: a super junction silicon (Si) MOSFET, a silicon carbide (SiC) MOSFET and a gallium nitride (GaN) high electron mobility transistor (HEMT). The practical considerations for adopting wide band-gap switching devices to BCM boost PFC converters are also addressed. These considerations include the gate drive circuit design and the PCB layout technique for the reliable and efficient operation of a GaN HEMT. In this paper it will be shown that the GaN HEMT exhibits the superior switching characteristics and pronounces its merits at high-frequency operations. The efficiency improvement with the GaN HEMT and its application potentials for high power density/low profile BCM boost PFC converters are demonstrated.

Key words: GaN HEMT, Interleaved boundary conduction mode (BCM) boost PFC converter, Si MOSFET, SiC MOSFET, Wide band-gap switching devices

I. Introduction

As industrial and consumer electronics shrink in size and expand in functionality, the demands placed on their power supplies has become increasingly challenging. This is especially true of the power supplies employed in information-displaying electronics, such as large-screen TV sets and flat-panel commercial signage, since they require both a lower profile and higher power density. For these off-line power supplies, the interleaved boundary conduction mode (BCM) boost power factor correction (PFC) converter [1]-[6] has been commonly used as a viable front-end ac-to-dc converter topology. High power density/low profile designs can be achieved with interleaved BCM boost PFC converters due to their main advantage of ripple current cancellation. Additionally, the volume of the aluminum heat sink is reduced by enhancing the efficiency and performance of the switching device. This in turn leads to miniaturization of the PFC converter. However, the performances of the switching devices present some practical limits in terms of the power density and thickness of BCM boost PFC converters.

Wide band-gap semiconductor devices such as silicon carbide (SiC) MOSFETs [7] and gallium nitride (GaN) high electron mobility transistors (HEMT) [8]-[11] have emerged as highly-efficient switching devices. These wide band-gap devices have been commercially available in recent years and have found potential applications in the power supplies of industrial and consumer electronics. On the other hand, conventional silicon-based MOSFETs have been developed into the super junction silicon (Si) MOSFETs [12], [13]. Each switching device has its own merits and limitations based on the nature and operational environment of the application circuits despite their common high switching performance. Therefore, it is necessary that these devices must be evaluated from the practical design perspectives so that designers can select the best switching device for their own applications.

The switching frequency of a BCM boost PFC converter constantly varies with the line voltage and output power in

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a very wide range. Additionally, the switching frequency significantly fluctuates within the period of the ac line voltage, which creates an extreme operational condition for the switching device of the BCM boost PFC converter. Therefore, it becomes a good candidate to evaluate the performance of the state of the art switching devices in real applications.

The practical issues for adopting wide band-gap switches to BCM boost PFC converters have not been fully addressed in previous publications [3]-[5]. Moreover, the performance of the state of the art switching devices, employed as the active switch in practical BCM boost PFC converters, has not been reported in the existing literature. Accordingly, this paper addresses the following important issues for the development of high power density/low profile BCM boost PFC converters using wide band-gap devices.

1) This paper presents practical techniques to achieve reliable and efficient operation of wide band-gap devices. Focuses are placed on the gate drive circuit design and the PCB layout technique to cope with the drawbacks of the GaN HEMT [14]. However, these techniques are equally applicable to other wide band-gap devices for the same application.
2) The second purpose of the paper is to experimentally evaluate the performance of wide band-gap devices in a relative manner. For this purpose, this paper presents the performance of a 500 W interleaved BCM boost PFC converter, designed for fanless operation at case temperatures below 65° C while employing the super junction Si MOSFET, SiC MOSFET or GaN HEMT.

This paper provides the practical engineering skills for the reliability and efficiency of wide band-gap devices, operating at a voltage level of 600 V with a maximum frequency of 800 kHz in the hard-switching condition. Examples of the gate drive circuit and PCB pattern design are provided, which minimize the detrimental effects on the small output capacitor of the GaN HEMT, while obtaining the full benefits of the fast switching capacity of the device.

This paper demonstrates that the GaN HEMT outperforms the other devices when employed to a BCM boost PFC converter. The GaN HEMT-based PFC converter achieves an excellent 98.5% efficiency at an input voltage of 230 V and an output power of 500 W. The paper provides the engineering insights and experimental data to support the high performance of the GaN HEMT-based PFC converter and it presents the engineering techniques to obtain such performance.

II. Power Semiconductor Devices

This section reviews the physical structures and material properties of the three semiconductor types. This section also comparatively analyzes the experimentally measured electrical parameters of the selected switching devices.

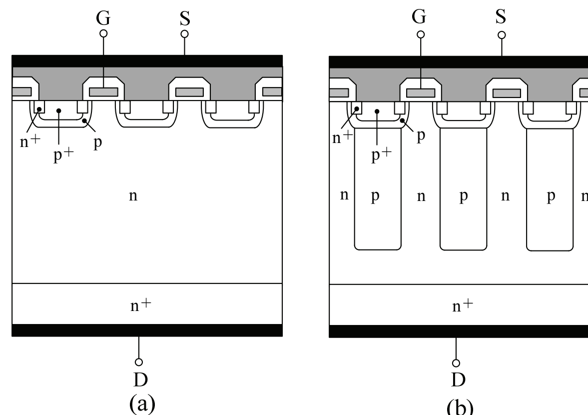


Fig. 1. Structure of conventional and super junction Si MOSFETs: (a) Conventional Si MOSFET, (b) Super-junction Si MOSFET.

A. *Super Junction Silicon MOSFET*

As an off-line power supply, the BCM boost PFC converter requires a MOSFET switch whose drain-source breakdown voltage exceeds V_{DS} = 600 V [15]. Fig. 1 depicts the structure of the two different MOSFETs. Both of them were devised to sustain a high voltage stress. Fig. 1(a) shows the conventional Si MOSFET, which consists of the thick layer of the lightly-doped n-type epitaxial region that is called the n-type drift layer. This structure increases the on-state resistance while providing the required voltage sustaining capacity. Therefore, it requires a wide chip area to deliver the rated current.

Fig. 1(b) shows the structure of the super junction Si MOSFET [12], [13]. To reduce the on-state resistance, the doping density is increased in the n-type drift layer. As illustrated in Fig. 1(b), p-type trenches are embedded into the n-type drift layer to acquire a high breakdown voltage with narrower cell pitches. This structure significantly decreases the on-state resistance, which increases the current density and decreasing the chip area. Furthermore, this structure also improves the switching characteristics while lessening the gate charge and output capacitance. In this paper, an IPW65R095C7 from Infineon [16] is adopted as a reference device for the super junction Si MOSFET.

B. *Wide Band-Gap Devices*

The structures of the two types of wide band-gap devices (SiC MOSFET and GaN HEMT) are shown in Fig. 2. The band-gap energy of the SiC is about three times that of the silicon case [14]. This allows the SiC MOSFET to be structured to offer a small turn-on resistance, while sustaining a large drain-source voltage. A thin n-type drift layer can be seen in the SiC MOSFET in Fig. 2(a), whose doping concentration is enhanced to lower the turn-on resistance. However, the breakdown voltage remains high because of the large band-gap energy. One demerit of SiC MOSFETs is that the thin n-type drift layer results in a large parasitic

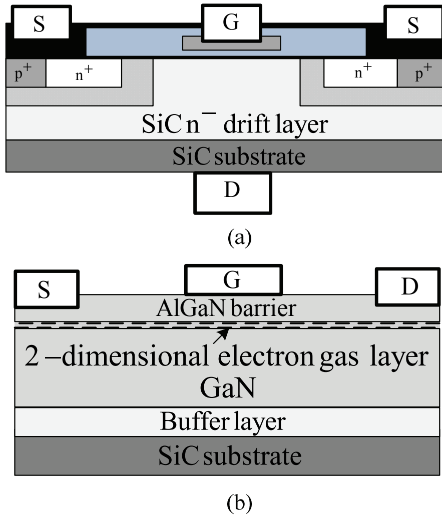


Fig. 2. Structure of wide band-gap switching devices: (a) SiC MOSFET, (b) GaN HEMT.

capacitance, which deteriorates the switching characteristics. For this comparative study, a MSA20K2D from Sanken [17] is selected as the reference SiC MOSFET.

Fig. 2(b) shows a cross-sectional view of a typical GaN HEMT [9], [18]. The GaN HEMT is usually fabricated in a lateral structure as shown in Fig. 2(b). Like the SiC, the band-gap energy of the GaN is approximately triples that of the silicon case. The most distinctive feature of this device is the existence of a 2-dimensional electron gas layer, which is formed at the heterojunction between the GaN and AlGaN. This 2-dimensional electron gas layer enhances the mobility of electrons, which in turn increases the current density of the channel and decreases the chip area required for the rated current. The lateral structure of the GaN HEMT reduces the gate charge and output capacitance, which improves the switching characteristics of the device. In addition, a typical GaN HEMT occupies only one-third of the chip area that is generally required with a super junction Si MOSFET for the same application. A RFJS1506F from RFMD [19] is chosen for the reference GaN HEMT in this comparative study.

The three switching devices are commonly molded in the TO-3P package. As a result, it offers a fair evaluation of the thermal performance of the application circuit.

C. Static and Dynamic Performance of Switching Devices

The electrical parameters/characteristics of the three state of the art switching devices are measured using a B1505 Power Device Analyzer from Agilent [20]. The electrical parameters of the three selected switching devices for this study are compared in Table I. A comparison of the measured parameters shows that the GaN HEMT offers superior characteristics over the other two devices. The on-resistance, chip area, gate charge and output capacitor of the GaN HEMT are all smaller than those of the other devices. In particular, the on-resistance specific area and gate charge of the GaN HEMT are at least one-third those of the other devices. These characteristics provide an excellent figure of the merits for the conduction loss [21], which is defined as the product of the on-resistance and the chip area: R_{DS} × Chip area = 0.39 $\Omega\cdot mm^2$. The GaN HEMT also exhibits an outstanding figure of the merits for the switching loss [21], which is the product of the on-resistance and the gate charge: $R_{DS} \times Q_G$ = 1.36 Ω·nC. These two merits of the GaN HEMT device greatly surpass the theoretical limits of silicon-based devices.

The parameters/characteristics of the three switching devices under specified operational conditions are shown in Fig. 3. The data are experimentally measured from the selected devices. A B1505A power device analyzer, from Agilent [20], was used to measure and analyze the experimental data. The test set-ups were built based on [20].

Fig. 3(a) exhibits the on-resistances of the three switching devices, measured while varying the ambient temperature. The GaN HEMT invariably depicts the smallest on-resistance, while the SiC MOSFET maintains a near constant on-resistance irrespective of the ambient temperature. On the other hand, the on-resistance of Si MOSFET almost doubles when the ambient temperature rises from 25 °C to 110 °C.

When temperature rises, the mobility of electrons decreases due to increased lattice vibrations, which impede the electron flow. This in turn, increases the on-resistance. This effect is most pronounced in the Si MOSFET with the smallest band-gap energy. The presence of a 2-dimensional electron gas layer offers the smaller on-resistance for the GaN HEMT. With a larger band-gap energy, the increasing rate of the on-resistance is also reduced. On the other hand, a greater thermal conductivity and a larger band-gap energy of the SiC results in a near constant on-resistance for the SiC MOSFET.

Fig. 3(b) shows the output capacitances of the three devices. These capacitances are measured while varying the drain-source voltage. Both the super junction Si MOSFET and the GaN HEMT present a small output capacitance. On the other hand, the SiC MOSFET exhibits a considerably larger output capacitance. This is mainly due to the presence of a thin n-type drift layer. The larger output capacitance generates turn-off ringings when combined with the parasitic inductors, which increases the switching losses. Fig. 3(c) displays turn-on waveforms of the gate voltage and drain current of the three switching devices. For both the GaN HEMT and the SiC MOSFET, the drain current starts flowing when the gate voltage reaches 2.5 V. However, all of the switching device require different gate voltages to deliver the rated current of I_D = 1 mA. The GaN HEMT delivers the rated current when the gate voltage becomes 3.1 V. The trans-conductance of the GaN HEMT is large due to the fast-current increasing slope. On the other hand, the SiC MOSFET carries the rated current of I_D = 1 mA when the gate voltage approaches 6 V. The trans-conductance of the

TABLE I
PARAMETERS OF THREE SWITCHING DEVICES

	Super junction Si MOSFET	SiC MOSFET	GaN HEMT
Device	IPW65R095C7	MSA20K2D	RFJS1506F
Manufacturer	Infineon	Sanken	RFMD
Package	PG-TO 247	TO3P	TO-247
Breackdown voltage: $V_{DC\,max}$ (V)	650	1200 *	650
On-resistance: R_{DS} (Ω)	0.084	0.10	0.075
Chip Area: (mm^2)	16.96	16.81	5.2
$R_{DS}\times$ Chip Area (Ω·mm^2)	1.42	1.68	0.39
Gate Charge: Q_G (nC)	45	106	16
Output capacitor: C_{OSS} (nF)	50	190	45
$R_{DS}\times Q_G$ (Ω·nC)	3.78	10.6	1.36

*Due to the larger band-gap energy, the n-type drift layer of the SiC MOSFET is much thinner than that of the Si MOSFET. For a 650 V SiC MOSFET, the drift layer is very thin. This reduces the on-resistance at the expense of a greatly increased output capacitor. The larger output capacitor in turn increases the turn-off switching loss, which makes the 650 V SiC MOSFET less appropriate for high-frequency operation. For this reason, a 650 V SiC MOSFET for high-frequency applications is not commercialized yet [14]. In this study, a 1200 V SiC MOSFET is used, which has the nearest parameters to those of the 650 V Si MOSFET and GaN HEMT.

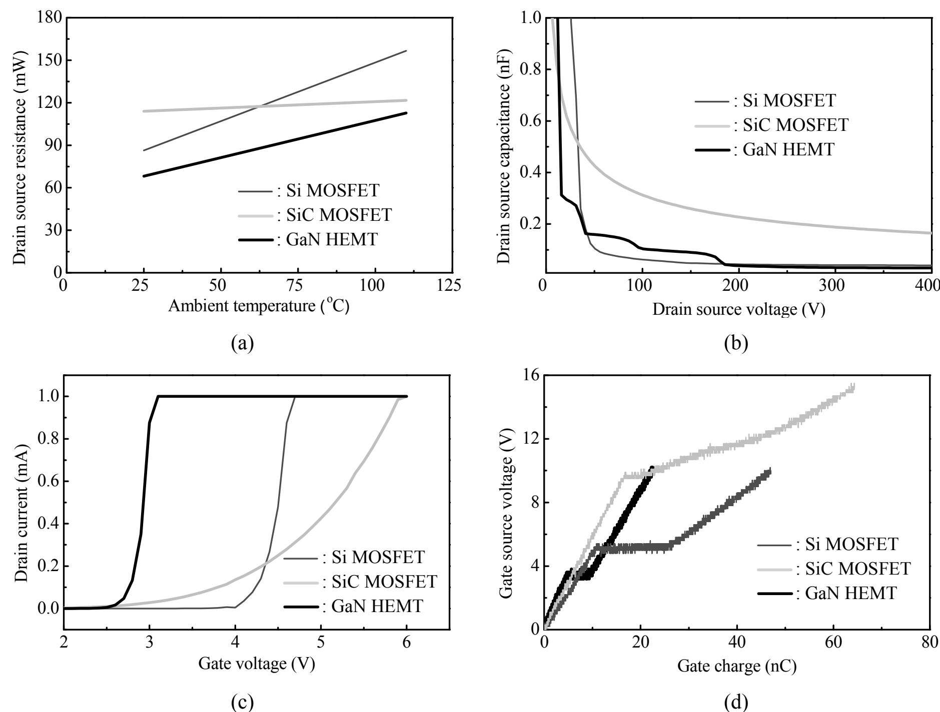


Fig. 3. Static and dynamic characteristics of the switching devices: (a) On-resistance at different temperatures; (b) Output capacitor at different drain-source voltages; (c) Turn-on characteristics; (d) Gate charge.

SiC MOSFET is smaller. Therefore, a longer time period is required to complete the channel formation. For the case of the super junction Si MOSFET, the trans-conductance is large. However, the initial voltage to trigger the current flow is about 4 V.

Lastly, Fig. 3(d) illustrates the gate charge of the three switches. The gate charge enables engineers to calculate the amount of current required for the drive circuit to turn on the switch in a desired period. The GaN HEMT shows the fastest switching characteristics, while the SiC MOSFET reveals the slowest response.

The earlier discussions all reveal that the GaN HEMT demonstrates superior switching characteristics. Thus, it can be the best device for high-frequency BCM boost PFC converters. Experimental confirmation of this statement will be provided later.

III. PROTOTYPE INTERLEAVED BCM BOOST PFC CONVERTER

A prototype interleaved BCM boost PFC converter employing the three switching devices is presented in this section.

A. Prototype Interleaved BCM Boost PFC Converter

Fig. 4 shows a circuit diagram of a 500 W prototype interleaved BCM boost PFC converter. The two BCM boost PFC modules operate in an interleaved manner to effectively reduce the inductor current ripple. A control IC R2A20117 from Renesas [22] is used to implement the standard closed-loop control. The voltage feedback circuit is configured with a trans-conductance op amp inside the control IC.

The prototype interleaved BCM boost PFC converters are shown in Fig. 5. The converters include two active switches and two diodes. They are all mounted on a common heat sink, along with the other circuit components. The control circuit is located on the rear side of the PCB.

The super junction Si MOSFET IPW65R095C7 is utilized for the active switches Q_1 and Q_2 of the prototype converter given in Fig. 5(a). To keep the case temperature below 65 °C with fanless operation, the converter is designed at a minimum baseline switching frequency of $f_{s\,base} = 65$ kHz. While meeting the thermal specifications, the converter is manufactured with dimensions of 160 mm × 155 mm × 25 mm.

The prototype converter, implemented with the SiC MOSFET MSA20K2D, is shown in Fig. 5(b). For operation with $f_{s\,base} = 200$ kHz, the heat sink dimensions are doubled, when compared with the Si MOSFET case at $f_{s\,base} = 65$ kHz. The converter is constructed with dimensions of 195 mm × 155 mm × 25 mm.

The prototype converter with the GaN HEMT RFJS1506F is shown in Fig. 5(c). With the superior properties of the GaN HEMT, the converter dimensions are significantly reduced to 100 mm × 155 mm × 25 mm for the same thermal specification at $f_{s\,base} = 200$ kHz. The benefits of high-frequency operation with the GaN HEMT can be readily seen by comparing the dimensions of the heat sink and the inductor shown with red and white lines in Fig. 5. A comprehensive performance evaluation of the PFC converters is given in a later section.

B. Variation of the Switching Frequency

The switching frequency of a BCM boost PFC converter varies widely as a function of both the line voltage and the output power, as demonstrated in earlier publications. Furthermore, the switching frequency varies instantaneously within the line voltage period. The instantaneous switching frequency f_s is evaluated as [1], [23]:

$$f_s = \frac{V_{rms}^2}{2LP_O}\left(1 - \frac{\sqrt{2}V_{rms}\sin\omega t}{V_O}\right) \tag{1}$$

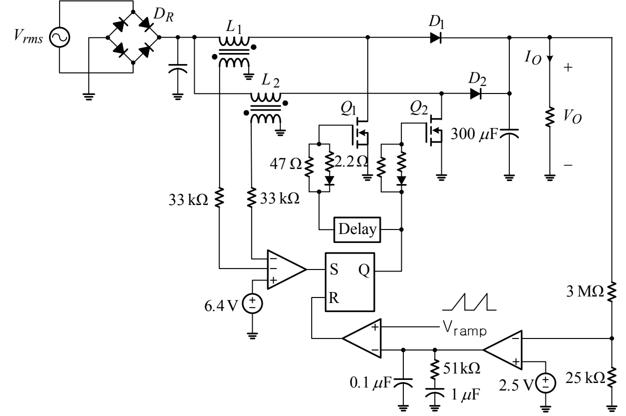


Fig. 4. Simplified circuit diagram of an interleaved BCM boost PFC converter with V_{rms} = 100-230 V, V_O = 390 V, I_O = 0.12-0.28 A, D_R: LVB2560 from Vishay, and D_1 and D_2: BVY10X-600P from NXP.

where V_O is the output voltage, V_{rms} is the rms value of the line voltage, and P_O is the output power. Equation (1) shows that the switching frequency varies as:

$$\frac{V_{rms}^2}{2LP_O}\left(1 - \frac{\sqrt{2}V_{rms}}{V_O}\right) < f_s < \frac{V_{rms}^2}{2LP_O} \tag{2}$$

The maximum switching frequency appears at the edges of the half line-voltage period. Meanwhile, the minimum switching frequency occurs at the center of the half line voltage period, which is referred to as the baseline switching frequency $f_{s\,base}$.

The baseline switching frequency variation of the prototype converter for given operational conditions is given in Fig. 6. Fig. 6(a) illustrates the baseline switching frequency when the input voltage varies between 90 V < V_{rms} < 250 V, while the output power is fixed at P_O = 500 W. The baseline switching frequencies for the given input voltage range are calculated using (2). The results are then divided by the baseline switching frequency evaluated with V_{rms} = 90 V to produce the normalized frequency. Fig. 6(a) reveals that the baseline switching frequency could be increased up to 200% while varying the input voltage within the given range. Similarly, the baseline switching frequencies, evaluated for 50 W < P_O < 500 W with V_{rms} = 230 V, are normalized to the baseline switching frequency at P_O = 500 W and V_{rms} = 230 V. The resulting curve is shown in Fig. 6(b), which indicates that the baseline switching frequency increases up to five times when the converter operates at the minimum load current I_O = 0.12 A. This widely varying switching frequency should be considered when evaluating the performance of the switching devices in the boost PFC converter.

C. Baseline Switching Frequency and Inductor Design

The performance of the prototype boost PFC converter is evaluated under three different baseline switching frequencies,

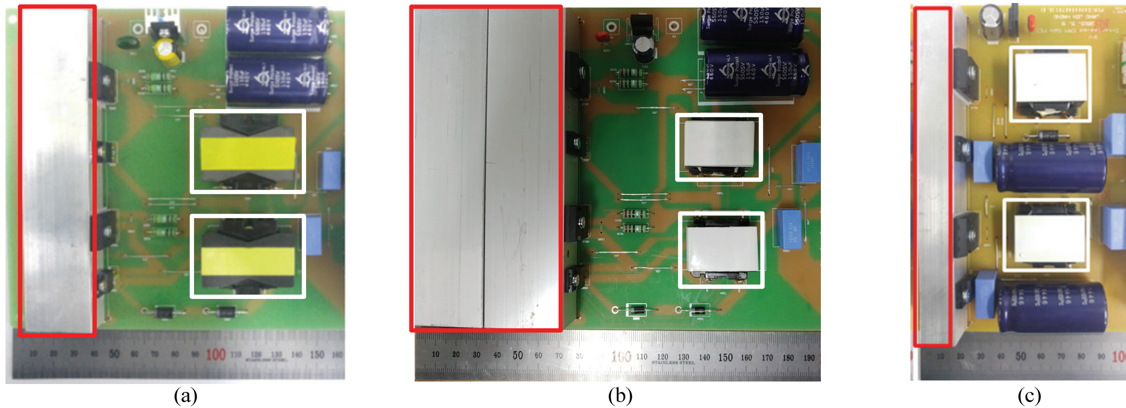


Fig. 5. 500 W prototype interleaved BCM boost PFC converters when constructed with a: (a) Super junction Si MOSFET IPW65R095C7, (b) SiC MOSFET MSA20K2D, (c) GaN HEMT RFJS1506F.

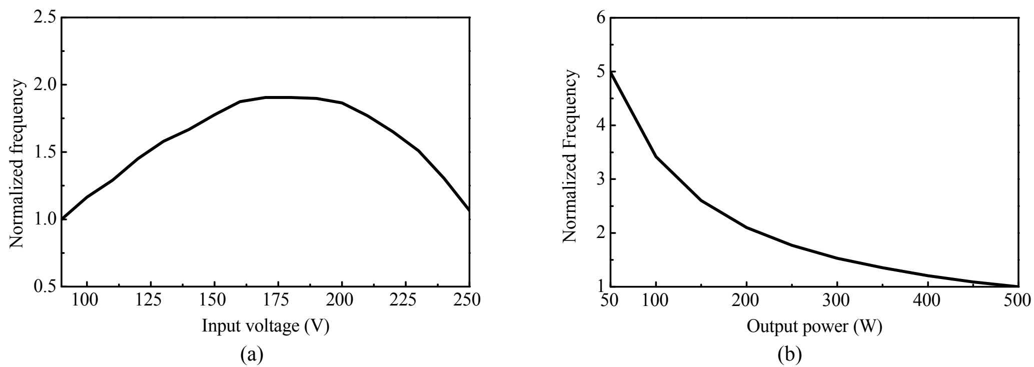


Fig. 6. Baseline switching frequency variation: (a) with respect to input voltage variations; (b) with respect to output power variations.

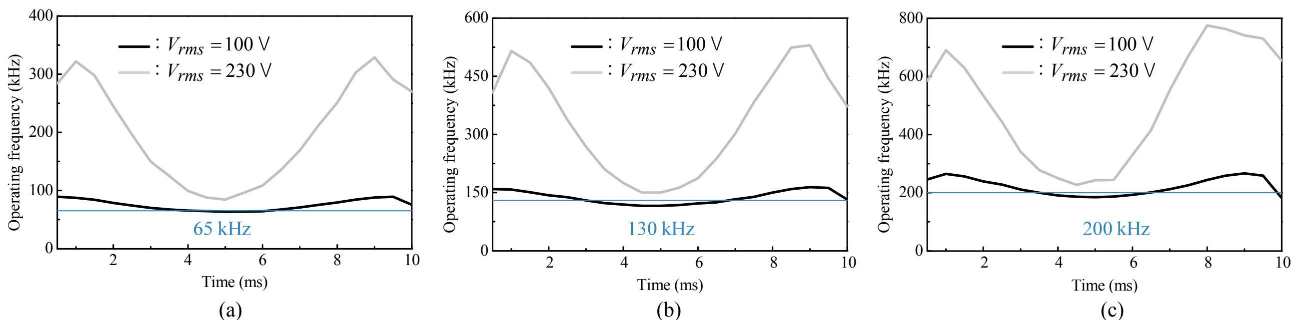


Fig. 7. Instantaneous switching frequency variation within half of a line-voltage period: (a) $f_{sbase} = 65$ kHz ; (b) $f_{sbase} = 130$ kHz ; (c) $f_{sbase} = 200$ kHz .

$f_{sbase} = 65$ kHz , $f_{sbase} = 130$ kHz and $f_{sbase} = 200$ kHz . The baseline switching frequencies are selected in consideration of the IEC 61000-3-2 and CISPR 22 EMC standards for conducted emission noise. This analysis offers useful insight to judge the relative merits of the three switching devices in high-frequency operation.

The instantaneous switching frequency variation of the PFC converter over a half line-voltage period is depicted in Fig. 7. Under the full load condition I_O = 1.28 A, the instantaneous switching frequencies are shown in Fig. 7, with baseline frequencies of $f_{sbase} = 65$ kHz , 130 kHz and 200 kHz at V_{rms} = 100 V. When V_{rms} = 230 V and $f_{sbase} = 200$ kHz , the instantaneous switching frequency rises more than three times when compared to the baseline switching frequency and approaches 800 kHz .

For each of the three baseline switching frequency conditions [23], the three different inductors are designed using the following equation:

$$L = \frac{V_{rms}^2}{f_{sbase} V_O I_O \left(1 + \frac{\sqrt{2} V_{rms}}{V_O - \sqrt{2} V_{rms}}\right)} \tag{3}$$

TABLE II
INDUCTOR DESIGN SUMMARY

Baseline switching frequency	65 kHz	130 kHz	200 kHz
Inductance	160 μH	80 μH	45 μH
Winding turns	32	16	10 (PQ4124) 15 (EE3124)
Wire diameter x Strands	USTC 0.1ϕ × 100		
Magnetic core	EE3124(200 kHz) or		
	PQ4124(65 or 130 kHz)		
Core material	PC47		

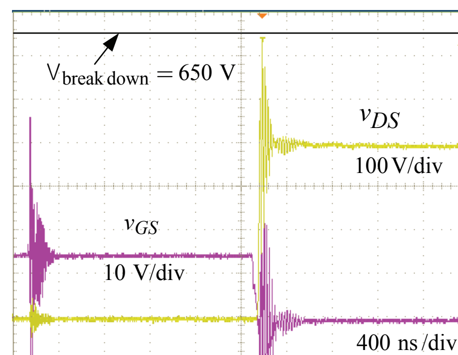
For the operational conditions of $f_{s\,base}$ = 65 kHz, 130 kHz, and 200 kHz, the inductances are determined as 160 μH, 80 μH and 45 μH, respectively.

The core material should be selected in consideration of the wide range of the operational frequency. PC47 ferrite material from TDK is chosen for its superior high-frequency characteristics. The core dimension and the number of winding turns are determined in order to minimize the core and copper losses. The dimension of the core should be selected based on the output power, the minimum (baseline) switching frequency and the area product of the core. The inductor design results are summarized in Table II.

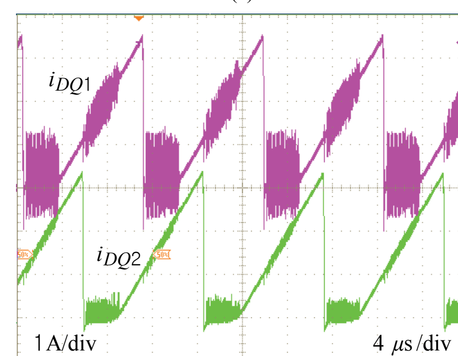
IV. PRACTICAL CONSIDERATIONS FOR THE GAN HEMT SWITCHING

As will be demonstrated in the next section, the GaN HEMT offers the best performance for the BCM boost PFC converter. Thus, this section addresses the practical engineering issues in employing a GaN HEMT as an active switch. As discussed earlier, the GaN HEMT features a lot of distinct advantages over Si MOSFET and SiC MOSFET. At the same time, the GaN HEMT has several inherent shortcomings, such as susceptibility to voltage-induced breakdown, low gate threshold voltage and proneness to high frequency turn-off oscillations [7], [14]. Thus, it is a challenging task to operate a GaN HEMT reliably and efficiently over the wide frequency range from 65 kHz to 800 kHz, under the hard-switching condition. The most common problem are the high-frequency voltage and current oscillations during the turn-off period of the switch.

This section demonstrates high-frequency voltage and current oscillations that can permanently damage the GaN HEMT. These destructive voltage/current oscillations are frequently activated by the high-voltage, high-frequency and hard-switching operation of a GaN HEMT. The current section later presents the gate drive circuit and the PCB layout technique to prevent such a catastrophic high-frequency oscillations.



(a)



(b)

Fig. 8. High-frequency oscillations during the GaN HEMT turn-off: (a) Voltage oscillation, (b) Current oscillation.

A. *High-Frequency Voltage and Current Oscillations in the GaN HEMT Switching*

During turn-off switching, the GaN HEMT is prone to destructive high-frequency oscillations in both the drain-source voltage and drain current. The small output capacitor of the device couples with the parasitic inductance in the circuit [24] to stimulate high-frequency oscillations. Fig. 8 shows examples of such oscillations. They are measured from the experimental PFC converter without any counter-measures against oscillations. As shown in Fig. 8(a), both the drain-source voltage, v_{DS}, and the gate-source voltage, v_{GS}, initiate high-frequency oscillations at the turn-off instant of the GaN HEMT. v_{DS} peaks dangerously near to the breakdown voltage of the device. This voltage peaking can result in a permanent failure of the GaN HEMT, which has little or no avalanche withstand capability [9].

v_{GS} also exhibits high-frequency oscillations in synchronization with the GaN HEMT turn offs. The v_{GS} oscillation can damage the gate terminal. More seriously, the oscillation can trigger uncontrollable turn ons during the turn-off period of the GaN HEMT, whose gate threshold voltage is notably low. Fig. 8(b) shows the current oscillation in i_D caused by the v_{GS} oscillation. Although presented in the different time scales, it can be inferred that the i_D oscillation is triggered by the v_{GS} oscillation. The following section

presents counter-measures to prevent the destructive high-frequency voltage/current oscillations demonstrated in Fig. 8.

B. Gate Driving Circuit and PCB Design

The active switch in the BCM boost PFC converter naturally achieves zero voltage turn on [1]. However, it turns off under the hard switching condition. The hard turn off could lead the high-frequency oscillations shown in Fig. 8. The gate drive circuit should be designed under careful considerations to avoid these oscillations, while fully exploiting the fast switching capacity of the device.

Fig. 9 shows the gate drive circuit employed for the prototype boost PFC converter. The main features of the gate drive circuit are listed below.

1) The use of a small 2.2 Ω gate-discharging resistance. During turn-off transitions, the GaN HEMT is exposed to a rapid rising of v_{DS} due to the small output capacitor. In turn, the high dv_{DS}/dt rate induces a large current influx into the parasitic capacitances of the device. In particular, a considerable current runs into the gate-source capacitance through the drain-gate capacitance. If the gate-discharging resistance is *not* sufficiently small, most of the current rushes into the gate terminal and instantly charges the gate voltage beyond the threshold level. This Miller turn-on spike could induce the current oscillations shown in Fig. 8(b).
2) The use of a ferrite bead right ahead of the gate terminal. During turn-off periods, the small gate-source capacitance can couple with the parasitic inductance around the gate-discharging path forming a series resonant circuit. For the purpose of damping down this resonance, while avoiding the Miller turn-on spike, a ferrite bead is used to present a high impedance to the high-frequency resonance. A ferrite bead CB 2012 GA 300 [25] is used in the experimental converter.
3) The use of an SMD-type non-inductive resistance for the current sensing resistor. The total parasitic inductance around the gate-discharging path should be minimized to reduce the chance of high-frequency resonance. The current sensing resistance, located between the source and the ground terminal, constitutes a large portion of the parasitic inductance. Thus, the use of a non-inductive windingless resistance is critical. An SMD-type 50 mΩ non-inductive resistance, CSR02TR R100F [26], is employed to reduce the total parasitic inductance to an acceptable level.

The PCB layout is another critical factor in securing stable and reliable operation of a PFC converter. The PCB pattern should be traced to provide sufficient damping for potential high-frequency oscillations. Fig. 10 illustrates the design

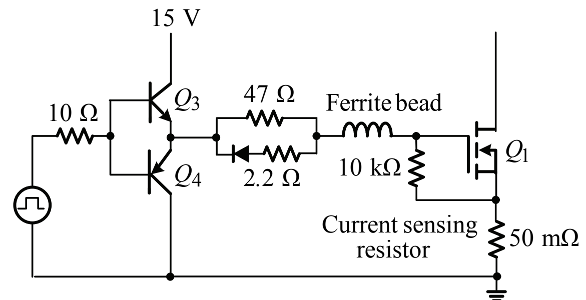
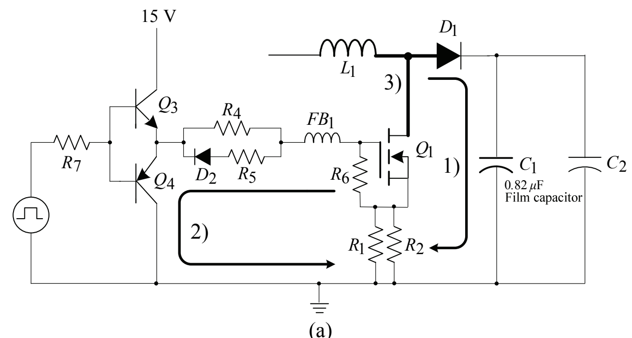
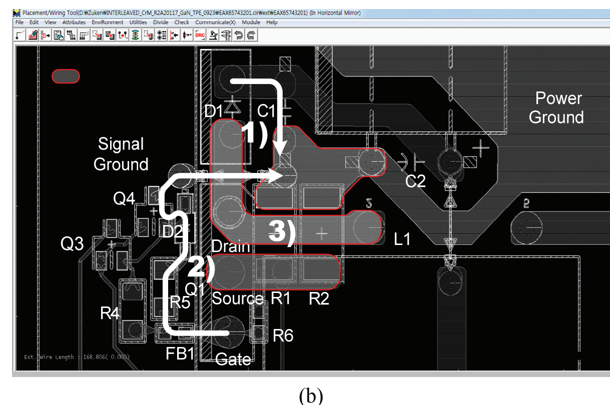


Fig. 9. Gate drive circuit for a GaN HEMT.



(a)



(b)

Fig. 10. PCB design for the experimental converter: (a) Circuit diagram, (b) PCB pattern.

points and pattern of the PCB used in the prototype PFC converter. Referring to Fig. 10(a), the PCB design guidelines are described below. They effectively damp the high-frequency oscillations, without compromising the benefits of the small output capacitor of the device.

1) Creation of a short current path along the GaN HEMT, a freewheeling diode and a 0.82 μF film capacitor connected in parallel with a bulky electric output capacitor, which is labelled as **1)** in Figs. 10(a) and (b). This current path offers an efficient filtering of the output ripple without unduly increasing the parasitic inductance.
2) Minimization of the gate-discharging path, which is labelled as **2)** in Figs. 10(a) and (b), to lower the parasitic inductance along the path.
3) Single point connection of the boost inductor, the anode terminal of the diode and the drain terminal of

the GaN HEMT, which is labelled as **3)** in Figs. 10(a) and (b), to minimize any parasitic inductance.

Fig. 10(b) shows the PCB layout of the experimental PFC converter, which incorporates the PCB layout rules described above. Fig. 11 highlights the effects of the PCB design rules by comparing the v_{GS} waveforms. Fig. 11(a) is a v_{GS} waveform before incorporating the PCB design rules, and Fig. 11(b) is a waveform with the PCB pattern of Fig. 10(b).

Although it was engineered for the GaN HEMT, the gate drive circuit and PCB layout can be employed for Si MOSFETs and SiC MOSFETs. The 15 V gate drive voltage is appropriate for proper operation of the three switches considered in this paper.

V. Efficiency Evaluation with Different Switching Devices

The performance of the three switching devices and the overall efficiency of the prototype PFC converter are discussed in this section. The turn-on loss in the BCM boost PFC circuit is negligible because this circuit naturally operates with zero-voltage turn on of the active switch. On the other hand, the turn-off loss can be critical. Fig. 12 illustrates the turn-off waveforms of the drain-source voltage v_{DS}, the drain current i_D and the product of v_{DS} and i_D for the three switching devices. v_{DS} increases linearly until it reaches the output voltage during the Miller plateau period of the gate voltage. v_{DS} ramps down to zero when the gate voltage drops from the Miller plateau to the threshold voltage. The total area formed by the $v_{DS} \cdot i_D$ product curve represents the turn-off loss. The GaN HEMT exhibits the fastest response time and the lowest turn-off loss when compared to the other switching devices.

The small gate charge and small output capacitance, listed in Table I, provide the superior turn-off behavior of the GaN HEMT. The low on-resistance and excellent switching characteristics of the GaN HEMT facilitate the device to operate at high frequencies without sacrificing the overall efficiency of the PFC converter.

Fig. 13 depicts the overall efficiency of the prototype boost PFC converter with the three switching devices operating at the low line condition of V_{rms} = 100 V. Among the three switching devices, the GaN HEMT yields the highest efficiency. In particular, the GaN HEMT invariably offers a high efficiency for heavy load conditions at $f_{sbase} = 200$ kHz. On the other hand, the efficiencies in the cases of the other devices rapidly drop under heavy load conditions due to the increased switching losses.

Fig. 14 shows the efficiency of the PFC converter at the high line condition of V_{rms} = 230 V. In this case, the GaN HEMT consistently presents higher efficiencies than the other devices for most operational conditions. The PFC converter with the GaN HEMT accomplishes an excellent 98.5% efficiency at the high line/full load condition with $f_{sbase} = 65$ kHz.

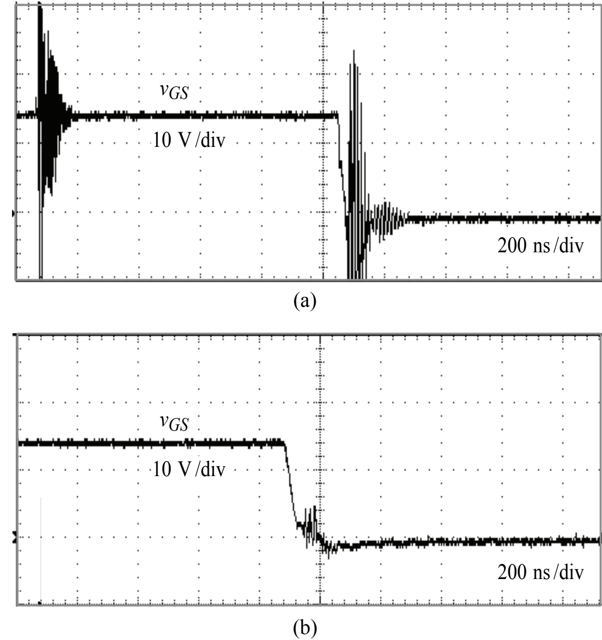


Fig. 11. v_{GS} waveforms: (a) Before PCB design optimization; (b) After PCB design optimization.

Fig. 15(a) shows the case temperature of the PFC converter of the three switching devices. Among the three switching devices, the GaN HEMT produces the lowest case temperature. Moreover, it only rises by 10 °C when the baseline switching frequency increases from $f_{sbase} = 65$ kHz to 200 kHz. The GaN HEMT operating at $f_{sbase} = 200$ kHz generates nearly the same temperature as the case of the Si MOSFET operating at $f_{sbase} = 65$ kHz. Accordingly, the baseline switching frequency can be increased threefold for the GaN HEMT device, while complying with the same temperature specifications. The reduced power loss at high frequency operation accelerates the miniaturization of the PFC converter. This again validates that the GaN HEMT facilitates the high power density/low profile implementation of the BCM boost PFC converter.

Fig. 15(b) illustrates the breakdown of the power losses of the switching devices. For all three switching devices, the conduction loss remains basically the same, regardless of the baseline switching frequency. Even so, the switching loss is quite different. The switching losses become considerable at high frequency operation with $f_{sbase} = 130$ kHz or 200 kHz for the Si MOSFET and SiC MOSFET devices. On the other hand, the switching loss becomes small and insignificant with the GaN HEMT device for all operational conditions including the case with $f_{sbase} = 200$ kHz.

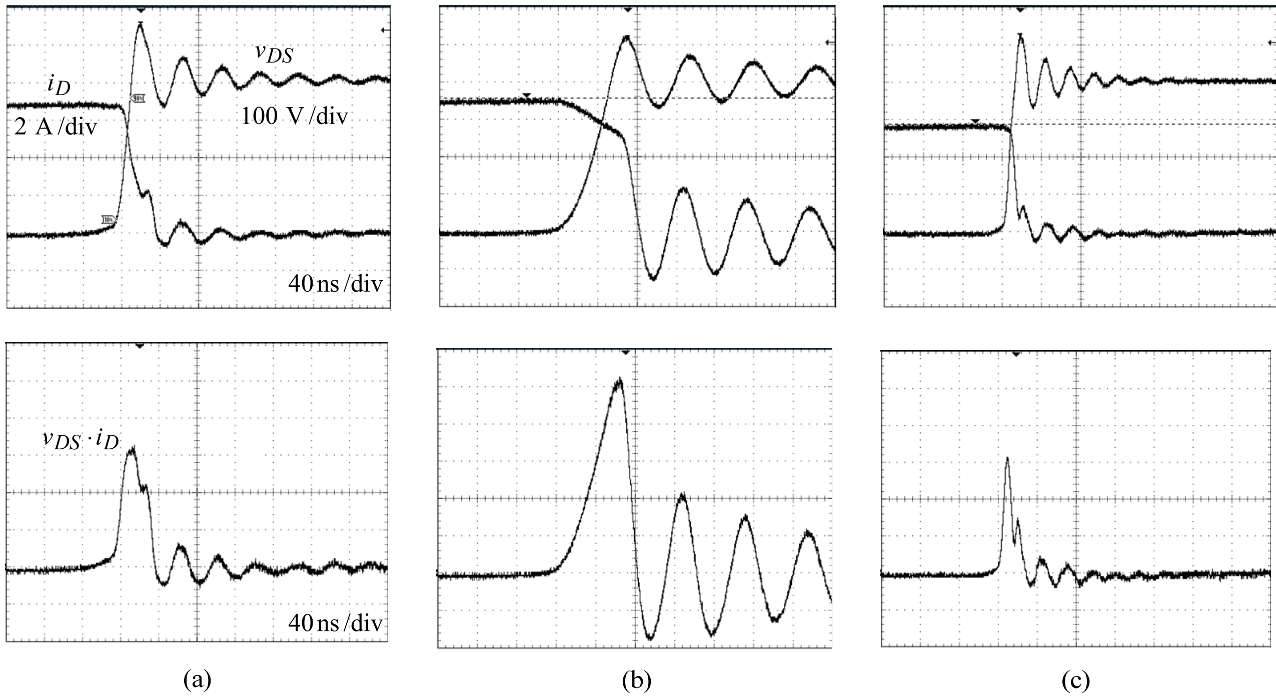


Fig. 12. Turn-off waveforms and switching loss: (a) Si MOSFET, (b) SiC MOSFET, (c) GaN HEMT.

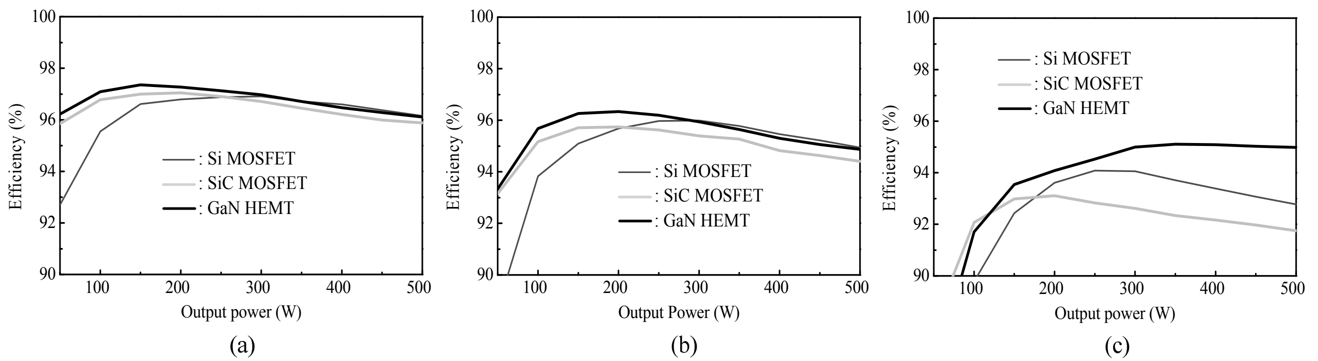


Fig. 13. Efficiency of the PFC converter at a low line voltage with different baseline switching frequencies: (a) $f_{sbase} = 65$ kHz, (b) $f_{sbase} = 130$ kHz, (c) $f_{sbase} = 200$ kHz.

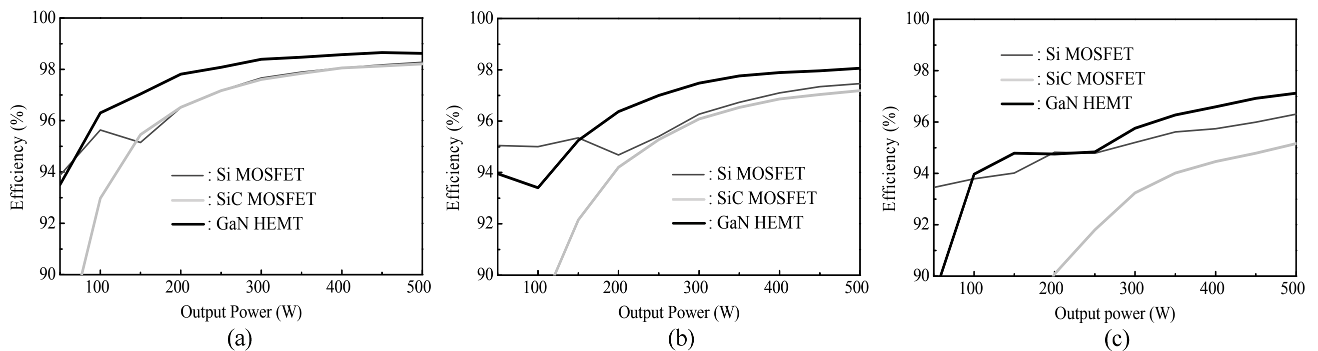


Fig. 14. Efficiency of the PFC converter at a high line voltage with different baseline switching frequencies: (a) $f_{sbase} = 65$ kHz, (b) $f_{sbase} = 130$ kHz, (c) $f_{sbase} = 200$ kHz.

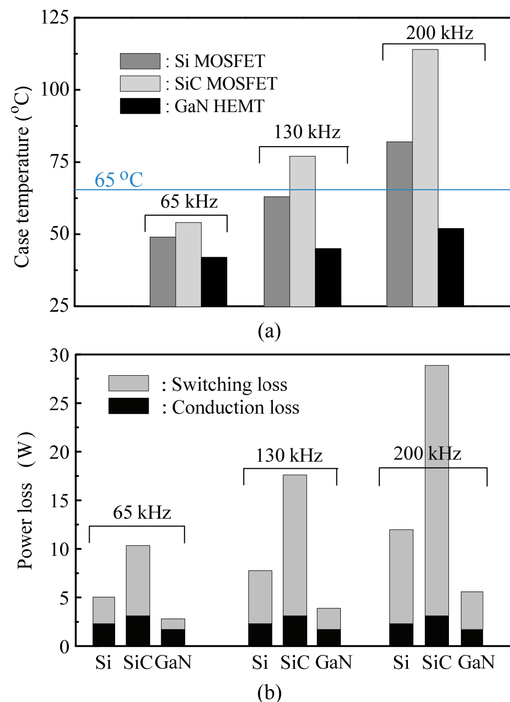


Fig. 15. Thermal performances and power losses of three semiconductor devices: (a) Case temperature, (b) Power losses.

VI. CONCLUSIONS

This paper demonstrated the implementation and performance evaluation of a 500 W interleaved BCM boost PFC converter employing wide band-gap switching devices. This paper addressed the practical engineering skills for the reliability and efficiency of wide band-gap devices operating at the voltage level of 600 V with a maximum frequency of 800 kHz in the hard-switching condition. Focuses are placed on the gate drive circuit design and PCB layout technique to cope with the drawbacks of the GaN HEMT. The techniques are equally applicable to the other wide band-gap devices for the same applications. Examples of the gate drive circuit and PCB pattern design are provided. They minimize the detrimental effects against the small output capacitor of the GaN HEMT, while attaining the full benefits of the fast switching capacity of the device.

The efficiencies and thermal performances of the BCM boost PFC circuit with three state of the art switching devices (the super junction Si MOSFET, the SiC MOSFET and the GaN HEMT) are analyzed in this paper. The impacts of the switching devices on the efficiency of the PFC converter are theoretically predicted and experimentally verified.

The GaN HEMT emerged as the most promising wide band-gap switching device for BCM boost PFC converters. The GaN HEMT provided superior performance and well pronounced its merits at high-frequency operations over the other devices. A threefold increase in the baseline switching frequency was allowed for with the GaN HEMT over the case of the super junction Si MOSFET, which was experimentally verified. This was accomplished without compromising the thermal performance of the PFC converter. The GaN HEMT will expedite the miniaturization of high power density/low profile BCM boost PFC converters for medium-power industrial and commercial electronics.

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