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High Efficiency Design Procedure of a Second Stage Phase Shifted Full Bridge Converter for Battery Charge Applications Based on Wide Output Voltage and Load Ranges

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Abstract

This work presents a high efficiency phase shifted full bridge (PSFB) DC-DC converter for use in the second stage of a battery charger for neighborhood electrical vehicle (EV) applications. In the design of the converter, Lithium-ion battery cells are preferred due to their high voltage and current rates, which provide a high power density. This requires wide range output voltage regulation for PSFB converter operation. In addition, the battery charger works with a light load when the battery charge voltage reaches its maximum value. The soft switching of the PSFB converter depends on the dead time optimization and load condition. As a result, the converter has to work with soft switching at a wide range output voltage and under light conditions to reach high efficiency. The operation principles of the PSFB converter for the continuous current mode (CCM) and the discontinuous current mode (DCM) are defined. The performance of the PSFB converter is analyzed in detail based on wide range output voltage and load conditions in terms of high efficiency. In order to validate performance analysis, a prototype is built with 42-54 V / 15 A output values at a 200 kHz switching frequency. The measured maximum efficiency values are obtained as 94.4% and 76.6% at full and at 2% load conditions, respectively.

Key words: Battery chargers, High efficiency, Phase shifted full bridge converter, Wide range load condition, Wide range output voltage regulation

I. INTRODUCTION

Nowadays, the demand for electrical vehicles (EVs) and plug in hybrid EVs is rising rapidly because of the benefits in terms of global warming and economics. Neighborhood EVs are propelled by an electric motor which is fed with power from a rechargeable battery [1]. The main problem with EVs is the battery charge. The batteries of EVs can be charged with off-board charge stations or on-board chargers from any available power outlet [2]. The on-board chargers provide the flexibility to charge a vehicle's battery from any power outlet at any time. Therefore, on-board systems encourage users to use EVs and can help increase of demand for EVs. However,

on-board chargers result in additional weight, volume and cost for EVs. The additional weight and volume have a negative effect on the performance of EVs [2]. Therefore, an on-board battery charger should be designed with a high power density [1], [4]-[6].

The high power density design of a charger can be achieved with an increase of the switching frequency. However, increasing the switching frequency results in lower efficiency due to increased switching losses. Therefore, soft switched converters are usually used in on-board battery charger systems [3]. A battery charger includes two stages, which are a front-end power factor correction boost converter and a DC-DC converter for regulating the battery output voltage [7], [8]. A phase shifted full bridge (PSFB) pulse width modulated modulation (PWM) converter and resonant converters are usually preferred in the second stage of battery chargers due to their soft switching capabilities [2], [7]-[11]. In the resonant converters, output voltage regulation is provided

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by varying the switching frequency which limits the optimization of the magnetic components. They also require high current rate semiconductors and have high conduction losses due to increased RMS currents [12]. The LLC resonant converter topology is preferred for battery charge applications over other resonant converter topologies since it has a narrow switching frequency range for output voltage regulation when compared to series resonant converters and it has a lower conduction loss under light load conditions when compared to parallel resonant converters. However, the resonant converter has a complex design procedure because the applied first harmonic approximation method can produce an error when switching frequency is far away from the resonant frequency [8], [10] and a detailed steady state analysis of the LLC converter is required to accurately predict its behavior [13], [14]. However, complex nonlinear equations do not allow for a closed-form solution. In PSFB PWM converters, a phase delay between the control signals of two diagonal switch allows for the soft switching operation of primary switches at a constant switching frequency. It has simple design procedure. Thus, a PSFB converter is used in this paper. Different design procedures for a high efficiency and high power density PSFB converter have been proposed in the literature [2], [15]-[21]. The most of them are focused on the constant output voltage required for data center or telecom applications. However, the design procedure is very different in battery charge applications due to the need for wide range output voltage regulation, especially for Lithiumion battery chargers.

In on-board EV battery chargers, Lithium-ion battery cells are usually used because of their high voltage and current rates, which provide a high power density [22], [23]. Therefore, Lithium-ion battery charger should cope with wide range output voltage regulations. According to the charge profile of Lithium-ion the battery cells, the charge process consists of the constant current (CC) mode and the constant voltage (CV) mode [10]. In the constant current mode, the battery cell charges with a constant current while its voltage is changing in a wide range. In the constant voltage mode, the battery cell reaches its maximum voltage value and continues to charge with a decreasing load. Therefore, a second stage PSFB converter should maintain its soft switching feature in the wide range output voltage regulation and wide range load condition. However, the soft switching capability of a PSFB PWM converter depends the load condition and dead time optimization [15]-[17].

Recently, high power density an on-board battery chargers with a PSFB converter have been proposed in [2] and [21]. In the design of the converters, SiC power semiconductors are evaluated to improve the efficiency and power density. However, the wide range output voltage regulation and load condition are not discussed in terms of high efficiency.

In this paper, second stage PSFB PWM converter design

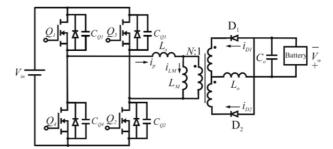


Fig. 1. Circuit schematic of the PSFB converter.

optimization based on the wide range output voltage and load condition is proposed for an on-board battery charger. The series connection of enough Lithium-ion battery cells determines the output voltage range. The soft switching operation of the converter is defined first. Then, for the CC charge mode, the optimum snubber inductances are evaluated based on the dead time requirement providing wide range output voltage regulation. In the CV charge mode, CCM and DCM boundary are determined to maintain the soft switching operation of primary switches under light load conditions based on [15] and [17]. Finally, a prototype is built to validate the proposed theoretical design approach which has 42-54 V / 15 A output values at a 200 kHz switching frequency. The soft switching operation of the converter is tested for wide range output voltage and load conditions.

II. BASIC PRINCIPLES OF THE PSFB DC-DC CONVERTER

A circuit diagram of the PSFB PWM converter is given in Fig. 1. Q_1 - Q_4 and D_1 - D_2 represent the primary MOSFETs and the rectifier diodes, respectively. L_M is the magnetizing inductance of the transformer and L_s represents the snubber inductance including the leakage inductance of the transformer and the added extra inductance to the primary side. L_o and C_o are the output filter inductor and the filter capacitor, respectively. V_{in} is the input voltage source, V_o is the battery voltage, and N represents the turns ratio of the transformer. In the operation of the converter, the Q_1 - Q_2 and Q_3 - Q_4 MOSFET pairs conduct in a half of one switching period.

A. CCM Operation Principle

Theoretical key waveforms of the converter in the CCM operation are given in Fig. 2.

At the beginning of one switching period, at $t=t_0$, Q_1 and Q_2 are turned on and the primary current increases linearly with the application of V_{in} to the primary side. Thus, D_2 is forward biased and conducts the output current.

At $t=t_1$, Q_1 is turned off, and the reflected output current starts to charge and discharge the parasitic capacitors of the Q_1 and Q_4 MOSFETs. When the discharge of the parasitic capacitor of Q_4 is completed at $t=t_2$, the antiparallel diode of

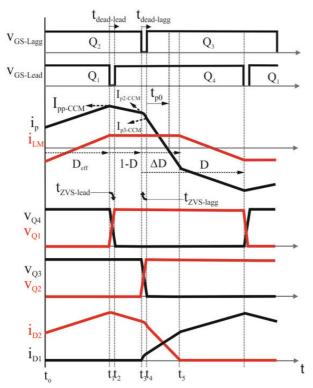


Fig. 2. Key waveforms of the PSFB PWM converter in the CCM operation.

 Q_4 is on. Thus, the voltage of the primary side of the transformer is zero. At the secondary side, D_2 still conducts the output current. During the conduction of the antiparallel diode of Q_4 , the control signal of Q_4 is applied to achieve zero voltage switching (ZVS) turn-on. The discharge of the parasitic capacitor can be achieved easily with the reflected output current to the primary side. The charge and discharge time of the parasitic capacitors in the leading leg, also known as the ZVS time interval, can be defined as:

$$t_{ZVS-lead} = \frac{(C_{Q1} + C_{Q4})V_{in}}{I_{pp-CCM}}.$$
 (1)

Where C_{Q1} and C_{Q4} define the parasitic capacitors of the Q_1 and Q_4 MOSFETs. The initial value of the primary current starting the charge and discharge process is defined as $I_{pp\text{-}CCM}$, as well as the peak value of the primary current, and it can be defined as the sum of the reflected peak output current and magnetizing current as follows:

$$I_{pp-CCM} = \frac{1}{N} (I_o + \frac{\Delta I_o}{2}) + \frac{V_{in}}{2f_s L_M} D_{eff}$$
 (2)

Where I_o is the output current, ΔI_o is the output current change, f_s is the switching frequency, and D_{eff} is the effective duty ratio of the converter. D_{eff} will be mentioned again after this part.

The dead time should allow for the full charge and discharge of the capacitors in the leading leg. This can be defined as follows:

$$t_{TVS-lead} \le t_{dead-lead}$$
 (3)

At $t=t_3$, Q_2 is off and the primary current starts to flow through the parasitic capacitors of Q_2 and Q_3 . The parasitic capacitors of Q_2 and Q_3 charge and discharge, respectively. Thus, the D_1 diode naturally conducts when the voltage of the parasitic capacitor of Q_2 is higher than the drop voltage of the leakage inductance of the transformer and D_1 . The conduction of both rectifier diodes removes the output current reflection to the primary side. Therefore, the stored energy in L_s should be enough to charge and discharge the parasitic capacitors. Otherwise, the ZVS turn-on process cannot be achieved. This can be defined as:

$$\frac{1}{2}L_{s}I_{p2-CCM}^{2} \ge \frac{1}{2}(C_{Q2} + C_{Q3})V_{in}^{2}. \tag{4}$$

Where C_{Q2} and C_{Q3} define the parasitic capacitors of the Q_2 and Q_3 MOSFETs. $I_{p2\text{-}CCM}$ is the critical primary current and it can be written as:

$$I_{p2-CCM} = I_{pp-CCM} - \frac{V_o}{2f_s L_o N} (1 - D).$$
 (5)

The output current commutation causes a lost duty ratio, ΔD , which limits the output voltage gain because no input power is transferred to the output. Therefore, the voltage gain of the PSFB converter in the CCM can be defined as follows:

$$V_o = \frac{V_{in}}{N}(D - \Delta D). \tag{6}$$

Where, D is the total duty ratio of the converter. The lost duty ratio can be extracted as:

$$\Delta D \approx \frac{2I_o L_s f_s}{NV_{in}} \ . \tag{7}$$

Thus, the effective duty ratio can be written as follows:

$$D_{\text{eff}} = D - \Delta D . \tag{8}$$

When $C_{\rm Q3}$ is discharged to zero voltage, the antiparallel diode of Q_3 turns-on. Therefore, Q_3 is turned on with ZVS at $t=t_4$. Then the inverse input voltage is applied across the primary side of the transformer. The conduction of both the D_1 and D_2 diodes continues for the output current commutation. The charge and discharge time of $C_{\rm Q2}$ and $C_{\rm Q3}$ in the lagging leg can be written as:

$$t_{ZVS-lagg} = \sqrt{L_s(C_{Q2} + C_{Q3})} t g^{-1} \frac{V_{in}}{I_{p2-CCM}} \sqrt{\frac{C_{Q2} + C_{Q3}}{L_s}}.$$
 (9)

During the output current commutation, the primary current changes its direction. If the primary current change its direction before the dead time ends, reverse resonance occurs and the discharged C_{Q3} starts to charge again. Therefore, the dead time should end before the primary current changes its direction [15], [16]. This can be defined as:

$$t_{ZVS-lagg} \le t_{dead-lagg} \le t_{p0} \tag{10}$$

Where t_{po} is the time interval when the primary current reaches zero as shown in Fig. 2. It can be written as:

$$t_{p0} = t_{ZVS-lagg} + L_{s} \frac{I_{p3-CCM}}{V_{in}}$$
 (11)

Where $I_{p3\text{-}CCM}$ is the operation point of the primary current after C_{Q2} and C_{Q3} charge and discharge, respectively. It can be extracted from the equivalent series resonance circuit during the charge and discharge process as

$$I_{p3-CCM} = \sqrt{I_{p2-CCM}^{2} - \frac{V_{in}^{2}(C_{Q2} + C_{Q3})}{L_{s}}}.$$
 (12)

At $t=t_5$, one half of a switching period is completed when the output current only flows through D_1 . The other half of a switching period works with the same principle but in the reverse direction of the primary current and voltage.

B. DCM Operation Principle

Theoretical key waveforms of the converter in the DCM operation are given in Fig. 3. The PSFB converter works in the DCM when the load current is smaller than the output current change, ΔI_o . The soft switching operation of the lagging leg switches depends on the load condition and it becomes poor at light load conditions due to insufficient energy stored in the L_s inductor. In the DCM operation, unlike the CCM operation, the stored energy in the magnetizing inductance attends the resonance that occurred during the discharge of the parasitic capacitors of the lagging leg switches due to the absence of output current commutation at the secondary side. Thus, ZVS turn-on of the lagging leg switches can be achieved by the use of magnetizing energy under light load conditions. In addition, the rectifier diodes are turned-off with ZCS. Therefore, the DCM operation of the PSFB converter is one of the most effective and simple ways to improve efficiency under light load conditions.

The PSFB converter can be operated in the DCM with an extended dead time even if the load current is higher than ΔI_o [15]. However, the increased current change at the primary and secondary sides increases the conduction losses when compared to the CCM operation with the same power rate. Therefore, the load boundary between the CCM and the DCM is important in terms of high efficiency.

At $t=t_0$, the Q_1 and Q_2 switches are on at the primary side and D_2 conducts the output current at the secondary side. At $t=t_1$, Q_1 is turned off and the reflected output current charges and discharges the parasitic capacitors of Q_1 and Q_4 as in the CCM operation. When the voltage of the Q_4 switch reaches zero at $t=t_2$, its body diode turns on and the i_{Ls} current decreases linearly with the reflected output voltage,– NV_0 . During this operation, the control signal of Q_4 is applied and it is turned-on with ZVS. At $t=t_3$, the output current falls to zero and the D_2 diode is turned off. Thus, at the primary side,

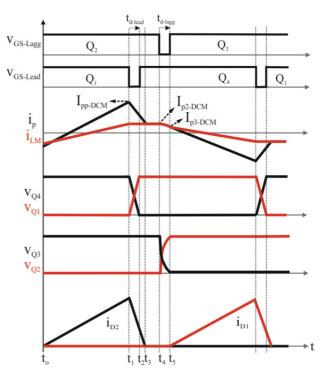


Fig. 3. Key waveforms of the PSFB PWM converter in the DCM operation.

the current flowing through L_s is equal to the magnetizing inductance current. When Q_2 is turned-off at $t=t_4$, the magnetizing current starts to charge and discharge the parasitic capacitors of Q_2 and Q_3 . It also starts to discharge the junction capacitors of the D_1 and D_2 rectifier diodes. The junction capacitor C_j is represented by $(C_j/2)x(2/N)^2$. Therefore, the magnetizing energy should be enough to discharge the parasitic and junction capacitors defined as:

$$\frac{1}{2}L_{M}I_{p2-DCM}^{2} \ge \frac{1}{2}(C_{Q3} + C_{Q2} + \frac{2C_{j}}{N^{2}})V_{in}^{2}.$$
 (13)

Where $I_{p2\text{-DCM}}$ is the operation point of the primary current when D_2 is turned-off. It can be defined as:

$$I_{p2-DCM} = \frac{V_{in}D_{DCM}}{2f_{\circ}L_{M}}.$$
 (14)

Here, D_{DCM} is the duty ratio of the PSFB converter in the DCM operation. It can be extracted from the volt-sec balance on the output filter inductor, and is defined as:

$$D_{DCM} = \sqrt{\frac{N^2 \frac{V_o^2}{V_{in}^2} f_s I_o L_o}{V_o (1 - N \frac{V_o}{V_{in}})}}.$$
 (15)

At $t=t_5$, Q_3 is turned-on and $-V_{in}$ is applied to the primary side of the transformer. Thus, one half of a switching period is completed and the other half works with the same principle.

III. DESIGN METHODOLOGY OF THE PSFB DC-DC CONVERTER

This section discusses the design parameters and operation points of the PSFB converter in terms of a high efficiency. The operation points are determined based on the Lithium-ion battery charge characteristics. The Lithium-ion battery charge characteristics include the CC and CV charge modes. Therefore, the soft switching performance of the PSFB converter is analyzed based on wide range output voltage regulation and wide range output current conditions. During the CC mode, the dead time is optimized to provide ZVS turn-on of the lagging leg MOSFETs for a wide output voltage range. In the CV mode, the CCM and DCM boundary is determined to provide ZVS turn-on of the lagging leg MOSFETS under light load conditions. Optimization of the operation points of the PSFB converter in the CC and CV modes without the addition of a snubber circuit provides less design complexity, lower cost and increased reliability.

A. Optimization of Magnetic Components

Optimization of the magnetic components includes the power transformer design and the output inductor design. The power transformer is optimized according to the low core and copper losses. The magnetic flux density variation controls the core losses and it depends on the core cross-sectional area A_{core} , the primary turns number N_p , the applied input voltage V_{in} , the switching frequency f_s and the effective duty ratio D_{eff} . It is given as follows:

$$\Delta B = \frac{V_{in} D_{eff}}{2N_p A_{core} f_s} \ . \tag{16}$$

 $D_{\it eff}$ varies while the other variables are constant during the operation of the converter, and it is determined according to the output voltage variation by the use of the voltage gain expression defined in (6).

The maximum magnetic flux density B_{max} controls the core saturation and it is equal to half the magnetic flux variation.

The switching frequency is determined according to the efficiency and the power density target. The primary turns number and the core volume are determined to keep the copper and core losses close each other. Thus, the minimum total power loss is provided for the power transformer.

The core loss can be calculated by a Steinmetz equation, which is given as follows:

$$P_{Core-Tr} = K f_s^{\alpha} B_m^{\beta} V.$$
(17)

Where the parameters k, β and α , are found by curve fitting, and V is the volume of the selected core.

The copper losses can be estimated by the use of the high frequency ac resistance of the windings as follows:

$$P_{Cu-Tr} = I_{p-RMS}^{2} R_{ac-pr} + 2I_{s-RMS}^{2} R_{ac-sec}$$
 (18)

Where $R_{ac\text{-}pr}$ and $R_{ac\text{-}sec}$ are the ac resistances of the primary

and the secondary windings, respectively. I_{p-RMS} and I_{s-RMS} are the RMS currents of the primary and secondary windings, respectively.

For optimization of the output inductor, the copper loss has priority when compared to the core loss since the dc component of the output current is larger than the ac component. Therefore, the core loss can be neglected and the copper loss is calculated with the same principle applied to the transformer.

B. Optimization of Semiconductors

The semiconductors are optimized taking into consideration the conduction loss, switching loss and reliability. The high breakdown electric field of SiC allows for a low turn-on resistance when compared to Si devices [24]. The active area where current is flowing is reduced in SiC technology. This results in a decreased device capacitance and operation at high switching frequencies [25]. In addition, SiC technology allows for operation at high temperatures and they are more reliable at a wide range of temperatures [26]. In this paper, SiC power MOSFETs are selected for the primary switches of PSFB converter taking into account the maximum output voltage and current rates. The conduction and switching losses are calculated with the help of parameters from a datasheet. The conduction loss is extracted by:

$$P_{Cond - MOSFET} = I_{MOSFET - RMS}^{2} R_{on - MOSFET}.$$
 (19)

The switching loss is given in detail in following sections.

The rectifier diodes at the secondary side are Schottky diodes providing soft reverse recovery and a low drop voltage. Thus, the reverse recovery loss can be neglected and the conduction loss can be calculated by:

$$P_{Cond-RD} = I_{RD-AVG}^{2} V_{FD}. (20)$$

Where I_{RD-AVG} is the average diode current and V_{FD} is the forward voltage drop of the rectifier diodes at the secondary side.

C. ZVS Optimization for Lagging Leg MOSFETS Based on a Wide Range Output Voltage

This section discusses the dead time optimization to provide ZVS turn-on of the lagging leg MOSFETs for wide range output voltage regulation in the CC mode of a battery charge application. The performance of the PSFB converter is evaluated while the output voltage varies in the CC mode. In the performance analysis of the PSFB converter, it is assumed that 14 Lithium-ion battery cell are connected in series. According to the charge characteristic of the Lithium-ion battery cell given in [10], several charge voltages are selected during the constant current mode between 3.1 V and 3.85 V. Thus, the output range of the converter is obtained as 43.4 V-53.9 V with 14 x (3.1 V-3.85 V).

According to the charge characteristic of the Lithium-ion battery cell, the output voltage is regulated with a constant current. Therefore, the soft switching performance of the PSFB converter should be evaluated in the CCM operation with a full load. The wide range output voltage regulation of the PSFB converter is controlled with a dead time change in the CCM operation.

In the ZVS turn-on of the leading leg switches, the dead time should be enough to allow for the discharge of the parasitic capacitors. Once the dead time is set for the maximum output battery voltage, it is always enough during the regulation of the lower output voltage range obtained with an extended dead time. The dead time of the leading leg for the maximum output battery voltage can be defined based on (3) as:

$$t_{dead-lead} > 79.48 \, ns \,. \tag{21}$$

The dead time should also be larger than the sum of the turn-off delay time t_{d-off} and falling time of the current t_f , which are obtained from semiconductor's datasheet. Thus, the dead time can also be defined as:

$$t_{dead-lead} \ge 42 \, ns$$
 . (22)

The dead time requirement of the lagging leg switches is different from the lagging leg switches. The required dead time should be large enough to allow for the discharge of the parasitic capacitor of the lagging leg switches. However, it should not be large enough to allow for a direction change of the primary current. Thus, the dead time for the lagging leg switches can be calculated based on (10) as:

$$101 ns < t_{dead-lagg} < 257 ns$$
 (23)

In the calculation results given above, the parasitic capacitors are obtained from the semiconductor's data sheet as 80 pF, and L_s is selected as 16 μ H. In the selection of L_s , the output voltage regulation of the converter and the soft switching range are taken into consideration.

The time interval t_{po} is the limitation factor for the selection of L_s , which adjusts the soft switching range over a wide output voltage range. The extension of t_{p0} increases the soft switching range of the primary switches while it limits the output voltage regulation.

Fig. 4 gives the variation of t_{p0} as a function of L_s in the CCM. If the turns ratio of the power transformer is selected as 6.5, the maximum value of L_s is limited with 26 μ H to achieve the desired output voltage regulation. A further extension of L_s can delay t_{p0} but cannot provide output voltage regulation. A transformer with less of a turns ratio provides a greater extension of t_{p0} but this also increases the conduction losses at the primary and secondary side of the converter. The dead time according to output voltage range is summarized in Table 1. According to the obtained results, the primary switches are turned-on with ZVS between 48 V and 54 V with a 26 μ H value of L_s . As shown in Fig. 4, the primary current falls to zero in 257 ns and the ZVS time interval is 101 ns with a 26 μ H value of L_s . These results

TABLE I
SWITCHING OPERATION OF THE LAGGING LEG MOSFETS BASED
ON A WIDE RANGE OUTPUT VOLTAGE

I_o =15 A, V_{in} =385 V, L_s =26 μH, C_{Q2} = C_{Q3} =80 pF, n=6.5			
V_o	$t_{dead ext{-}lagg}$	$D_{\it eff}$	Turn-on Sw.
42	364 ns>t _{p0}	0.71	Hard
44	$322 \text{ ns} > t_{p0}$	0.74	Hard
46	$279 \text{ ns} > t_{p0}$	0.78	Hard
48	$237 \text{ ns} > t_{p0}$	0.81	ZVS
50	$195 \text{ ns} < t_{p0}$	0.84	ZVS
52	$153 \text{ ns} < t_{p0}$	0.88	ZVS
54	$110 \text{ ns} < t_{p0}$	0.91	ZVS

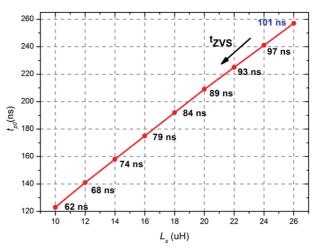


Fig. 4. Change of t_{p0} based on the variation of L_s .

provide the dead time requirement of the lagging leg switches, given in (23).

D. ZVS Optimization of Lagging Leg MOSFETS Based on the Wide Range Output Load Condition

In this section, the CV mode of battery charge applications is evaluated in terms of high efficiency. When the battery voltage reaches its maximum value, it starts to charge with the CV mode. In this mode, the PSFB converter works with a constant voltage and a decreasing load current. The soft switching turn-on operation of the lagging leg switches depends on the load condition and it can decay under a light battery current. The DCM operation is a simple and effective way to reduce the switching losses of the PSFB converter under a light load condition. However, the boundary between the CCM and DCM is important to reach a high efficiency. Therefore, this section discusses the boundary between the CCM and the DCM.

The switching losses of the PSFB converter are compared for the CCM and the CCM+DCM operations and the obtained results are given in Fig. 5.

In the calculation, the turn-on switching loss of the leading switches is neglected due to the ZVS turn-on process. The turn-off switching losses for the leading and lagging leg

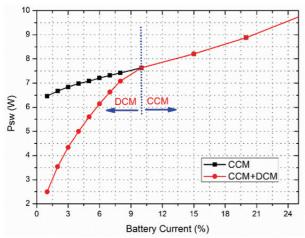


Fig. 5. Switching loss comparison of the PSFB converter for the CCM and the CCM+DCM operations.

switches in the CCM operation can be obtained by:

$$P_{sw-off-lead} = \frac{1}{2} V_{in} I_{pp} t_f f_{sw}. \tag{24}$$

In the calculations, it is accepted that the switches of each leg are turned off under I_{pp} . In the CCM, the ZVS turn-on operation of the lagging leg switches is lost under certain load conditions and switching loss occurs. In this situation, the turn-on switching loss can be calculated by:

$$P_{sw-on-lead} = \frac{1}{2} (C_{Q1} + C_{Q4}) V_r^2 f_{sw}.$$
 (25)

Where V_r is the remaining voltage across the parasitic capacitor of the leading leg switches. This voltage varies according to the load condition of the battery, and it can be defined as:

$$V_r = V_{in} - \sqrt{\frac{L_s}{C_{Q1} + C_{Q4}}} I_{p2-CCM} . {26}$$

In the DCM operation, the turn-off switching losses are calculated with same approach given for the CCM operation. There are no turn-on switching losses in the DCM operation. Therefore, the switching losses are decreased under a 10% load condition with the DCM operation.

In the DCM operation, the core and conduction losses should be taken into consideration to determine the operation boundary. The conduction loss increases with high ripples while the core and switching losses are reduced in the DCM operation. Here, the core loss represents the transformer core loss since the output inductor core loss in the very light load conditions is insignificant in the total power loss. Fig. 6 provides the efficiency change of the converter in the CCM, and in CCM and DCM operations. The reducing core loss and switching loss in the DCM operation keep the efficiency high at under 12% of the load current when compared to the CCM operation. This result shows that reducing the core and switching losses is more dominant when compared to

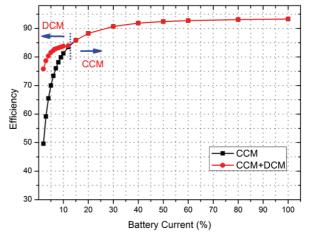


Fig. 6. Efficiency comparison of the PSFB converter in the CCM and DCM operations.

increased conduction loss in the DCM operation. Therefore, the DCM operation boundary can be determined as 12% of the battery current to reach high efficiency.

IV. MEASUREMENT RESULTS

The obtained theoretical results of the proposed design optimization are verified with a prototype designed for the second stage of an on-board EV battery charger. The prototype is fed from a DC power supply with 385 V DC. A DC electronic load is used to simulate the battery charge profile. The prototype is operated at a 200 kHz switching frequency with 42 V-54 V /15 A. In the design of the prototype, the following steps have been implemented.

Step 1: Magnetic Components: The power transformer is built with a 12:2 turns ratio and copper foils on an E65/32/27 core taking into consideration the output voltage regulation, copper loss and core loss. Thus, the maximum magnetic flux is obtained between 0.05-0.07 Tesla for a 42-54 V output voltage range when f_s is 200 kHz and V_{in} is 385 V.

The series connected inductor to the primary side of the transformer is built with a 26 μ H inductance value based on the ZVS turn-on of the lagging leg switches with a wide range output voltage regulation as analyzed in part III. C.

The output inductor is built with multiple Litz wires on a cut leg U core at 1.1 μ H. A UU-120B cut legs core is used with 2 turns. The magnetic flux density variation changes between 0.0066 Tesla–0.02 Tesla while the output voltage changes between 42 V–54 V in the CC operation mode of the battery charge. These magnetic flux density variation values create very low core losses in the CCM. The DCM operation is applied under a 12 % load condition in the CV mode and the magnetic flux density variation is quite low when compared to the CCM. Therefore, it can be neglected.

Step 2: Power Semiconductors: C2M0080120 SiC MOSFETs are used for the primary switches taking into consideration the advantages of SiC technologies mentioned

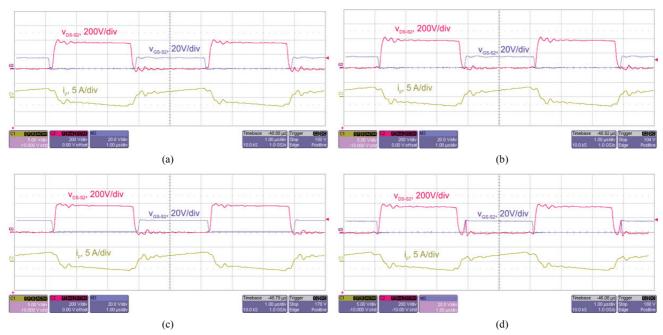


Fig. 7. Measured voltage of the S₂ MOSFET (v_{DS-S2}) and the primary current at: (a) V_o =54 V; (b) V_o =50 V; (c) V_o =48; (d) V_o =42 V (I_o =15 A, f_s =200 kHz and V_{in} =385 V).

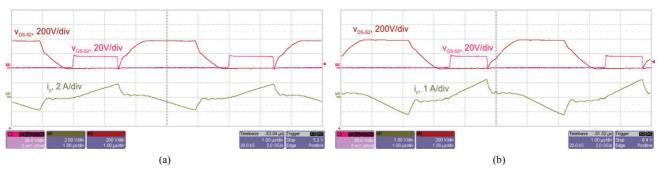


Fig. 8. Measured voltage of the S₂ MOSFET (v_{DS-S2}) and the primary current (i_p) with: (a) 10% load; (b) 5% load (V_o =54 V, f_s =200 kHz and V_{in} =385 V).

in part III. DSS2x101-015A Schottky diodes are used to produce DC output voltage at the secondary side.

Step 3: Operation Points: According to the battery charge characteristic of the Lithium-ion battery cell, the PSFB converter is operated in the CCM for the CC battery charge mode and in the CCM+DCM for the CV battery charge mode. In the CV mode, the DCM operation is applied under a %12 load condition to reach a high efficiency over a wide load range. For this purpose, the effective duty ratio $D_{\rm DCM}$ is determined as 0.57 and 0.43 for 10% and 5% load conditions, respectively. Thus, the dead time is determined to be approximately 1 μs and 1.32 μs for 10% and 5% load conditions.

A prototype has been built according to the procedure given above. Firstly, the soft switching performance of the lagging leg switches at the primary side is tested for a wide range output voltage in the CC mode. Fig. 7 shows the measured voltage of S_2 MOSFET and primary current

waveforms while the battery voltages are 54 V, 50 V, 48 V and 42 V with a constant battery current. The measured waveforms, given in Fig. 7 (a), (b) and (c), validate the ZVS turn-on process of the lagging leg switches between 54 V and 48 V. However, the ZVS turn-on process is not achieved below 48 V, as shown in Fig. 7 (d), since the primary current falls to zero before the dead time is completed and charges the parasitic capacitor again as anticipated in the theoretical analysis.

To evaluate the ZVS turn-on performance of the lagging leg in the CV battery charge mode, the voltage of the S_2 MOSFET and the primary current are measured between 5% and 10% load conditions in the DCM operation. The measured results are given in Fig. 8.

The efficiency of the second stage of the PSFB converter is measured for wide voltage and current ranges. The measured efficiency values are shown in the graphic given in Figure 9. Fig. 9(a) shows the efficiency values for a wide output voltage

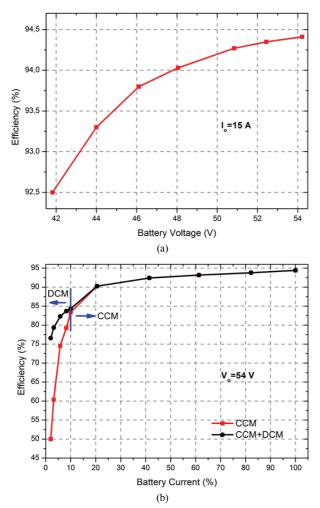


Fig. 9. Measured efficiency values: (a) Based on wide range battery voltage conditions, CC mode; (b) Based on wide range battery current conditions, CV mode.

range. The maximum efficiency is measured at a 54 V battery voltage as 94.4%. Fig. 9(b) gives the measured results for a wide range battery current. Applying the DCM operation under a 12% load increases the efficiency when compared to the CCM operation. The efficiency is measured as 76.6% at a 2% load.

V. CONCLUSIONS

In this paper, the design optimization of a second stage PSFB converter for on-board EV battery chargers is proposed. In the design procedure, a wide range battery voltage and a wide range battery current are taken into consideration to reach a high efficiency in most of the Lithium-ion battery charge profile. The soft switching operation of the primary switches of the PSFB converter is analyzed based on wide range voltage and current conditions. In the theoretical analysis, the converter is optimized to operate with soft switching from a 48 to 54 V output voltage in the CC battery charge mode. In the CV mode, the DCM operation is applied

below a 12% load to maintain the soft switching operation of the primary switches. Finally, a prototype is built to validate the obtained theoretical results. The prototype is built to operate with a 42-54 V/15 A output at a 200 kHz switching frequency. The efficiency of the proposed converter design is measured as 94.4% at a 54V/15A output and as 76.6% at a 54V/0.3 A output.

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