

# Voltage-Fed Push-Pull PWM Converter Featuring Wide ZVS Range and Low Circulating Loss with Simple Auxiliary Circuit

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## Abstract

A new zero-voltage-switching (ZVS) push-pull pulse-width modulation (PWM) converter is proposed in this paper. The wide ZVS condition for all of the switches is obtained by utilizing the energy stored in the output inductor and magnetizing inductance. As a result, the switching losses can be dramatically reduced. A simple auxiliary circuit including two small diodes and one capacitor is added at the secondary side of a high frequency (HF) transformer to reset the primary current during the circulating stage and to clamp the voltage spike across the rectifier diodes, which enables the use of low-voltage and low-cost diodes to reduce the conducting and reverse recovery losses. In addition, there are no active devices or resistors in the auxiliary circuit, which can be realized easily. A detailed steady operation analysis, characteristics, design considerations, experimental results and a loss breakdown are presented for the proposed converter. A 500 W prototype has been constructed to verify the effectiveness of the proposed concept.

**Key words:** Push-pull, Simple auxiliary circuit, Voltage-fed, Zero-voltage-switching

## I. INTRODUCTION

In medium-small power and low-input-voltage applications such as battery chargers, uninterruptible power supply (UPS), electric vehicles and distributed renewable energy systems i.e., fuel cells, solar cells and wind turbines, a high voltage step-up dc/dc converter is generally required to serve as an interface between a low-voltage source and a high-voltage bus (200-400V) [1]-[4]. Usually, a push-pull converter is the preferred choice due to its simple circuitry, high-voltage conversion ratio, electric isolation and good transformer utilization. However, conventional push-pull converters, including voltage-fed and current-fed converters, suffer from the drawbacks of hard-switching and high-voltage overshoots across the primary switches and secondary diodes due to the resonance between the leakage inductance of the HF transformer and the junction capacitors during the turn-off transient, which results in high switching losses and large

voltage rating components [5]. In particular, when the switching frequency becomes higher, these limitations become more serious. To solve these problems, a number of zero-voltage and zero-current switching (ZVZCS) push-pull converters have been proposed during the past several years [5]-[18], [21], [22]. These topologies can be categorized according to their modulation strategy as either variable frequency modulation (VFM) [6]-[12] or pulse-width modulation (PWM) strategies [5], [13]-[20].

The VFM is mainly adopted in resonant converters to realize the ZVZCS operation of switches and to maintain the regulation of the output voltage. In [6]-[9], LCL, LLC and LC resonant-tanks are added in the secondary of voltage-fed push-pull converters to assist in ZVS or ZCS for the primary switches. In addition, the leakage inductance of the HF transformer and parasitic capacitance of the device can be utilized to achieve soft-switching. However, the resonant current is much higher than the input current, which leads to the need for higher current-stress devices. In addition, the resonant-tank was implemented in current-fed push-pull converters and the ZVZCS was achieved in the same manner as that of the voltage-fed type. The topology in [10] can achieve ZVS turn-on for the primary switches and ZCS

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turn-off for the rectifier diode. However, the duty cycle has to be fixed at 0.5. In [11], Primary switches operate under ZCS turn-off whereas the rectifier diodes operate under hard turn-off. A simple and cost-effective method of paralleling one capacitor in the secondary winding of the HF transformer has been proposed in [12]. This is done to assist in ZCS turn-off of the primary switches and to clamp the winding voltage-spike. However, it still uses hard switching turn-on.

It should be noted that VFM makes the magnetic design and control strategy more complex and challenging while the PWM converters can eliminate these drawbacks. Therefore, many PWM push-pull converters have been proposed in recent years. PWM current-fed push-pull converters with one or two active-clamp circuits have been presented in [13], [14] to suppress the voltage surge, and to support ZVS turn-on. However, current-fed topologies usually require a larger input inductor, higher voltage rating switch, additional snubbers and an auxiliary soft-start circuit when compared with voltage-fed structures [13], [15], [16]. Therefore, it is not a preferred candidate in some applications. On the other hand, the voltage-fed type does not have these limitations. In view of the aforementioned shortcomings, in [17], [18], two complicated snubbers are paralleled with primary switches to suppress the voltage spike and to recycle the leakage inductance energy. However, the switches still operate under hard-switching. Voltage-fed push-pull converters with active-clamp circuits have been discussed in [19], [20], where all of the switches can realize ZVS turn-on and suppress the voltage spike. However, the ZVS condition is determined by the leakage inductance. Therefore, the switches lose the ZVS condition easily under a certain light load. Another attractive approach has been presented in [21], where only one switch is inserted between the input voltage source and the middle point of the HF transformer in the two primary windings. This structure possesses characteristics similar to those of the phase-shift full bridge topology. All of the switches can realize ZVS operation with the PWM control. However, a narrow ZVS range and a rectifier voltage ringing are two key problems. Therefore, one saturable inductance is implemented to suppress the voltage spike and to widen the ZVS range in [22]. However, this topology still loses ZVS operation until half-load. More importantly, the large circulating primary current increases the conduction loss and reduces the conversion efficiency.

Considering these problems, this paper proposes a new voltage-fed push-pull converter that features an extended ZVS load range, lower circulating losses and a lower voltage spike. The primary switches can achieve ZVS operation over a wide load range by the energy stored in the magnetizing inductance and output filter. A simple auxiliary circuit including two diodes and one capacitor in the secondary can reset the primary current to  $I_{Lm}/2$  ( $I_{Lm}$  is the maximum value of the magnetizing current) during the circulation stage. It can

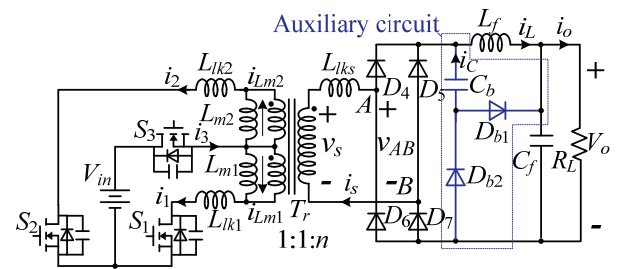


Fig. 1. Circuit configuration of the proposed converter.

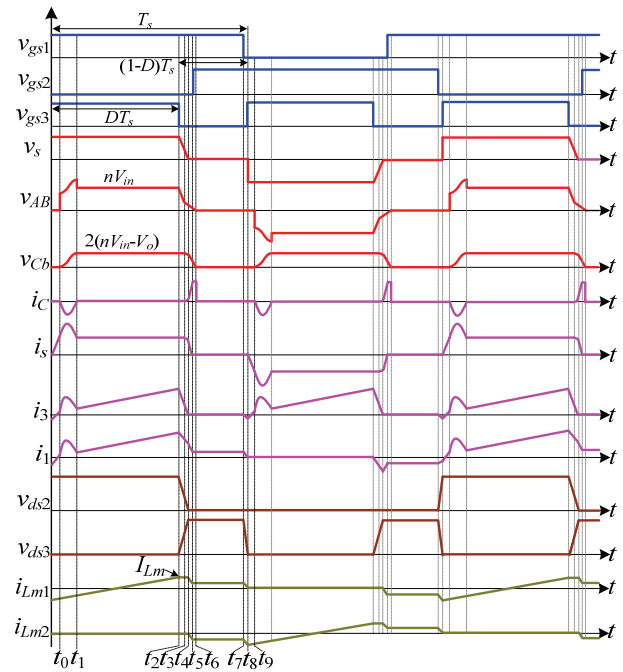


Fig. 2. Typical steady-state waveforms of the proposed converter.

also assist in clamping the rectifier diodes voltage. The operation, characteristics, design considerations, a performance comparison and a loss breakdown are illustrated. A 500 W 100 kHz prototype has been implemented and tested to verify the proposed concept.

This paper is organized as follows. Section II shows a diagram of the proposed converter and its steady-state operation. In Section III, the key characteristics and design considerations are discussed. Experimental results are presented in Section IV. Section V gives some conclusions.

## II. CIRCUIT DESCRIPTION AND STEADY-STATE OPERATION

Fig. 1 shows the circuit configuration of the proposed voltage-fed push-pull converter, where  $T_r$  is the HF transformer with a turns ratio of 1:1:  $n$ , which consists of the leakage inductances  $L_{lk1}$ ,  $L_{lk2}$  and  $L_{lks}$  and the magnetizing inductances  $L_{m1}$  and  $L_{m2}$ . The input source  $V_{in}$  is linked to two primary windings through the switches  $S_1$ ,  $S_2$  and  $S_3$ . The secondary side circuit is made up of a full bridge rectifier; a

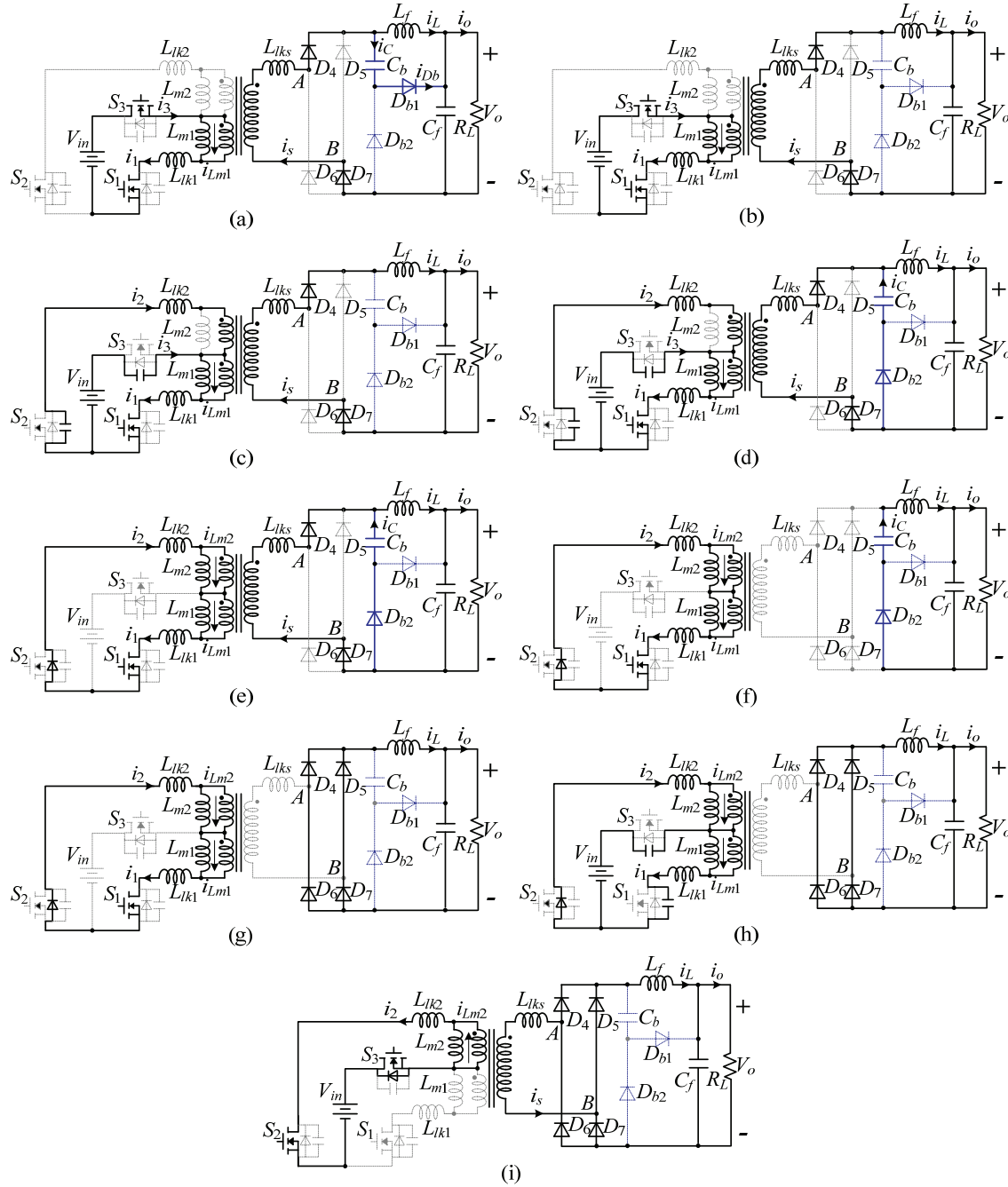


Fig. 3. Equivalent circuits for each of the intervals: (a) Interval 1 ( $t_0-t_1$ ); (b) Interval 2 ( $t_1-t_2$ ); (c) Interval 3 ( $t_2-t_3$ ); (d) Interval 4 ( $t_3-t_4$ ); (e) Interval 5 ( $t_4-t_5$ ); (f) Interval 6 ( $t_5-t_6$ ); (g) Interval 7 ( $t_6-t_7$ ); (h) Interval 8 ( $t_7-t_8$ ); (i) Interval 9 ( $t_8-t_9$ ).

simple auxiliary circuit consisting of one clamping capacitor  $C_b$  and two diodes  $D_{b1}$  and  $D_{b2}$ ; an LC filter and a load. Note that three switches are driven by the gate signals adopted in [22]. In addition, dead time is inserted between the gate signals to achieve ZVS operation.

Before analyzing the steady-state operation of the proposed converter, some assumptions are made to simplify the explanation.

1) The switches  $S_1\sim S_3$  are ideal MOSFETs with antiparallel body diodes  $D_1\sim D_3$  and capacitors  $C_1\sim C_3$ , and the diodes

$D_4\sim D_7$  are ideal devices.

2) The capacitance of  $C_f$  is large enough. Therefore, the voltage across it can be seen as a constant during the switching process.

3)  $C_1=C_2=C_3$ ,  $L_{k1}=L_{k2}=L_{ks}/n^2=L_{lk}$  and  $L_{m1}=L_{m2}=L_m$ .

Based on the above assumptions, Fig. 2 illustrates typical steady-state waveforms of the proposed converter. During one complete switching period of  $S_3$ , the operation principle can be divided into nine intervals. The corresponding equivalent circuits of all the different intervals are shown in Fig. 3.

**Interval 1** [ $t_0 \leq t < t_1$ , Fig. 3(a)]:  $S_1$  and  $S_3$  are conducting and the secondary current  $i_s$  reaches  $I_o$ . At the same time, the voltage  $v_{AB}$  increases to  $V_o$ . The diode  $D_{b1}$  starts turn-on and the clamping capacitor  $C_b$  is charged through  $D_{b1}$  and  $C_f$  via the resonance between  $L_{lks}$  and  $C_b$ . Then,  $v_{AB}$  continues increasing from  $V_o$ , and  $v_{Cb}$  begin rising from 0. The primary currents  $i_1$  and  $i_3$  rise along with an increase of the current  $i_s$  and the magnetizing current  $i_{Lm1}$ . In addition, the magnetizing current can be viewed as rising linearly. Equations during this process can be obtained by solving the equivalent circuit in Fig. 3(a). In addition, the voltage across  $C_b$ , i.e.  $v_{Cb}$ , the current through  $C_b$  i.e.  $i_C$ , the primary switches currents  $i_1 \sim i_3$  and the magnetizing current  $i_{Lm1}$  can be expressed as:

$$v_{Cb}(t) = (nV_{in} - V_o)[1 - \cos(\omega_{r0}t)] - I_o Z_{r0} \sin(\omega_{r0}t) \quad (1)$$

$$i_C(t) = \frac{nV_{in} - V_o}{Z_{r0}} \sin(\omega_{r0}t) - I_o [1 - \cos(\omega_{r0}t)] \quad (2)$$

$$i_s(t) = I_o - i_C(t) \quad (3)$$

$$i_1(t) = i_3(t) = n[I_o - i_C(t)] + i_{Lm1}(t) \quad (4)$$

$$i_{Lm1}(t) = i_{Lm1}(t_0) + (V_{in} \cdot t) / L_m \quad (5)$$

where  $\omega_{r0}$  and  $Z_{r0}$  represent the resonant angular frequency and the resonant impedance, which are given by:

$$\omega_{r0} = 1 / \sqrt{L_{lks} C_b}, Z_{r0} = \sqrt{L_{lks} / C_b} \quad (6)$$

In this interval, the power is transferred from the input source to the output. At  $t=t_1$ , the current through  $C_b$  reaches 0,  $v_{Cb}$  goes up to its peak value  $2(nV_{in} - V_o)$ , and this stage ends.

**Interval 2** [ $t_1 \leq t < t_2$ , Fig. 3(b)]: At  $t_1$ ,  $D_{b1}$  is turned off and the voltage  $v_{AB}$  is returned to  $nV_{in}$ . In addition,  $v_{Cb}$  maintains its peak value until the next interval. Power is still transferred from the input to the load during this interval.

**Interval 3** [ $t_2 \leq t < t_3$ , Fig. 3(c)]: At  $t_2$ ,  $S_3$  is turned off (ZVS due to  $C_3$ ) and the current through the primary starts charging the antiparallel capacitor  $C_3$  of  $S_3$  and discharging that of  $S_2$ . To maintain the HF transformer flux-balance, the voltage across  $S_3$  and  $S_2$  can be considered as linearly charged and discharged because both the filter inductor and the magnetizing inductance are large enough. They are given by:

$$v_{ds3}(t) = (nI_o + I_{Lm}) \cdot t / (C_2 + C_3) \quad (7)$$

$$v_{ds2}(t) = 2V_{in} - (nI_o + I_{Lm}) \cdot t / (C_2 + C_3) \quad (8)$$

where  $v_{ds3}$  and  $v_{ds2}$  are the voltages across the switches  $S_3$  and  $S_2$ , respectively.

During this interval, the primary winding voltage and the secondary rectifier voltage are also declined in accordance with the variations of  $v_{ds3}$  and  $v_{ds2}$ . In addition, the decreasing of  $i_3$  leads to the reverse increasing of  $i_2$  to remain  $nI_o + I_{Lm}$  constant.

**Interval 4** [ $t_3 \leq t < t_4$ , Fig. 3(d)]: When the rectifier voltage  $v_{AB}$  decreases to the value of  $V_{Cb}$ , the diode  $D_{b2}$  begins conducting and the capacitor  $C_b$  holds the rectifier voltage  $v_{AB}$ .

This implies that the rectifier voltage falls down much slower than the primary winding voltage. The difference voltage  $v_s - v_{AB}$  is applied to the secondary leakage inductance  $L_{lks}$ , and the secondary current  $i_s$  starts going down from  $I_o$ . Accordingly, the variation of the voltage  $v_{Cb}$ ,  $v_s$  and the secondary current  $i_s$  can be derived as:

$$v_{Cb}(t) = V_{Cb} - \frac{I_o C_{eq}}{C_b(C_b + C_{eq})} \omega_{r1} \sin(\omega_{r1}t) + \frac{I_o C_{eq}}{C_b(C_b + C_{eq})} t \quad (9)$$

$$i_s(t) = I_o \left(1 - \frac{C_{eq}}{C_b + C_{eq}}\right) \cos(\omega_{r1}t) + \frac{I_o C_{eq}}{C_b(C_b + C_{eq})} \quad (10)$$

$$v_s(t) = V_{Cb} + \frac{I_o}{\omega_{r1}} \left(\frac{1}{C_b + C_{eq}} - \frac{1}{C_{eq}}\right) \sin(\omega_{r1}t) - \frac{I_o}{C_b + C_{eq}} t \quad (11)$$

where  $\omega_{r1}$  and  $C_{eq}$  represent the resonant angular frequency and the equivalent capacitance in this stage, and are calculated as:

$$\begin{cases} \omega_{r1} = \sqrt{(C_b + C_{eq}) / (L_{lks} C_b C_{eq})} \\ C_{eq} = (C_2 + C_3) / n^2 \end{cases} \quad (12)$$

At  $t_4$ , the primary winding voltage reaches 0. At the same time, the voltage across  $S_2$  also decreases to 0 and  $D_2$  conducts providing ZVS turn-on for  $S_2$ . The secondary current  $i_s$  and the rectifier voltage  $v_{AB}$  reach  $i_s(t_4)$  and  $v_{Cb}(t_4)$ , and this interval ends.

**Interval 5** [ $t_4 \leq t < t_5$ , Fig. 3(e)]: After  $t_4$ ,  $D_2$  and  $S_1$  are conducting and the winding voltage is maintained at 0. Therefore,  $v_{Cb}$  is applied to the leakage inductance  $L_{lks}$ , and the secondary current falls down very fast. The secondary current  $i_s$  and the voltage  $v_{Cb}$  can be calculated as:

$$v_{Cb}(t) = [i_s(t_4) - I_o] Z_{r0} \sin(\omega_{r0}t) + v_{Cb}(t_4) \cos(\omega_{r0}t) \quad (13)$$

$$i_s(t) = I_o + [i_s(t_4) - I_o] \cos(\omega_{r0}t) + \frac{v_{Cb}(t_4)}{Z_{r0}} \sin(\omega_{r0}t) \quad (14)$$

During this stage, note that the currents  $i_1$  and  $i_2$  fall down along with the decreasing of the current  $i_s$ . When  $i_1$  goes down to  $I_{Lm}$ , the magnetizing current is provided by two windings commonly. Later on,  $i_{Lm1}$  descends from  $I_{Lm}$  to  $I_{Lm}/2$ , and  $i_{Lm2}$  ascends from zero to  $-I_{Lm}/2$ . This interval finishes when  $i_s$  reaches zero.

**Interval 6** [ $t_5 \leq t < t_6$ , Fig. 3(f)]: At  $t_5$ , the secondary current  $i_s$  is 0 and the primary current resets to the magnetizing current. This implies that there remains a small magnetizing current during the next circulating interval. Then the energy stored in  $C_b$  supplies the load, and the voltage  $v_{Cb}$  drops quickly. This can be expressed by:

$$v_{Cb}(t) = v_{Cb}(t_5) - I_o \cdot t / C_b \quad (15)$$

**Interval 7** [ $t_6 \leq t < t_7$ , Fig. 3(g)]: This interval begins when  $C_b$  discharges completely. All of the rectifier diodes start to turn on and the load current commutates through the rectifier. In addition, the primary operates at the circulating stage with the half magnetizing current  $I_{Lm}/2$ .

**Interval 8** [ $t_7 \leq t < t_8$ , Fig. 3(h)]: At  $t_7$ ,  $S_1$  is turned off (ZVS due to  $C_1$ ), and the turn-off current is  $I_{Lm}/2$ . The turn-off loss is small since only  $I_{Lm}/2$  remains through the devices. Then  $I_{Lm}/2$  starts discharging and charging  $C_3$  and  $C_1$ , respectively. This means the voltage across  $S_3$  falls from  $V_{in}$ , and the voltage across  $S_1$  increases from 0. If the energy stored magnetizing inductance is large enough,  $v_{ds3}$  decreases to 0 quickly providing the ZVS turn-on condition for  $S_3$ .

During this interval, the secondary state is the same as that of interval 7, and the energy stored in  $L_f$  and  $C_f$  offers the load current.

**Interval 9** [ $t_8 \leq t < t_9$ , Fig. 3(i)]: At  $t_8$ ,  $S_3$  is turned on with ZVS. Then  $V_{in}$  is applied to the leakage inductance  $L_{lk2}$ . The current  $i_2$  increases quickly and when it is larger than  $I_{Lm}$ , the secondary current  $i_s$  starts flowing through the secondary winding reversely. The diodes  $D_4 \sim D_7$  conduct commonly to deliver power until  $i_s$  increases to  $I_o$ . Subsequently, the next cycle starts.

### III. CHARACTERISTICS AND DESIGN CONSIDERATIONS

#### A. Steady State Analysis

From the aforementioned description, the steady state features of the proposed converter can be derived in this section. Fig. 4 shows simplified operating waveforms in the secondary. The steady-state dc voltage gain of the converter by the flux balance of the filter inductor during the whole switching period can be derived as:

$$\frac{V_o}{V_{in}} = \frac{D - d_1 + d_2}{1 - d_1 + d_2} \cdot n \quad (16)$$

where  $D$  is the duty ratio of  $S_3$ , and  $d_1$  and  $d_2$  represents two delay stages.

**Delay stage  $d_1$ :** By the analysis in interval 9, the duration time of this process is such that the input voltage is applied to the leakage inductance and the secondary current  $i_s$  increases to  $I_o$ . Therefore, it can be expressed by:

$$d_1 = \frac{\Delta t_1}{T_s} = \frac{f_s L_{lk2} I_o}{n V_{in}} \quad (17)$$

**Delay stage  $d_2$ :** In this interval, the secondary voltage  $v_{AB}$  decreases to zero due to the discharging process of  $C_b$ . Thus,  $d_2$  can be approximately obtained by:

$$d_2 = \frac{\Delta t_2}{T_s} = \frac{(n V_{in} - V_o) C_b f_s}{I_o} \quad (18)$$

By (16)-(18), the steady-state voltage gain can be further obtained. Taking the following prototype as an example, Fig. 5 shows a comparison of the voltage gain between the proposed converter and the topology presented in [22] under the same specifications. Obviously, it has a higher voltage gain than the concept in [22].

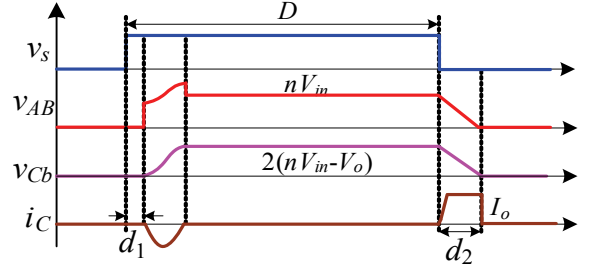


Fig. 4. Simplified waveforms in the secondary.

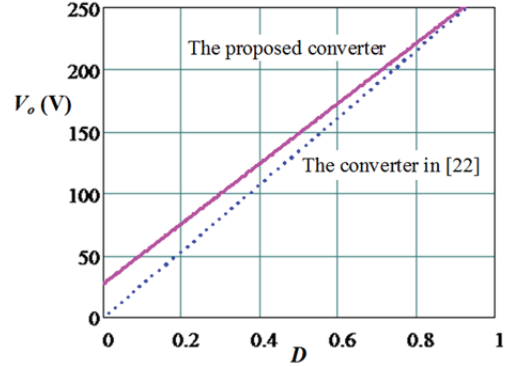


Fig. 5. Comparison of the steady state voltage gain with that of the topology in [22].

#### B. Soft-Switching for Devices

**For  $S_1$  ( $S_2$ ):** According to the description of intervals 3 and 4, the switches  $S_1$  ( $S_2$ ) realize ZVS turn-on by utilizing the energy stored in the output inductor  $L_f$  and the magnetizing inductance to discharge  $C_1$  ( $C_2$ ) and charge  $C_3$ . Therefore, from the energy perspective, the ZVS condition of  $S_1$  ( $S_2$ ) can be expressed by:

$$L_m (I_{Lm})^2 + (L_f / n^2) (n I_o)^2 \geq C (2V_{in})^2 + C (V_{in})^2 \quad (19)$$

The required dead time  $t_{d1}$  can be obtained by:

$$t_{d1} \geq (4V_{in} C) / (n I_o + I_{Lm}) \quad (20)$$

**For  $S_3$ :** From the explanation of interval 8, the ZVS operation of  $S_3$  is only determined by the charging and discharging energy from the magnetizing inductance. This expression is approximately given by:

$$L_m (I_{Lm} / 2)^2 > C (2V_{in})^2 + C (V_{in})^2 \quad (21)$$

In addition, the needed dead time  $t_{d2}$  is:

$$t_{d2} \geq (8V_{in} C) / I_{Lm} \quad (22)$$

From (19)-(22), it can be seen that the ZVS operation for  $S_3$  is more difficult than that for  $S_1$  ( $S_2$ ). It can also be seen that it is only decided by the maximum magnetizing current, which is determined by the input voltage and the conduction time of  $S_3$ . The maximum magnetizing current  $I_{Lm}$  can be approximately derived as:

$$I_{Lm} = \Delta I_{Lm} / 2 = V_{in} D T_s / (2L_m) \quad (23)$$

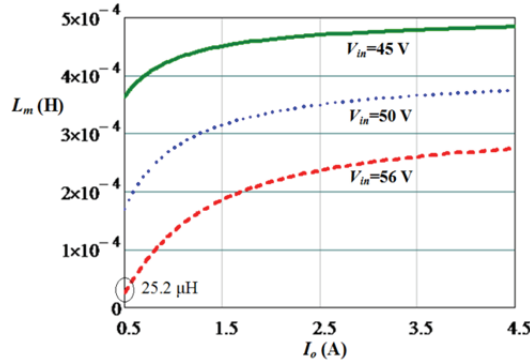


Fig. 6. Plots of the relationships among  $L_m$ ,  $V_{in}$  and  $I_o$ .

Combing (16)-(18), (21) and (23), the magnetizing inductance for achieving the ZVS operation of  $S_1 \sim S_3$  under different values of  $V_{in}$  and load currents  $I_o$  can be determined. Here, by setting the specifications of the following prototype to  $V_{in}=45 \sim 56$  V,  $V_o=200$  V, turns ratio  $n=6$ , switching frequency  $f_s=100$  kHz, etc., the relationship among them is plotted as Fig. 6. Note that all of the switches can achieve ZVS turn-on if the converter works under the curve region. This curve is used to determine that the harshest ZVS operation conditions are with  $V_{in}=56$  V for the following prototype since the duty cycle  $D$  is small. This results in a smaller magnetizing current, which further reduces the energy charging and discharging capacitors  $C_1 \sim C_3$ . From Fig. 6,  $L_m=25.2$   $\mu$ H can be designed to realize ZVS for all of the switches at more than a 20% load when the input voltage is 56 V.

For  $D_4 \sim D_7$ : The diodes  $D_4 \sim D_7$  can be turned off naturally since the secondary current  $i_s$  decreases to zero before the circulating stage, where the secondary winding voltage is zero. Therefore, the reverse-recovery problem of the rectifier diodes can be eliminated in this converter.

### C. Voltage and Current Stress of the Power Devices

Since the clamping capacitor  $C_b$  and the diode  $D_{b1}$  provide a clamping path to the filter capacitor  $C_f$  in this converter, the voltage spikes in the topologies of [19]-[22] caused by parasitic ringing between the leakage inductance and diode junction capacitors are released. The voltage stress of the rectifier diodes  $D_4 \sim D_7$  can be clamped to:

$$V_{rec} = V_o + V_{C_b} = nV_{in}(2-D) \quad (24)$$

Formula (24) illustrates that the voltage stresses on the rectifier diodes are inversely proportional to the duty cycle. Thus, the lower voltage stress of the rectifier diode can be maintained as pushing up the duty cycle  $D_{eff}$ , and this value is the minimal achievable voltage with  $D_{eff}=1$ . In practice, the duty cycle can be selected as high as possible such as 0.8-0.9.

The average current through  $D_4 \sim D_7$  can be calculated by:

$$I_{D4} = I_{D5} = I_{D6} = I_{D7} = P_o / (2V_o) \quad (25)$$

where  $P_o$  represents the rated output power.

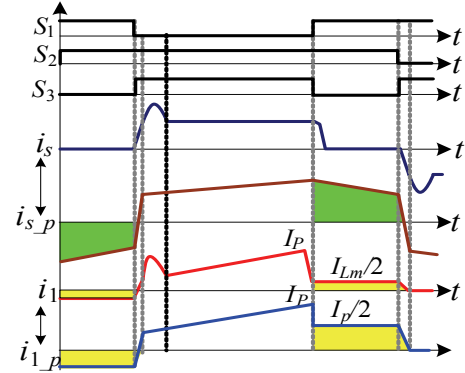


Fig. 7. Comparison of circulating currents with those of a similar converter.

The voltage stresses across  $D_{b1}$  and  $D_{b2}$  are equal to  $V_o$ , and average current through them can be calculated by:

$$\begin{cases} I_{D_{b2}} = d_2 I_o \\ I_{D_{b1}} = f_s \int_0^{d_1 T_s} \left[ \frac{nV_{in} - V_o}{Z_{r0}} \sin(\omega_{r0} t) - I_o (1 - \cos(\omega_{r0} t)) \right] dt \end{cases} \quad (26)$$

Similarly, the voltage stresses across  $S_1$  and  $S_2$  are  $2V_{in}$ , and the stress across  $S_3$  is  $V_{in}$ . The average current through them can be expressed by:

$$\begin{cases} I_{S1} = I_{S2} = nP_o / (2\eta V_o) \\ I_{S3} = nP_o / (\eta V_o) \end{cases} \quad (27)$$

where  $\eta$  and  $P_o$  represent the conversion efficiency and output rated power.

### D. Selection of the Clamping Capacitor $C_b$

To ensure that both the primary current and the secondary current are reset during the conduction intervals 4 and 5, the discharge time of the energy stored in the clamping capacitor  $C_b$  should be larger than that of the energy stored in the secondary leakage inductance  $L_{lks}$ . Thus, the clamping capacitor  $C_b$  can be designed as:

$$C_b > L_{lks} \cdot I_o^2 / [2(nV_{in} - V_o)]^2 \quad (28)$$

### E. Reduced Circulating Loss

Simplified primary and secondary waveforms of the proposed converter are compared to those of the topologies in [21], [22] in Fig. 7, where  $i_s$  and  $i_1$  are the currents through the secondary winding and the switch  $S_1$  in the proposed converter, and  $i_{s_p}$  and  $i_{1_p}$  represent those in [21]-[22]. It can be seen that only a small magnetizing current flows through the primary side and that the secondary current  $i_s$  remains zero during the circulating interval. Therefore, the conduction loss during this stage can be minimized, which results in a higher efficiency when compared with the previous ones.

### F. Performance Comparison

The proposed converter is an improved version of the converters presented in [21], [22]. However, their performances

TABLE I  
SPECIFICATIONS OF THE PROTOTYPE

Names	Parameters
Input voltage	45–56V DC
Output voltage	200 V DC
Switching frequency	100 kHz
Output rated power	500 W
Switches: $S_1 \sim S_3$	IRFP260N. (External shunt capacitance: 1nF)
HF Transformer	EE55/ PC40; Turn ratio: $N_{P1}:N_{P2}:N_s = 5:5:30$
Secondary diodes: $D_4 \sim D_7$	MUR860
Clamping diodes: $D_{b1}, D_{b2}$	MUR840
Clamping capacitor $C_b$	27 nF film capacitor
Output inductor $L_f$	500 $\mu$ H
Output capacitance $C_o$	470*2 $\mu$ F

and working principles are quite different. The proposed converter can realize a higher voltage gain and ZVS operation for all of the switches in a wider load range. The rectifier voltage ringing can be eliminated and more conduction loss during the circulating stage can be reduced through the secondary simple auxiliary circuit. More importantly, there are no active devices or resistors in the auxiliary circuit, which can be realized easily.

#### IV. EXPERIMENTAL RESULTS

A 500 W prototype has been built and tested in the laboratory to verify the analysis and performance of the proposed converter. The prototype is controlled by a DSP TMS320F2812 digital signal processor. The detailed specifications are listed in Table I.

From equations (16)–(18) and Fig. 5, taking the required dead time and the delay characteristics into account, the maximum duty cycle can be selected as 0.8 to keep enough voltage gain. The voltage stress on the rectifier diode can be calculated as 324V by (24). According to Fig. 6, the magnetizing inductance can be designed as 25  $\mu$ H under the specified input voltage to ensure the realization of ZVS turn-on for all of the switches at more than a 20% load. The leakage inductance of the HF transformer  $L_{lks}$  has been measured at about 2.6  $\mu$ H. In addition, by (28), the clamping capacitor can be shown to be larger than 14 nF. In the prototype,  $C_b$  was selected as 27 nF.

Experimental results of the prototype under different input voltage and load conditions are shown in Fig. 8 and Fig. 9, respectively. Fig. 8 shows typical waveforms for  $V_{in}=45$  V at a full load, and Fig. 9 shows them for  $V_{in}=56$  V at a 20% load (100W). It can be seen that the experimental waveforms match closely with those shown in Fig. 2. In addition, the currents in Fig. 8 and Fig. 9 have some distortion since the resonant power loop includes the winding resistance, parasitic capacitance of the transformer and filter, and forward voltage

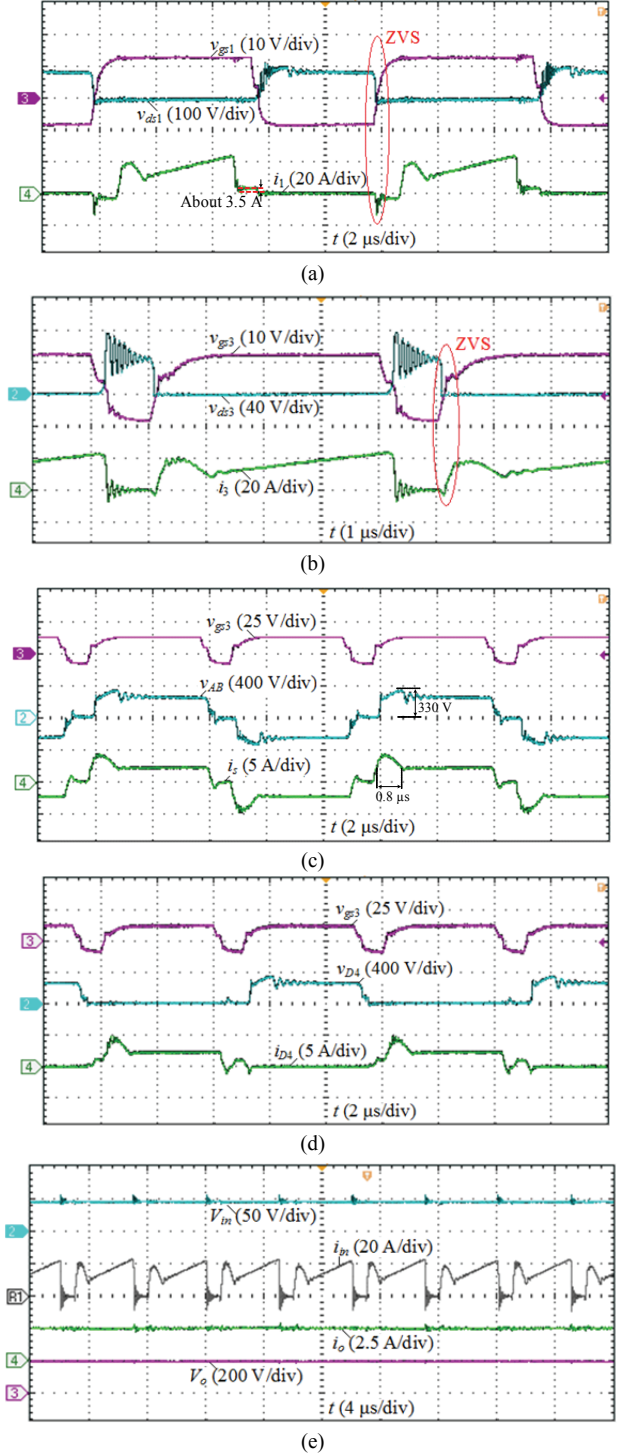


Fig. 8. Experimental waveforms under the conditions of a 45 V input voltage and a full load. (a)  $v_{gs1}$ ,  $v_{ds1}$  and  $i_1$ ; (b)  $v_{gs3}$ ,  $v_{ds3}$  and  $i_3$ ; (c)  $v_{gs3}$ ,  $v_{AB}$  and  $i_s$ ; (d)  $v_{gs3}$ ,  $v_{D4}$  and  $i_{D4}$ ; (e)  $V_{in}$ ,  $i_{in}$ ,  $V_o$  and  $i_o$ .

drops of the switch and diode, which can lead to additional power loss.

Fig. 8(a) and Fig. 9(a) illustrate the gate-source voltage  $v_{gs1}$ , drain-source voltage  $v_{ds1}$  and switch current  $i_1$  waveforms of  $S_1$  at a full load and a 20% load, respectively. It can be seen that the current through  $S_1$  goes to the negative before

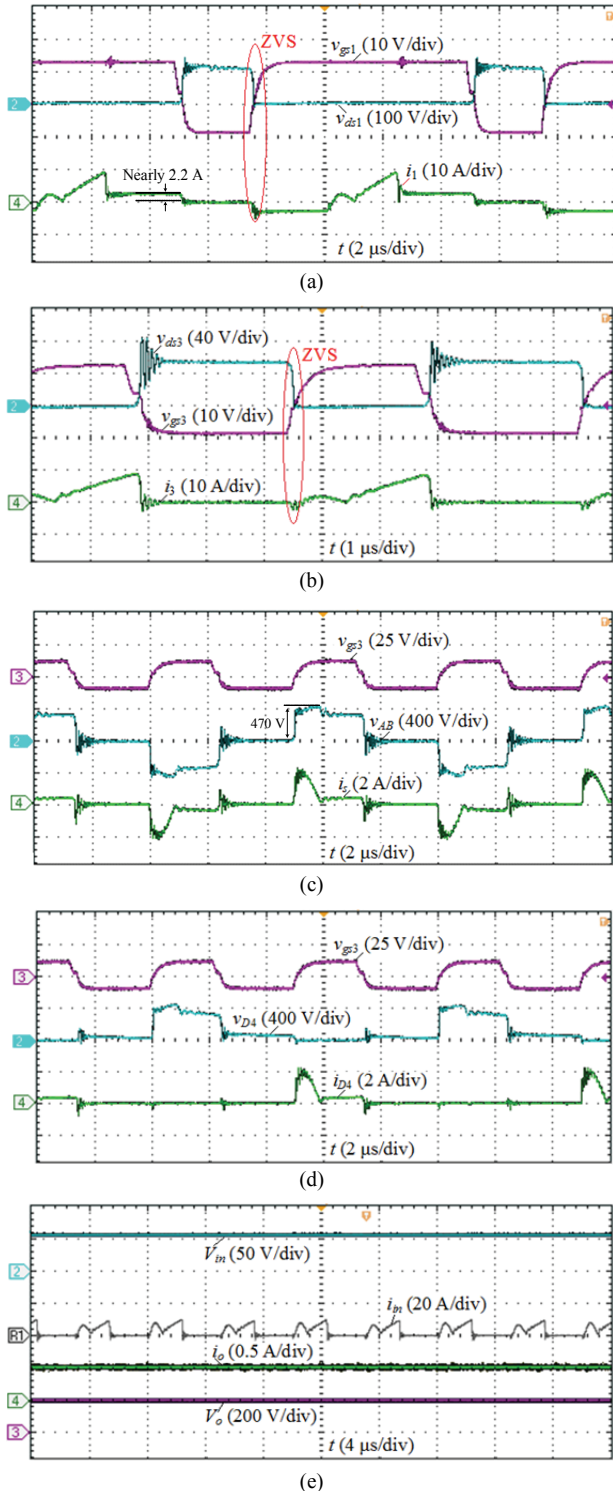


Fig. 9. Experimental waveforms under the condition of a 56 V input voltage and a 20% load. (a)  $v_{gs1}$ ,  $v_{ds1}$  and  $i_1$ ; (b)  $v_{gs3}$ ,  $v_{ds3}$  and  $i_3$ ; (c)  $v_{gs3}$ ,  $v_{AB}$  and  $i_s$ ; (d)  $v_{gs3}$ ,  $v_{D4}$  and  $i_{D4}$ ; (e)  $V_{in}$ ,  $i_{in}$ ,  $V_o$  and  $i_o$ .

conducting, which means that the ZVS turn-on for  $S_1$  can be realized easily under two conditions. In addition, it can be seen that the circulating currents decreases to about 3.5 A and 2.2 A, which are much smaller than half the maximum primary current. This implies that the conduction loss can be

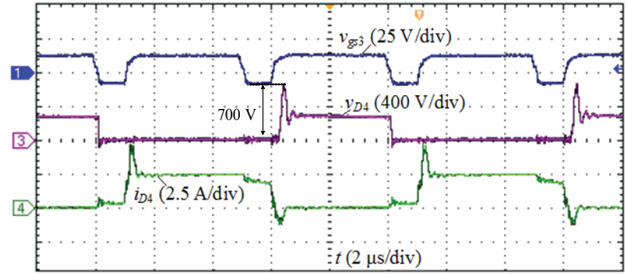


Fig. 10. Waveforms of  $v_{gs3}$ ,  $v_{D4}$  and  $i_{D4}$  without a clamping circuit at a full load.

reduced dramatically during the circulating stage when compared to existing topologies.

Fig. 8(b) and Fig. 9(b) show voltage and current waveforms of the switch  $S_3$ , which presents the ZVS realization of  $S_3$  at either a full load or a 20% load. However, note that there still exists a voltage ringing across  $S_3$ . The reason is that when  $S_3$  is off, the higher leakage inductance energy resulting from the primary peak current transfers to the output capacitor of  $S_3$ . In addition, other factors such as the stray inductances resulting from wiring connections, parasitic capacitors of the high frequency transformer and measurements produce some ringing.

Fig. 8(c)-(d) and Fig. 9(c)-(d) present secondary voltage and current waveforms. It can be seen that, by the simple auxiliary circuit, the transient overvoltage can be clamped to about 330 V and 470 V, which nearly match the designed values in (24). The clamping capacitor voltage is applied to the secondary leakage inductor in interval 5, which forces a decline of the diode current to 0 before the circulating stage, which is no voltage across the secondary diode. Hence, the diode can achieve a natural turn-off. These performances enable the use of low-voltage and low-cost diodes to reduce the conducting loss and reverse recovery loss.

Fig. 8(e) and Fig. 9(e) show the input and output voltage and current waveforms under two load conditions.

For comparison, the measured waveforms of  $D_4$  with  $V_{in}=45V$  at a full load from the converter in [21], [22] without a clamping circuit are presented in Fig. 10. Apparently, a much higher voltage spike, i.e., 700V occurs during the turn off process. In addition, it can be observed that the diode has a serious reverse recovery problem. However, it can be seen from Fig. 8 and 9(d) that this issue can be effectively resolved.

An efficiency comparison, with different output powers at  $V_{in}=45V$ , between the calculated and measured results for the proposed prototype and the basic converter in [21], [22] is shown in Fig. 11. The loss calculation models presented in [8], [23] and [24] are adopted here to assess the power loss of the proposed converter at different output powers. From Fig. 11, it can be seen that they have similar values for calculated and measured efficiencies. The measured peak efficiency can reach or exceed 93.02% for the prototype. However, only 92.38% can be obtained from the basic converter. Overall, the



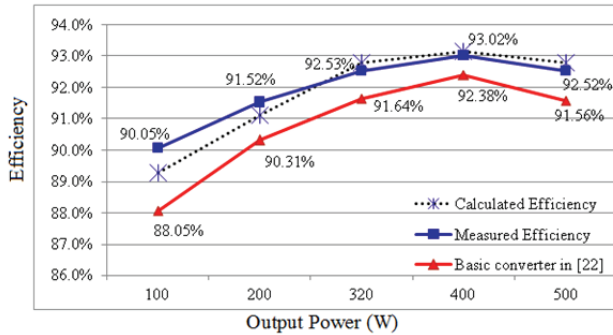
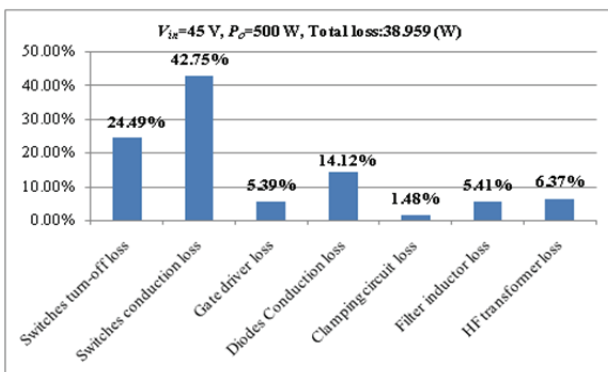
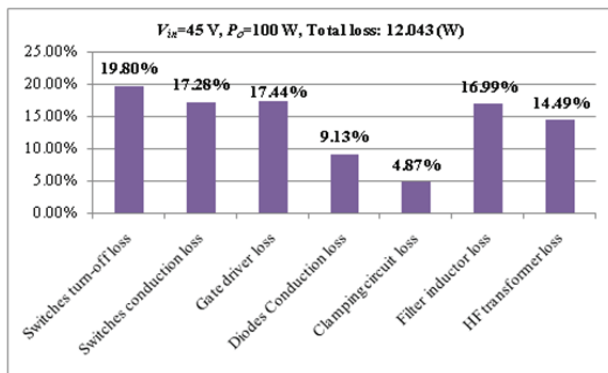


Fig. 11. Efficiency comparison between the calculated and measured results for the proposed prototype and the basic converter in [21], [22].



(a)



(b)

Fig. 12. Loss breakdown of the prototype at different output powers with  $V_{in}=45$  V. (a) 500W; (b) 100W.

proposed converter has a higher efficiency than the basic one over a wide load range. This is due to a lower circulating-loss, wider ZVS operation and lower rectifier stress.

Fig. 12 shows loss distribution assessments at a 20% load and the rated load. It is easy to see that the remarkable 42.75% loss in the rated load is the conduction loss of  $S_1\sim S_3$ , which results in a high on-resistance  $R_{DS(on)}$  of 40 m $\Omega$ . This implies that the efficiency can be further improved by using lower on-resistance switches. In addition, the added clamping circuit loss occupies a small portion of the losses. However, it has a key function for reductions of the rectifier diode voltage stress and primary circulating current.

## V. CONCLUSIONS

This paper proposes a new wide ZVS load range PWM voltage-fed push-pull converter. The steady-state operation, the characteristics and a performance comparison with similar converter have been presented. Experimental results from a 500 W prototype were obtained to verify the effectiveness of the proposed converter. The distinctive features of the proposed converter are summarized as follows.

- 1) All of the switches can realize ZVS turn-on over a wide load range with PWM control.
- 2) A higher voltage gain is obtained in comparison with similar converters.
- 3) The voltage stresses of the rectifier diodes can be suppressed and clamped by using a simple auxiliary circuit, which does not include any active devices or resistors.
- 4) The primary current can be reset by the secondary circuit during the circulating interval, and lower circulating current results in lower conduction loss and higher efficiency.

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