JPE 18-3-27

https://doi.org/10.6113/JPE.2018.18.3.931
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

# Analysis of Z-Source Inverters in Wireless Power Transfer Systems and Solutions for Accidental Shoot-Through State

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**Abstract**

Wireless power transfer (WPT) technology has been the focus of a lot of research due to its safety and convenience. The Z-source inverter (ZSI) was introduced into WPT systems to realize improved system performance. The ZSI regulates the dc-rail voltage in WPT systems without front-end converters and makes the inverter bridge immune to shoot-through states. However, when the WPT system is combined with a ZSI, the system parameters must be configured to prevent the ZSI from entering an "accidental shoot-through" (AST) state. This state can increase the THD and decrease system power and efficiency. This paper presents a mathematical analysis for the characteristics of a WPT system and a ZSI while addressing the causes of the AST state. To deal with this issue, the impact of the system parameters on the output are analyzed under two control algorithms and the primary compensation capacitance range is derived in detail. To validate the analysis, both simulations and experiments are carried out and the obtained results are presented.

**Key words:** Accidental shoot-through, Parameter design, Wireless power transfer, Z-source inverter

## I. INTRODUCTION

Wireless power transfer (WPT) technology can deliver power through an electromagnetic field without any physical connection between the transmitter and receiver [1]-[3]. Recent advancements in this field have led to more stringent design requirements being proposed and studied by researchers, such as efficiency improvement [4]-[8], coupling variation [9], [10], foreign object detection [11], [12], and output regulation [13]-[15]. Electronic technology plays a crucial role in these research studies and spurs WPT technology development.

The voltage source inverter (VSI) is an essential part of a WPT system that generates high-frequency ac power for transmission across a wireless media. Unfortunately, the output voltage of a conventional VSI is always equal to or lower than the input voltage, which limits this inverter's application in small-voltage or wide input situations. To address this barrier, front-end converters, such as boost converter or buck-boost converter are inserted between a dc source and a VSI to boost the dc-rail voltage [16], [17]. However, this requires more space and increases the cost of the system. For example, to add one additional high-power-high-frequency IGBT/MOSFET, one extra heat-sink and associated drive circuitry need to be accommodated. Considering the incremental costs and design complications, the ZSI presents a better alternative to front-end converters in WPT systems. A typical circuit layout is described in Fig. 1.

When compared with a conventional VSI, the ZSI has an input diode $D_S$ and a Z-source network added between the dc voltage source and the VSI [18]. The Z-source network consists of two identical inductors ($L_1$ and $L_2$) and capacitors

Manuscript received Oct. 8, 2017; accepted Jan. 3, 2018
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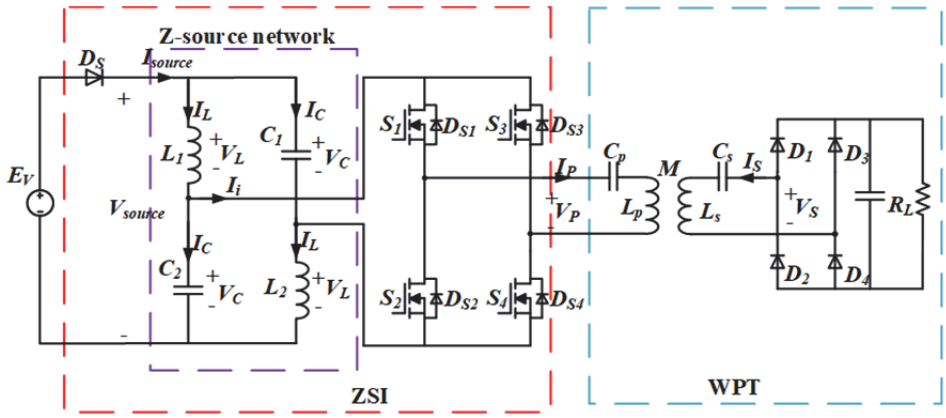



Fig. 1. Circuit of a WPT system with a ZSI.

($C_1$ and $C_2$) to boost the output voltage by shorting one or two legs of the rear-end inverter bridge. This is also referred to as the shoot-through (ST) state.

Guidelines to design a Z-source network based on steady state parameters were presented in [19]. Since the network is connected to a three-phase VSI, the output current of the network is regarded as a constant current. Meanwhile, the current of the network in a WPT system is approximately sinusoidal over part of one switching period due to a sinusoidal resonant current. Accordingly, the mathematical analysis in [19] should be modified when applied to a WPT system. In [20], the benefits of a ZSI in resonant converters are analyzed. These benefits include improved robustness and reliability, buck/boost function, and high efficiency over wide input and load ranges. The authors of [20] provided a good analysis for the application of a ZSI in resonance networks. However, the mathematical basis for the parameter design of the reduced Z-source network is lacking. In [21], the load regulation in a ZSI with two control methods is addressed and the operation principles are highlighted. However, the aforementioned researches only studied systems where the reflected impedance from the point of view of the inverter side is purely resistive. In practice, a resonant network may be deliberately mismatched or configured to be inductive for ZVS. The authors of [22] focused on ZVS operation and system modeling with an inductive impedance. This illustrates the benefits of asymmetrical voltage-cancellation control (AVC) for the series–parallel compensation topology. The accidental shoot-through (AST) state was not observed in this study. Therefore, it was not addressed by the authors. The authors of [23] presented the AST state, analyze its causes, and gave qualitative suggestions in terms of coil inductance and mutual inductance design. Although the guideline in [23] provides a solution direction, the mathematical design range is not provided for practical applications. In reality, when the primary equivalent impedance is mismatched with respect to the capacitance or inductance, the affected system may enter the AST state. This paper focuses on the impact of inductive impedance on the ZSI since some researchers configure the primary impedance to be inductive for ZVS operation. The analysis result can provide guidance and limitations for the configuration. The solution of capacitive operation is similar to that of inductive operation. In this paper, the conditions that cause the ZSI to enter the AST state are quantitatively analyzed, and the compensation capacitance range to avoid this state is provided in detail. Furthermore, an analysis and some suggestions for the coil inductance design and coupling coefficient design are also offered in this study.

This paper is organized as follows. Mathematical models of the WPT system and the Z-source inverter are reviewed in Section II. The AST state and its causes are presented in Section III. In Section IV, two control methods are described and comparedt. Then, the system parameters are derived under the two controls and the compensation capacitance range is formulated as well. Simulations and experiments are carried out and illustrated in Section V. Finally, some conclusions are given in Section VI.

## II. Mathematical Analysis of WPT and a ZSI

### A. Topology and Parameter Design of a WPT System

According to the placement of the compensation capacitors on the primary and secondary sides, there are four basic topologies: Series–Series (SS), Series–Parallel (SP), Parallel–Series (PS) and Parallel–Parallel (PP).

The ZSI creates a new control state, called the ST state, where at least one leg of the inverter is shorted. Thus, the inverter is effectively short-circuited at that time. If the primary side adopts a parallel compensation capacitor (PS and PP), the resonance path breaks because the terminals of the transmission coil and compensation capacitor are shorted at the ST state, and the energy stored in the compensation capacitor is discharged through switches. Therefore, series compensation on the primary side (i.e., SS and SP) is recommended. The authors of [22], [23] adopt the SP topology considering ZVS operation, while SS topology is

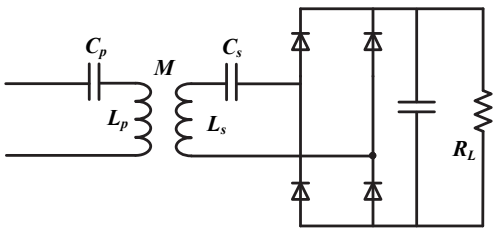



Fig. 2. Circuit diagram of a resonant network and a load.

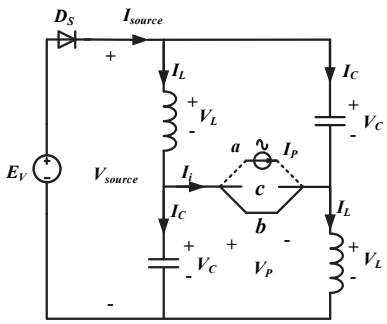



Fig. 3. Equivalent circuits of the three states of the ZSI: ***a***--active state; ***b***--ST state; ***c***--zero state.

analyzed in this paper. The reflected impedance from the secondary side in the SS topology can be easily adjusted to a resistance. Then, adjusting the primary compensation capacitor can determine the primary impedance characteristic, which facilitates the analysis in this paper. As shown in Fig. 2, $R_L$ represents the load resistance, $L_S$ and $C_S$ represent the receiver (Rx) coil inductance and compensation capacitance, $L_P$ and $C_P$ denote the transmission (Tx) coil inductance and compensation capacitance, and $M$ stands for the mutual inductance between the Tx and Rx coils.

The secondary side impedance $Z_S$ can be defined as:

$$Z_s(\omega) = j\omega L_s - j\frac{1}{\omega C_s} + \frac{8R_L}{\pi^2}. \tag{1}$$

When the switches work at the secondary resonant frequency $\omega_o$, $Z_S$ is purely resistive. The reflected impedance from the secondary side to the primary side is indicated as:

$$Z_{refs} = \frac{\pi^2 {\omega_o}^2 M^2}{8R_L}. \tag{2}$$

Accordingly, the primary side impedance can be formulated as:

$$Z_{inv} = j\omega L_p - j\frac{1}{\omega C_p} + \frac{\pi^2 {\omega_o}^2 M^2}{8R_L}. \tag{3}$$

According to Equ. (3), adjusting the capacitance can change the impedance characteristic. For instance, enlarging $C_P$ can make the primary resonant frequency lower than the switch frequency $\omega_o$, which leads to the impedance $Z_{inv}$ to be inductive. Furthermore, $M$ may be changed during practical application, which can make $Z_{inv}$ deviate far from pure resistance if the compensation capacitor has already been mismatched [23]. This paper analyzes the situation where the primary equivalent impedance is inductive or capacitive due to capacitance mismatching.

To guarantee a high transfer efficiency and a large power transfer, the quality factor of the Tx and Rx coils should be set to a large value. If the quality factor is small, the primary current cannot be sinusoidal, which can influence the ZSI performance.

At first, it can be obtained that:

$$\begin{cases} Q_S = \dfrac{\pi^2 \omega_o L_S}{8R_L} \\ Q_P = \dfrac{\omega_o L_P}{Z_{refs}} \end{cases} \tag{4}$$

where, $Q_S$ and $Q_P$ are the quality factors of the Rx and Tx coils.

Assuming that:

$$L_S = nL_P, M = k\sqrt{L_S L_P} \tag{5}$$

where, $n$ expresses the ratio coefficient, and $k$ expresses the coupling coefficient, and Equ. (4) can be expressed as:

$$\begin{cases} Q_S = \dfrac{\pi^2 \omega_o L_S}{8R_L} \\ Q_P = \dfrac{1}{k^2 Q_S} \end{cases}. \tag{6}$$

From Equs. (5) and (6), it can be concluded that the value of $Q_S$ is inversely proportional to the value of $Q_P$. Therefore, both of them should be set to moderate values. The ratio coefficient of the coil inductances does not influence the quality factor. Accordingly, two identical coils are proposed in this literature. The quality factors and coupling coefficient in accordance with the SAE J2954 guidelines are considered to be around 10 and 0.2, respectively.

### *B. Analysis of a ZSI*

Due to the Z-source network, the rear-end inverter has a shoot-through state in addition to the traditional active state and zero state. The three states are presented in Fig. 3 [19], where $V_{source}$ and $I_{source}$ are the voltage across and the current through the input terminals of the Z-source network, $V_L$ and $I_L$ are the voltage across and the current through the inductor, $V_C$ and $I_C$ are the voltage across and the current through the capacitor, $I_i$ is the current drawn from the Z-source network, and $V_P$ and $I_P$ are the primary input voltage and resonant current, respectively. $I_{Pm}$ and $\phi_P$ are the amplitude and phase of $I_P$.

State ***a*** is referred to as the active state, where the diagonal switches ($S_1$ and $S_4$ or $S_2$ and $S_3$) are turned on. The resonant converter draws $I_P$ from the Z-source network in the active state. The dashed line denotes that $I_i$ is not equal to $I_P$ if the system goes into the AST state. This will be fully analyzed and presented in Section III. State ***b*** is the new state, called the ST state, where at least two switches on the same bridge leg are turned on. In this state, $I_P$ is independent of the Z-source network and $I_i$, and the shorted bridge is used as the

free-wheeling circuits for $I_P$ and $I_i$. State ***c*** is referred to as the zero state, where the same horizontal switches ($S_1$ and $S_2$ or $S_3$ and $S_4$) are turned on.

According to the authors of [18], [19], [24], the zero state can be treated as a special case of the active state. Thus, this paper only analyzes systems operated in the active state and the ST state. Defining the period of the switch cycle $T_o$, the active period is written as $t_A = (1\text{-}d_S)T_o$ and the ST period is written as $t_S = d_S T_o$, where $d_S$ is the ST state duty ratio.

*1) Active State*

During the active period, the ZSI can be formulated as:

$$\begin{cases} V_{source}=E_V, I_{source}\neq 0 \\ V_{source}=V_L+V_C, I_{source}=I_L+I_C \\ I_i=I_L-I_C \\ |V_P|=V_C-V_L, I_P=\text{sign}(V_P)I_i \end{cases}. \tag{7}$$

The inductors and capacitors in the Z-source network are usually set large to suppress the harmonics and ripple. Therefore, both $I_L$ and $V_C$ can theoretically be treated as constants and replaced by their average values $\bar{I}_L$ and $\bar{V}_C$. Then, on basis of Equ. (7), $I_C$ and $|V_P|$ can be presented as:

$$\begin{cases} I_C = I_L - I_i \approx \bar{I}_L - \text{sign}(V_P) I_{Pm} \sin(\omega_o t\text{-}\phi_P) \\ |V_P| + E_V = 2\bar{V}_C \end{cases}. \tag{8}$$

*2) ST State*

During the ST period, the ZSI can be formulated as:

$$\begin{cases} V_{source}\neq 0, I_{source}=0 \\ V_{source}=V_L+V_C, I_{source}=I_L+I_C \\ I_i=I_L-I_C \\ V_P=V_L-V_C=0, |I_P|\neq|I_i| \end{cases}. \tag{9}$$

By replacing the average value $\bar{I}_L$ into Equ. (9), $V_L$, $I_C$ and $I_i$ can be written as:

$$\begin{cases} V_L \approx \bar{V}_C \\ I_C \approx -\bar{I}_L, I_i \approx 2\bar{I}_L \end{cases} \tag{10}$$

which means that the capacitors are charging the inductors, and $I_i$ reaches its maximum value in this state. Meanwhile, the ZSI and WPT resonant network can be regarded as two independent parts. In other words, $I_i$ and $I_P$ have no impact on each other.

Based on the voltage balance and current balance principles, $\bar{I}_L$ and $\bar{V}_C$ can be calculated as:

$$(1-d_S)(E_V-\bar{V}_C)\text{-}d_S\bar{V}_C = 0 \tag{11}$$

$$\frac{\int_0^{t1}\bar{I}_L - I_{Pm}\sin(\omega_o t\text{-}\phi_P)+\int_{t1}^{t2}-\bar{I}_L+\int_{t2}^{t3}\bar{I}_L+I_{Pm}\sin(\omega_o t\text{-}\phi_P)+\int_{t3}^{t4}-\bar{I}_L}{T_o}=0 \tag{12}$$

where, the time interval [0, $t1$] represents the active state period with a positive output voltage, [$t2$, $t3$] represents the active state period with a negative output voltage, and [$t1$, $t2$] and [$t3$, $t4$] represent the ST state periods. The value of this time point is depended on the control algorithm.

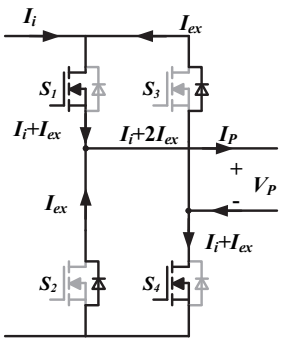



Fig. 4. Current routine in the AST state.

By the variable separation of Equ. (11), the relationship between $\bar{V}_C$ and $E_V$ can be further presented as:

$$\bar{V}_C = \frac{1-d_S}{1-2d_S}E_V. \tag{13}$$

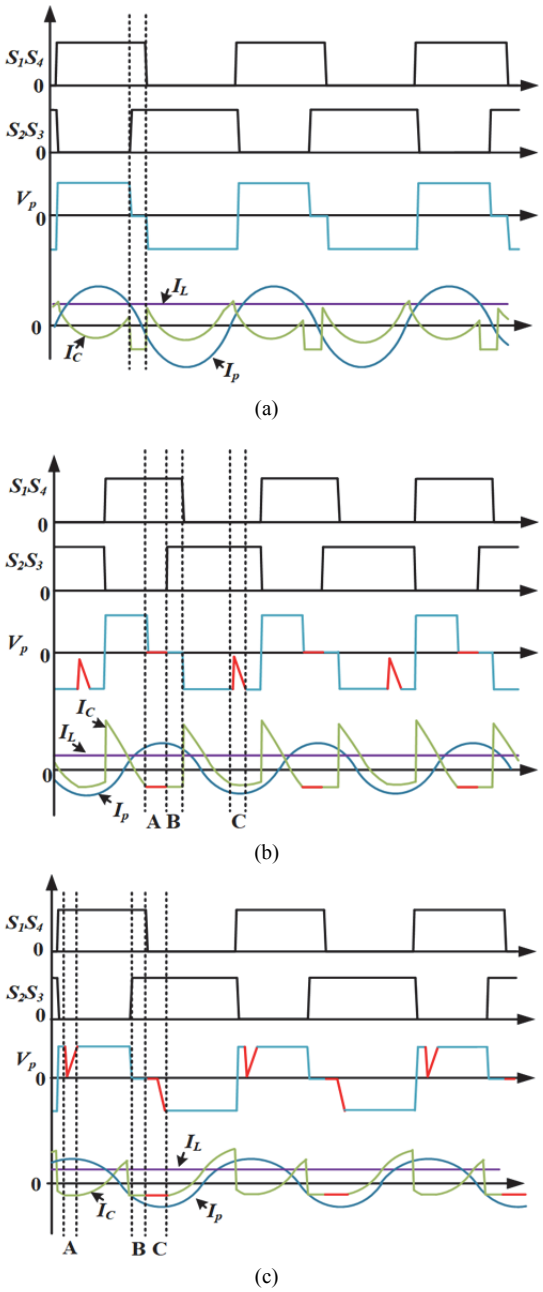
Accordingly, the duty ratio $d_S$ must be less than 0.5.

As analyzed in Equs. (7) and (9), the primary input voltage $V_P$ is a square waveform. Thus, the amplitude is equal to $|V_P|$ in Equ. (8), and is further rewritten by substituting Equ. (13) as:

$$\hat{V}_P = \frac{1}{1-2d_S}E_V. \tag{14}$$

## III. Accidental Shoot-Through State

For a single-phase ZSI, large inductances and capacitances are required to suppress the double switching-frequency ripple [25]. Moreover, when the inductance is small, it is easier for the inductor current to enter the discontinuous current mode (DCM), causing the dc-link voltage to drop [26]. To obtain a large continuous current through the inductors, a stable voltage across the capacitors. In addition, to limit ripple, the parameters of the Z-source network are set to large values in this literature. However, If the whole system parameters are poorly configured, the AST state in the ZSI may still occur. Unlike the dc-link voltage drop caused by discontinuous current [26], the AST state is caused by the resonant current freewheeling through the inverter's antiparallel diodes. Specifically, when the Z-source network cannot supply enough current $I_i$ to provide the primary resonant current $I_P$, part of the resonant current $I_{ex}$ goes through the parasitic or antiparallel diodes of the turned-off MOSFETs in the inverter bridges, dropping the output voltage to zero and pushing the ZSI into the AST state, as demonstrated in Fig. 4. Once this problem occurs, it can be observed in the initial stage of the system and persists even when the system comes to a stable state. The amplitude of the ZSI output voltage increases due to the effective ST state duty ratio surges. Simply enlarging the inductance and capacitance cannot solve the AST problem,




(a) (b) (c)

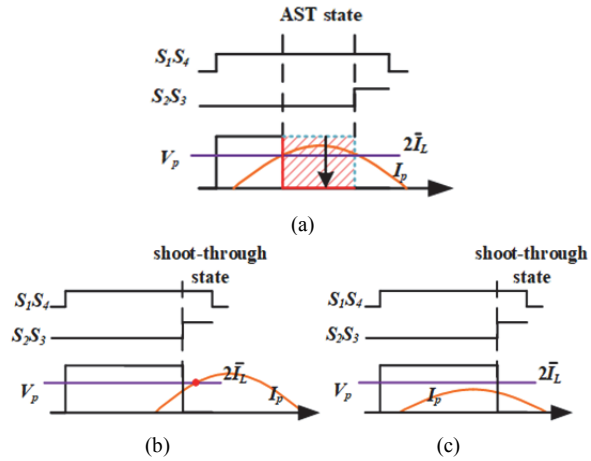
Fig. 5. PSIM simulations: (a) Normal operation; (b) AST with an inductive impedance; (c) AST with a capacitive impedance.

which is essentially caused by the network mismatch and always happens at the active state. At such times, Equ. (7) can be modified as:

$$\begin{cases} V_{source} = V_L + V_C, 0 = I_L + I_C \\ I_i = I_L - I_C, \\ V_P = 0, |I_P| = |I_i + 2I_{ex}| \succ |I_i| \end{cases} \tag{15}$$

which is similar to the ST state equation.

To present the AST state, simulations are conducted in the PSIM environment. Results of these simulations are illustrated in Fig. 5. Fig. 5(a) describes waveforms where the primary equivalent impedance is matched to approximate or pure resistance. Fig. 5(b) shows waveforms where the primary equivalent impedance is matched to a large inductance. Fig. 5(c) shows waveforms where the primary equivalent impedance is matched to a large capacitance.




(a) (b) (c)

Fig. 6. Operating waveforms: (a) AST state; (b) Strategy 1: delay the crest; (c) Strategy 2: suppress the crest.

Fig. 5(a) demonstrates a properly functioning system. The output voltage is in conformity with the switch actions, and the waveforms show good agreement with Equs. (7) and (9). However, the waveforms in Fig. 5(b) show the AST state with an inductive impedance, which can be described by Equ. (15). It can be seen that the theoretical active state in interval **A** and interval **C** has already become the AST state. The difference between interval **A** and interval **C** is caused by the asymmetry of the control algorithm. These AST states start at the points given in Equ. (16).

$$\begin{cases} I_C = -\bar{I}_L \\ \left| I_{Pm} \sin(\omega_o t_{intervalA} + 2k\pi - \phi_P) \right| = 2\bar{I}_L \\ \left| I_{Pm} \sin(\omega_o t_{intervalC} + 2k\pi - \phi_P) \right| = 2\bar{I}_L \end{cases} \tag{16}$$

where, $t_{intervalA}$ and $t_{intervalC}$ are the start time points of interval **A** and interval **C**, respectively.

Fig. 5(c) illustrates the AST state of the capacitive impedance, where the theoretical active states in interval **A** and interval **C** are also the AST state. In interval **C**, $V_P$ is zero at first because of the AST state. Then, it ramps down to a minus value because of the capacitive impedance. However, the AST state can still be illustrated by Equs. (15) and (16). Thus, the analysis method for the inductive condition can also be used for the capacitive condition. A detailed analysis for the inductive impedance scenario is given in this paper.

Based on Equs. (15) and (16), there are two solutions, presented in Fig. 6(a), to avoid the AST state. One strategy is to make $I_P$ larger than $2\bar{I}_L$ only in the ST state, as shown in Fig. 6(b). The other strategy, depicted in Fig. 6(c), is to maintain the resonant current amplitude $I_{Pm}$ to be less than $2\bar{I}_L$, that is:

$$\frac{\bar{I}_L}{I_{Pm}} > \frac{1}{2}. \tag{17}$$

## IV. Control Algorithms and Parameter Design

### A. Control Algorithms in a ZSI

Prior to analyzing the feasibility of the above solutions, two control algorithms, phase shift control (PSC) and asymmetrical voltage-cancellation control (AVC), are presented and compared. PSC is a widely used control technique in full-bridge converters. It changes the output power by phase shifting the switching conductions. Meanwhile, the AVC controls the output variation by the zero-voltage duty ratio in the first half of a cycle. The AVC can help a VSI realize the zero-voltage switch [27]. However, its asymmetricity makes the system more complicated. To achieve the AST state, the switching conductions of the PSC and AVC are modified and all of the zero states are replaced. Fig. 7(a) and Fig. 7(b) depict typical waveforms of the PSC and AVC, respectively. $\alpha$ is equal to $d_S \cdot 2\pi$, and $V_{P1}$ denotes the fundamental harmonic of the primary voltage $V_P$. $\phi_1$ denotes the phase lag between $V_{P1}$ and $V_P$, and $\phi_P$ denotes the phase lag between $V_{P1}$ and $I_P$. Assuming that the phase of $V_{P1}$ is zero, $\phi_P$ is the phase of $I_P$ as stated in Section II.

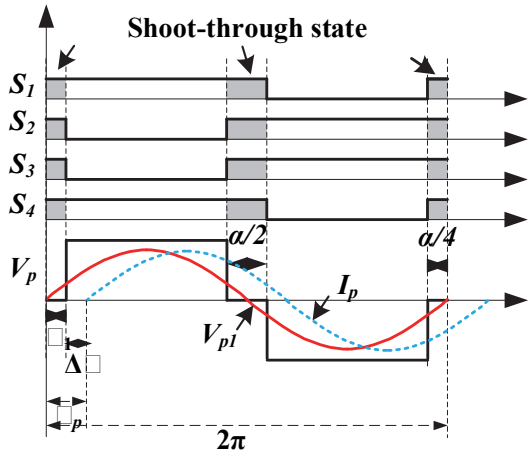
By a Fourier series expansion, the fundamental harmonic voltage $V_{P1}$ can be derived from the voltage $V_P$. The amplitude, phase lag and total harmonic distortion (THD) are calculated as:

$$\begin{cases} V_{P1m} = \dfrac{4\hat{V}_P}{\pi}\cos\dfrac{\alpha}{4} \\ \phi_1 = \cos\dfrac{\alpha}{4} = \tan^{-1}\dfrac{\sin\dfrac{\alpha}{2}}{3+\cos\dfrac{\alpha}{2}} \\ THD = \dfrac{\dfrac{\pi^2}{8}\left(1-\dfrac{\alpha}{2\pi}\right)-\cos^2\dfrac{\alpha}{4}}{\cos^2\dfrac{\alpha}{4}} \end{cases} \tag{18}$$

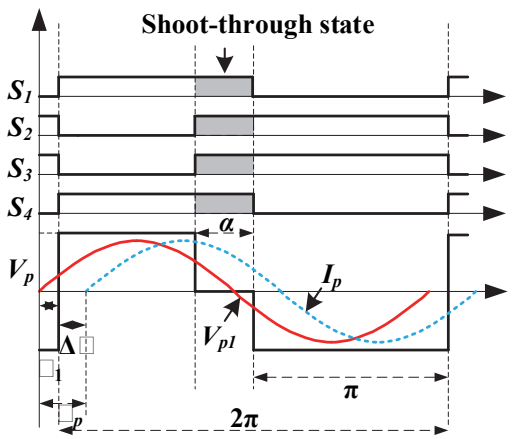
for the PSC, and as:

$$\begin{cases} V_{P1m} = \dfrac{\hat{V}_P}{\pi}\sqrt{10+6\cos\alpha} \\ \phi_1 = \tan^{-1}\dfrac{\sin\alpha}{3+\cos\alpha} \\ THD = \dfrac{2\pi^2\left(1-\dfrac{\alpha}{2\pi}\right)-(10+6\cos\alpha)}{10+6\cos\alpha} \end{cases} \tag{19}$$

for the AVC.




(a)




(b)

Fig. 7. Typical waveforms under two control strategies: (a) PSC; (b) AVC.

Comparing Equ. (18) with Equ. (19), it can be seen that the PSC can generate a larger voltage amplitude with the same ST duty ratio while having a larger phase $\phi_1$ than the AVC. Once the DC source voltage, the ST duty ratio, the control method, and the equivalent primary impedance are determined, $\phi_P$ can also be determined. A small $\phi_1$ means a large $\Delta\phi$ in Fig. 7. Therefore, the current wave crest has greater possibility to appear in the ST state in the positive half cycle under the AVC. However, it cannot solve the problem existing in the negative half cycle because there is no ST state under the AVC. Furthermore, it is difficult to keep the crest from showing up in the ST state unless $\phi_P$ is close to $0.5\pi$ or $d_S$ is over 0.25, which increases the reactive power, decrease the efficiency and reduces the output scope. Thus, maintaining the resonant current amplitude $I_{Pm}$ less than $2\bar{I}_L$ is the easier of the two methods described. Therefore, it is recommended in this paper.

The relationships between the *THD* and $\alpha$ are represented in Fig. 8. The dotted dashed line represents the *THD* of the AVC, the dotted line represents the *THD* of the PSC, and the solid line represents the result of the *THD* of the PSC minus

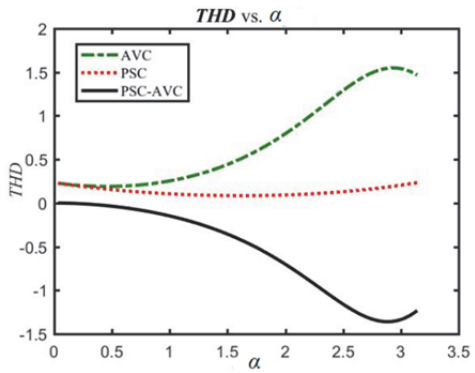



Fig. 8. *THD* vs. $\alpha$ for different controls.

the *THD* of the PSC. As can be seen, the two *THD* values go up with the enhancement of $\alpha$. However, the growth range of the AVC is larger than that of the PSC. When the AST state occurs, the effective ST duty ratio $d_S$ increases, and $\alpha$ and the *THD* increase accordingly. It is worth noting that the distortion is more obvious under the AVC.

### *B. Parameter Design under Different Controls*

#### *1) System under the PSC*

Since the resonant coils work as a resonant frequency filter and only the fundamental frequency component is allowed to pass, $V_P$ can be approximated by its fundamental harmonic voltage $V_{P1}$.

$$V_{P1}=\frac{4E_V}{\pi(1-2d_S)}\cos(\frac{d_S\pi}{2})\sin(\omega_o t). \tag{20}$$

With Equ. (3), $I_P$ can be derived as:

$$I_P = I_{Pm}\sin(\omega_o t-\phi_P) \tag{21}$$

where:

$$\begin{cases} I_{Pm}=\dfrac{4E_V}{\pi(1-2d_S)|Z_{inv}|}\cos(\dfrac{d_S\pi}{2}) \\ \phi_P=\tan^{-1}\left[(\omega_o L_p-\dfrac{1}{\omega_o C_p})\Big/\dfrac{\pi^2\omega_o{}^2M^2}{8R_L}\right] \\ |Z_{inv}|=\sqrt{(\omega_o L_p-\dfrac{1}{\omega_o C_p})^2+(\dfrac{\pi^2\omega_o{}^2M^2}{8R_L})^2} \end{cases}. \tag{22}$$

Under the PSC, Equ. (12) can be modified and rewritten as:

$$\begin{aligned}&(1-2d_S)T_o\bar{I}_L \\ &=-\frac{I_{Pm}}{\omega_o}\left\{\begin{matrix}\cos\left[\omega_o(\frac{T_o}{2}-\frac{d_S T_o}{4})-\phi_P\right]-\cos\left[\omega_o(\frac{d_S T_o}{4})-\phi_P\right] \\ -\cos\left[\omega_o(T_o-\frac{d_S T_o}{4})-\phi_P\right]+\cos\left[\omega_o(\frac{T_o}{2}+\frac{d_S T_o}{4})-\phi_P\right]\end{matrix}\right\}\end{aligned} \tag{23}$$

which can be further simplified as:

$$\bar{I}_L=\frac{2}{(1-2d_S)\pi}\cos(\frac{d_S}{2}\pi)\cos\phi_P I_{Pm}. \tag{24}$$

If $\phi_P$=0, the impedance is purely resistive. It can be drawn from Equ. (24) that:

$$\frac{\bar{I}_L}{I_{Pm}}=\frac{2\cos(\frac{d_S}{2}\pi)}{(1-2d_S)\pi}\geq 0.64 \qquad d_S\in[0,0.5), \tag{25}$$

which means the resonant current amplitude $I_{Pm}$ is always less than $2\bar{I}_L$.

If $0.5\pi>\phi_P>0$, the impedance is inductive. By substituting Equ. (24) into Equ. (17), it requires:

$$\phi_P<\cos^{-1}\frac{(1-2d_S)\pi}{4\cos(\frac{d_S}{2}\pi)}. \tag{26}$$

Equ. (26) implies that the range of $\phi_P$ decreases with the increment of $d_S$. When $d_S$ is zero, the ZSI works as a conventional VSI and Equ. (26) is always satisfied. When $d_S$ is above zero, the Z-source network comes into play and the variation of $\phi_P$ has to obey Equ. (26) or the AST phenomenon occurs. In addition, according to Equ. (24) and Equ. (26), this state is mainly caused by the resonant network rather than the Z-source network. This explains the claim at the beginning of Section III that changing the inductance and capacitance in the Z-source network cannot solve the AST problem.

Since the phase displacement $\phi_P$ is limited, the variation of $C_P$ has a certain range. By substituting Equs. (4) and (22) into Equ. (26), this can be formulated as:

$$\frac{1}{\omega_o{}^2L_P}<C_P<\frac{1}{\omega_o{}^2L_P\left[1-\tan(\cos^{-1}\dfrac{(1-2d_S)\pi}{4\cos(\frac{d_S}{2}\pi)})\Big/Q_P\right]}. \tag{27}$$

#### *2) System under the AVC*

When the control algorithm is changed to the AVC, the fundamental harmonic of the primary resonant voltage $V_P$ is rewritten as:

$$V_{P1}=\frac{E_V}{\pi(1-2d_S)}\sqrt{10+6\cos(2d_S)}\sin(\omega_o t). \tag{28}$$

$I_P$ can be derived as

$$I_P = I_{Pm}\sin(\omega_o t-\phi_P) \tag{29}$$

where:

$$\begin{cases} I_{Pm}=\dfrac{E_V}{\pi(1-2d_S)|Z_{inv}|}\sqrt{10+6\cos(2d_S)} \\ \phi_P=\tan^{-1}\left[(\omega_o L_p-\dfrac{1}{\omega_o C_p})\Big/\dfrac{\pi^2\omega_o{}^2M^2}{8R_L}\right] \\ |Z_{inv}|=\sqrt{(\omega_o L_p-\dfrac{1}{\omega_o C_p})^2+(\dfrac{\pi^2\omega_o{}^2M^2}{8R_L})^2} \end{cases}. \tag{30}$$

Comparing Equ. (22) with Equ. (30), $I_{Pm}$ in the AVC is smaller than that in the PSC. To some extent, the system under the AVC has less possibility to encounter the AST problem.

Under these conditions, Equ. (24) is changed to:

$$\bar{I}_L=\frac{1}{2(1-2d_S)\pi}\left[\cos(2d_S\pi+\phi_P-\tan^{-1}\frac{\sin 2d_S\pi}{3+\cos 2d_S\pi})+3\cos(\phi_P-\tan^{-1}\frac{\sin 2d_S\pi}{3+\cos 2d_S\pi})\right]I_{Pm} \quad (31)$$

whose complicity is caused by asymmetricity.

Since:

$$\tan^{-1}\frac{\sin 2d_S\pi}{3+\cos 2d_S\pi}\le\tan^{-1}\frac{\sin 2d_S\pi}{1+\cos 2d_S\pi}=d_S\pi \quad (32)$$

the following is obtained:

$$\begin{aligned}&\cos(2d_S\pi+\phi_P-\tan^{-1}\frac{\sin 2d_S\pi}{3+\cos 2d_S\pi})+3\cos(\phi_P-\tan^{-1}\frac{\sin 2d_S\pi}{3+\cos 2d_S\pi})\\&\ge\cos(2d_S\pi+\phi_P-d_S\pi)+3\cos(\phi_P-d_S\pi)\\&\ge\cos(d_S\pi+\phi_P)+3\cos(d_S\pi-\phi_P)\end{aligned} \quad (33)$$

By substituting Equs. (33) and (31) into Equ. (17), it is further rewritten as:

$$\frac{\bar{I}_L}{I_{Pm}}>\frac{2\cos(d_S\pi+\phi_P)}{(1-2d_S)\pi}>\frac{1}{2}. \quad (34)$$

If:

$$\phi_P<\cos^{-1}\frac{(1-2d_S)\pi}{4}-d_S\pi \quad (35)$$

the AST state will never occur.

If $\phi_P=0$, it can be derived that:

$$\frac{\bar{I}_L}{I_{Pm}}>\frac{2\cos d_S\pi}{(1-2d_S)\pi}\ge 0.76 \qquad d_S\in[0,0.5). \quad (36)$$

Since the AVC can be considered as a generalization of PS and asymmetrical duty-cycle (ADC) control [27], a conclusion can be drawn from Equs. (36) and (25) that the AST state never occurs in a purely resistive impedance system provided the AVC control and its derivative methods are adopted. These two equations also explain the why the AST state did not occur in the aforementioned research [21], [28].

The range of the compensation capacitance is:

$$\frac{1}{\omega_o^2 L_P}<C_P<\frac{1}{\omega_o^2 L_P\left[1-\tan(\cos^{-1}\frac{(1-2d_S)\pi}{4}-d_S\pi)\Big/Q_P\right]}. \quad (37)$$

It is worth mentioning that this range is smaller than the practical range because of inequation Equ. (33). Equs. (35) and (37) are both sufficient but unnecessary conditions.

In addition, Equs. (27) and (37) indicate that a large $Q_P$ can reduce the capacitance range. In other words, high $Q_P$ systems are more sensitive to the capacitance variation. $Q_P$ is inversely proportional to the coupling coefficient $k^2$ according to Equ. (6). Therefore, a large coupling coefficient $k$ helps in decreasing $Q_P$ to enlarge the capacitance range. Compared with the solution in [23], the difference in the recommended $k$ is caused by the compensation topology. For the SP topology, the secondary reflected impedance contains the receiver inductance. As a result, the primary compensation capacitance is different. A small $k$ is preferred to maintain ZVS in the SP so that $L_P$ needs to be larger than $L_S$ to avoid the AST state as a trade-off in [23]. However, in this study, Equs. (27) and (37) indicate that transfer coils with a small inductance can better void the AST state because $C_P$ has a larger range for variations and compensation. Assuming that other conditions are the same, the range of $C_P$ is [7.46 nF, 8.86 nF] if $L_p$ is 470 μH and it is [43.4 nF, 58.6 nF] if $L_p$ is 80 μH based on Equ. (27). It is obvious that a Z-source inverter can be less sensitive and have better performance in small inductance coil systems.

### C. Power and Efficiency Estimation

When the primary compensation capacitor changes, the equivalent impedance and input/output power are different.

Due to Equs. (7) and (9), the input power of a Z-source network, $P_{source}$, can be calculated as:

$$\begin{aligned}P_{source}&=\int V_{source}I_{source}dt=\int E_V(I_L+I_C)dt\\&=\int E_V(2\bar{I}_L-\mathrm{sign}(V_P)I_{Pm}\sin(\omega_o t-\phi_P))dt.\end{aligned} \quad (38)$$

If Equ. (17) is not satisfied, $I_{source}$ may become negative and part of the integral in Equ. (38) becomes negative. Moreover, $\bar{I}_L$ and $I_{Pm}$ are reduced when the equivalent impedance increases. In general, the reduction of the input power of the Z-source network is inevitable and this trend is experimentally verified in the next section.

For the PSC, the input power is illustrated as:

$$P_{source}=4E_V\left[\pi\bar{I}_L(1-d_S)-I_{Pm}\cos(\frac{d_S\pi}{2})\cos\phi_P\right] \quad (39)$$

where, the input power for the AVC is illustrated as:

$$P_{source}=E_V\left\{4\pi\bar{I}_L(1-d_S)-I_{Pm}\left[\cos(2d_S\pi+\phi_P-\phi_1)+3\cos(\phi_P-\phi_1)\right]\right\}. \quad (40)$$

Then, the efficiency $\eta$ can be assessed and defined as:

$$\eta=\frac{P_{load}}{P_{source}}=\frac{V_{load}^2}{R_L P_{source}}. \quad (41)$$

Above all, the AST state leads to an increase in the *THD* value as shown in Fig. 8. This means a reduction in the percentage of the fundamental frequency content. Additionally, since resonant coils filter higher harmonics and only allow the fundamental frequency to go through, the power transferred to the load decreases further and the efficiency declines.

## V. Simulation and Experimental Results

In this section, simulations are carried out in the PSIM environment to validate the analysis. As mentioned in Section IV, the AST state occurs less in a small inductance transfer coil than in a large one. However, to verify the proposed method, the inductance of the Tx coil is set to a medium value. The coil-to-coil gap and the coil diameter are selected according to the recommendation range of the SAE J2954 guidelines. Once the coils are determined and the coil-to-coil gap is selected, the mutual inductance and coupling coefficient are set. The parameters of the simulations are listed in Table I.

TABLE I
MODEL PARAMETERS

| Parameter | Value |
|---|---|
| $R_L$ | 15 Ω |
| $L_P$ | 294 μH |
| $L_S$ | 298 μH |
| $M$ | 38.5 μH |
| $C_S$ | 11.8 nF |
| $f_o$ | 85 kHz |
| $E_V$ | 100 V |
| $L_1$ & $L_2$ | 2 mH |
| $C_1$ & $C_2$ | 440 μF |
| $d_S$ | 0.1 |

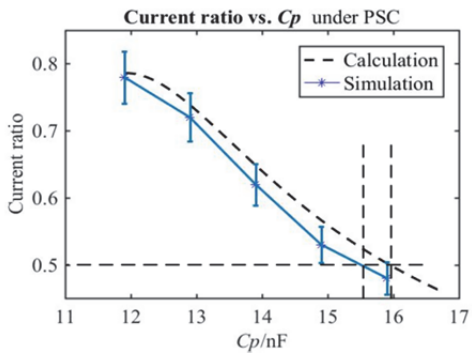



Fig. 9. Calculation and simulation ratios of $\bar{I}_L$ and $I_{Pm}$ under: (a) PSC; (b) AVC.

TABLE II
EXPERIMENTAL SETUP

| Parameter | Value |
|---|---|
| *Controller* | DSP TMS320F28335 |
| $S_1$~$S_4$ | SCT3040 |
| $D_{S1}$~$D_{S4}$ | MUR3020PT |
| $D_1$~$D_4$ | DSEI60-12A |
| $D_S$ | MUR3020PT |
| *Z-source inductors* | Toroidal Fe-Si-Al, 2 mH |
| *Z-source capacitors* | Nichicon electrolytic, 220 μF/200 V |
| *Coil diameter* | 40 cm |
| *Coil-to-coil gap* | 15 cm |

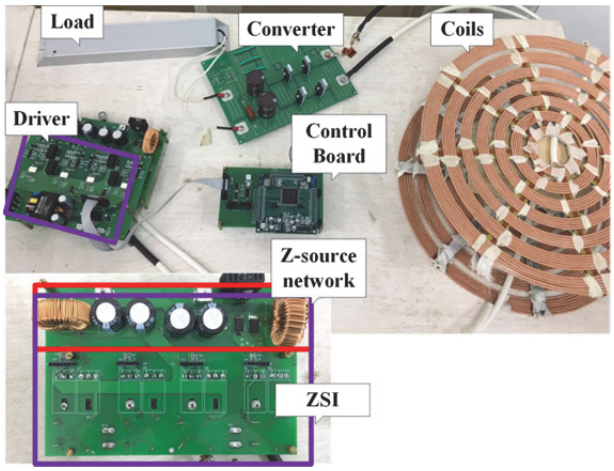
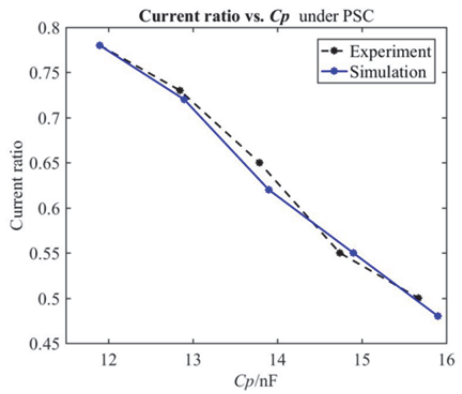



Fig. 10. Experimental platform.

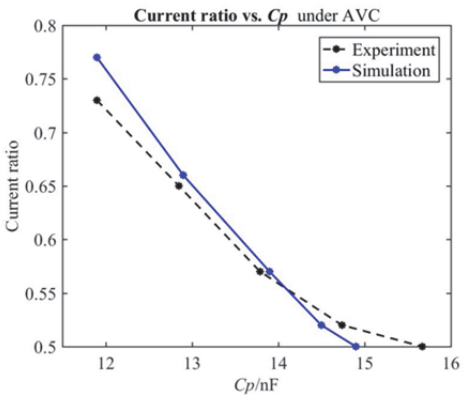
During simulations, $C_P$ is adjusted and the ratios of $\bar{I}_L$ and $I_{Pm}$ are presented in Fig. 9. For the PSC, the regular range of the capacitance $C_P$ is [11.9 nF, 15.9 nF] calculated by Equ. (27). Fig. 9(a) depicts the current ratios versus $C_P$ under the PSC. The dashed line represents the calculation results based on Equ. (24), and the solid line represents the simulation results. The relative error remains around 3%. For the AVC, the regular range of the capacitance $C_P$, calculated by Equ. (38), is [11.9 nF, 13.9 nF]. Fig. 9(b) depicts the current ratios versus $C_P$ under the AVC. The upper dashed line represents calculation results based on Equ. (33), the lower dashed line represents calculation results based on Equ. (34), and the solid line represents simulation results. The simulation results lie between the two calculated results, which implies that Equ. (37) is stricter than the practical range while Equ (33) is more relaxed. Although the dashed lines do not fit the simulation very well, they follow the same trend.

An experimental platform has been developed to demonstrate and evaluate the above analysis. Fig. 10 shows the experimental platform and some of the components are tabulated in Table II. A DSP TMS320F28335 was used as a digital controller, SiC MOSFETs SCT3040 were selected for inverter switches, and Schottky diodes DSEI60-12A were selected for rectifier side diodes. For the Z-source network, the MUR3020PT was chosen as the input diode and parallel diodes for the SiC MOSFETs, four nichicon electrolytic capacitors (220 μF, 200 V) and two toroidal inductors (Fe-Si-Al, 2 mH) were applied. The coil diameter is 40 cm and the coil-to-coil gap is set to 15 cm. The inductances are measured by a Keysight E4980AL LCR meter under 85 kHz.

If the intrinsic resistance of the coils cannot be ignored, $Q_P$ is decreased and the range of $C_P$ in Equs. (27) and (37) should increase. In this experiment, if the intrinsic ac resistance of the coils, 2 Ω, is taken into account, the regular range of the capacitance $C_P$ is changed to [11.9 nF, 16.1 nF] for the PSC and [11.9 nF, 13.7 nF] for the AVC, which both have a small increase. Thus, the intrinsic resistors can be

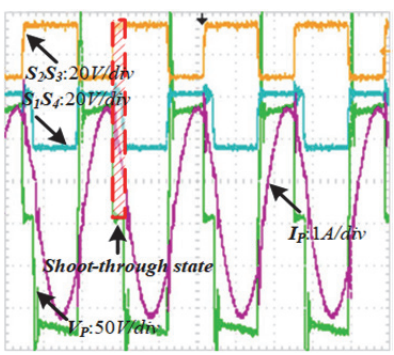



(a)

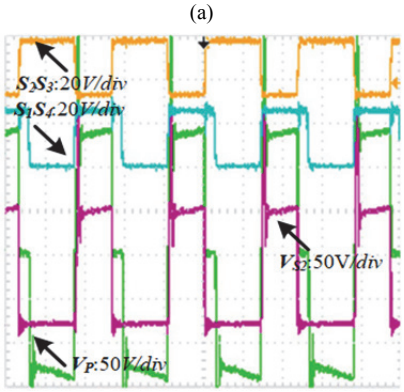



(b)

Fig. 11. Experimental and simulation ratios of $\bar{I}_L$ and $I_{Pm}$ under: (a) PSC; (b) AVC.

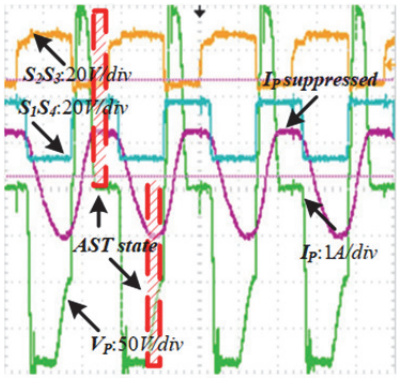



(a)

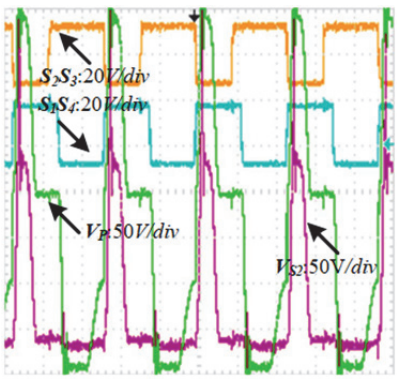



(b)

Fig. 12. Normal State (a) Experimental Output (b) Switch voltage.




(a)




(b)

Fig. 13. AST State (a) Experimental Output (b) Switch voltage.

ignored. Fig. 11(a) depicts the current ratios versus $C_P$ under the PSC. The dashed line represents the experiment results and the solid line represents the simulation results. Fig. 11(b) depicts the current ratios versus $C_P$ under the AVC. The dashed line represents the experiment results and the solid line represents the simulation results.

The experiments and simulations both illustrate the same trends in having errors within a reasonable range. At first, although the capacitors are measured by a Keysight E4980AL LCR meter under 85 kHz, the total capacitance might change when they are working in parallel. Secondly, the full bridge has a power loss caused by the MOSFETs. Since the switch conductions under the PSC and the AVC are different, the power loss and the errors in Fig. 11(a) and Fig. 11(b) are inconsistent. However, the experiment validates the analysis.

Waveforms, when the system works well, are illustrated in Fig. 12(a). The voltage is in conformity with the control logic of the switches, and the amplitude is around 125 V. The switch voltage across $S_2$ and the corresponding gate driver waveforms are presented in Fig. 12(b). When the gate signal of $S_2$ is negative, $S_2$ is shut off and the voltage across $S_2$ is high. The gate driver and voltage waveforms reflect that there is no extra current passing through the parallel or parasite diode of $S_2$.

Meanwhile, to present the AST state in an experiment, the primary compensation capacitance is added to 19.3 nF, and the waveforms are depicted in Fig. 13(a). The red dashed area

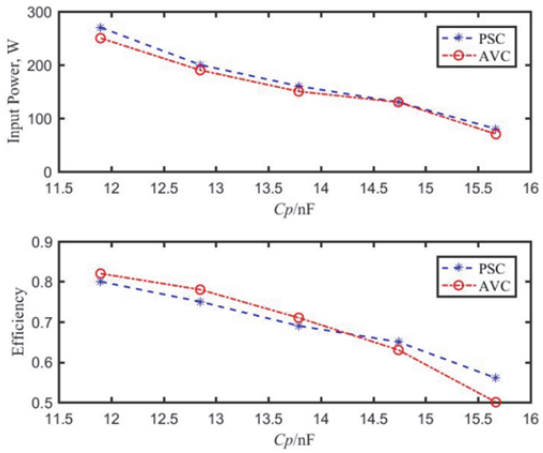



Fig. 14. Input power and efficiency under PSC and AVC.

denotes the AST state. Part of the positive half cycle voltage decreases to zero and part of the negative half cycle voltage recedes too. The amplitude of the inverter output rises to 190 V, which should theoretically be around 125 V as in Fig. 12(a). This is due to the fact that part of active state is replaced by the ST state and the effective ST duty ratio $d_S$ increases. The primary current $I_P$ is suppressed as analyzed at the beginning of Section III. The switch voltage across $S_2$ and the corresponding gate driver waveforms are presented in Fig. 13(b). However, when compared with the switching voltage in Fig. 12(b), a part of the theoretically high voltage becomes zero, which means there is extra current passing through the parallel and parasite diode of $S_2$, which decreases the voltage to zero. In addition, the distortion of the switching voltage is obvious and the zero level is unstable. Experimentally, to detect and measure this error state, the system is put into the AST state repeatedly, resulting in a breakdown where three diodes ($D_{S2}$, $D_{S4}$, $D_{S4}$) are shorted out. The observed waveforms verify the presented analysis.

In the experiment, the RMS value of the input current is obtained from the dc source set at 100 V. The system efficiency is measured based on Equ. (41). The input power and efficiency under the PSC and the AVC are depicted in Fig. 14. As can be seen, the input power of the PSC is larger than that of the AVC since the PSC can generate a larger voltage amplitude with the same ST duty ratio as analyzed in Equs. (18) and (19). The power drop is more obvious when the impedance deviates from pure resistance or when the AST state occurs. On the other hand, the efficiency of the AVC is higher than that of the PSC which verifies the AVC advantage stated in [22], [27]. However, this efficiency decreases more quickly. One reason is that the capacitor range of the AVC is smaller than that of the PSC. Therefore, the system under the AVC has a greater possibility to enter the AST state first when $C_P$ increases. After the AST state occurs, the efficiency decreases more obviously when compared with the decrement before the breakdown occurs. Moreover, when $C_P$ increases, the efficiency of the AVC decreases more quickly due to the THD value increasing more quickly and becoming larger as mentioned in Section III and analyzed in Section IV.

## VI. Conclusions

This paper applied a ZSI into a WPT system and presented the AST problem caused by resonant network mismatch. A mathematical analysis was carried out to show that this problem does not occur when the equivalent impedance, as seen by the ZSI, is purely resistive. However, when the equivalent load is adjusted to be inductive or capacitive, the ZSI may enter the AST state. This state can increase the THD value, and decrease the input power and system efficiency. To address this problem, this paper proposed to maintain the resonant current amplitude $I_{Pm}$ at less than twice the current through inductors in the Z-source network ($2\bar{I}_L$). To realize this requirement, the primary compensation capacitance, which is usually used to adjust the equivalent impedance, should be limited to a certain range, which was discussed in this paper based on different control algorithms when the impedance is inductive. From the range limitation, it can be concluded that small inductance coils, a small quality factor and a large mutual inductance can help the ZSI be less sensitive to load variation and to address the AST state. Simulations and experimental results verified the analysis and the correctness of the calculated capacitance range.

## Acknowledgment

This work was supported by United Foundation of NSFC-Henan (U1604136). The authors would like to thank the associate editor and the peer reviewers for their valuable suggestions which significantly improve the quality of this paper.

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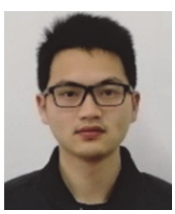

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