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Shunt Active Filter for Multi-Level Inverters Using DDSRF with State Delay Controller

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Abstract

The traditional power control theories for the harmonic reduction methods in multilevel inverters are found to be unreliable under unbalanced load conditions. The unreliability in harmonic mitigation is caused by voltage fluctuations, non-linear loads, the use of power switches, etc. In general, the harmonics are reduced by filters. However, such devices are an expensive way to provide a smooth and fast response to secure power systems during dynamic conditions. Hence, the Decoupled Double Synchronous Reference Frame (DDSRF) theory combined with a State Delay Controller (SDC) is proposed to achieve a harmonic reduction in power systems. The DDSRF produces a sinusoidal harmonic that is the opposite of the load harmonic. Then, it injects this harmonic into power systems, which reduces the effect of harmonics. The SDC is used to reduce the delay between the compensation time for power injection and the generation of a reference signal. The proposed technique has been simulated using MATLAB and its reliability has been verified experimentally under unbalanced conditions.

Key words: Cascaded multi-level inverter, Decoupled double synchronous reference frame, Instantaneous PQ theory, Positive, Negative and zero sequence components, Shunt active filter, State delay controller

I. INTRODUCTION

Recently, power quality problems have been aggravated due to the introduction of power electronic equipment in industrial and domestic products. Since power electronic circuits exhibit non-linear characteristics, they induce both harmonics and distortions of the voltage and current in power system networks. This can result in a poor power factor, active and reactive power problems, electromagnetic interference, poor efficiency, heating of the equipment and conductors, and increased line losses. These problems affect the longevity of power system components. To suppress the harmonic components in power systems, various filtering techniques have been widely used in recent years [1], [2]. These filters can be active or passive. The active filters include the series active and Shunt Active Filters (SAF). Meanwhile, the passive filters are based on components used for filtering.

Series filters provide a high impedance to the harmonic currents. However, they allow the fundamental frequency of the current to reach the supply voltage. Shunt active filters provide a low impedance path for harmonic currents, and divert harmonics to the ground [3]. Shunt filters are less expensive when compared to series filters since they do not carry the full load current. Passive filters are comparatively bulky and are not economical at high power ratings. Hence, there is a need for precise fine tuning to reduce harmonic currents over a wide range of the frequency spectrum. The Fourier transformation method is widely employed to solve frequency domain characteristics [4]. Many researchers and industrialists have implemented shunt active power filters to compensate for power system harmonics by injecting the required component to retain the balanced voltage and current profile [5]-[9]. In the extraction of harmonics from an unbalanced system with a non-linear load, the reference signal plays a significant role. A targeted output is achieved by controlling the DC link voltage with suitable switching pulses to the inverter circuit.

Three-phase power systems have distorted power content and harmonics. The Synchronous Reference Frame (SRF) theory was implemented by a Phase Locked Loop (PLL) and its performance was unsatisfactory under unbalanced and

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severely distorted conditions [10], [11]. Hence, the authors of this paper proposed a decoupled double synchronous reference frame theory, to detect the positive, negative and zero sequence components of the power consumed by non-linear loads and sources [12]. This theory overcomes the above mentioned drawbacks and gives an accurate estimation of all the sequences of components without a reduction of the bandwidth. The rotating double synchronous reference frame generates the signals of dq_1 and dq_2 from αβ and they are translated into β, which is equal to zero.

In addition, the harmonic losses are estimated under an unbalanced load to generate a reference signal for injecting adequate compensating power into the grid. To warrant a precise compensation from unbalanced source and load distortions, a discrete PID controller is used to provide the feedback of the decoupling block. Thus, an exact gating signal has been provided to a Five Level Cascaded – Multi Level Inverter (FLC-MLI) circuit with feedback.

II. Re-Examination of the Instantaneous Power Theory and Unbalanced Conditions

A. Unbalanced Source and Power

In three-phase unsymmetrical power systems, equations that represent the zero, positive and negative sequences of the components are:

$$\begin{bmatrix} V_{as} \\ V_{bs} \\ V_{cs} \end{bmatrix} = V_0 \begin{bmatrix} y(\omega t + \varphi_0) \\ y(\omega t + \varphi_0) \\ y(\omega t + \varphi_0) \end{bmatrix} + V_1 \begin{bmatrix} y(\omega t + \varphi_1) \\ y\left(\omega t - \frac{2\pi}{3} + \varphi_1\right) \\ y\left(\omega t + \frac{2\pi}{3} + \varphi_1\right) \end{bmatrix} + V_2 \begin{bmatrix} y(\omega t + \varphi_2) \\ y\left(\omega t + \frac{2\pi}{3} + \varphi_2\right) \\ y\left(\omega t - \frac{2\pi}{3} + \varphi_2\right) \end{bmatrix} \quad (1)$$

where:

$y -$ cos

$\omega t -$ angular frequency

V_{as}, V_{bs}, V_{cs} – supply voltages of phases a, b, c

$V_1, V_2, V_0 -$ positive, negative and zero sequence voltages

$\varphi_1, \varphi_2, \varphi_0 -$ positive, negative and zero sequence angles

V_0, V_1 and V_2 are the peak values of the unsymmetrical voltage components, which can be simplified as:

$$V_s = \begin{bmatrix} V_{as} \\ V_{bs} \\ V_{cs} \end{bmatrix} = \begin{bmatrix} V_{a0} \\ V_{b0} \\ V_{c0} \end{bmatrix} + \begin{bmatrix} V_{a1} \\ V_{b1} \\ V_{c1} \end{bmatrix} + \begin{bmatrix} V_{a2} \\ V_{b2} \\ V_{c2} \end{bmatrix} \quad (2)$$

Similarly, the unsymmetrical source current component is represented as:

$$I_s = \begin{bmatrix} I_{as} \\ I_{bs} \\ I_{cs} \end{bmatrix} = \begin{bmatrix} I_{a0} \\ I_{b0} \\ I_{c0} \end{bmatrix} + \begin{bmatrix} I_{a1} \\ I_{b1} \\ I_{c1} \end{bmatrix} + \begin{bmatrix} I_{a2} \\ I_{b2} \\ I_{c2} \end{bmatrix} \quad (3)$$

V_s – supply voltage

I_s - supply current

V_{a1}, V_{a2}, V_{a0} – positive, negative and zero sequence voltages of phase 'a'

Similarly, V_{b1}, V_{b2}, V_{b0} and V_{c1}, V_{c2}, V_{c0} are the sequence voltages of phases 'b' and 'c'

I_{as}, I_{bs}, I_{cs} – supply current of phases a, b, c

I_{a1}, I_{a2}, I_{a0} – positive, negative and zero sequence currents of phase 'a'

Similarly, I_{b1}, I_{b2}, I_{b0} and I_{c1}, I_{c2}, I_{c0} are the sequence currents of phase 'b' and 'c'

In general, the apparent power of the source is:

$$S_s = P_s + j\,Q_s = V_s I_s^* \quad (4)$$

where:

$S_s -$ apparent power of the source

$P_s -$ real power of the source

$Q_s -$ reactive power of the source

According to the instantaneous PQ theory from Fig.1, the power balancing equation is:

$$S_{s120} = S_{l120} + S_{f20} \quad (5)$$

The subscripts 1, 2 and 0 indicate the positive, negative and zero sequence components. S_{s120} is the apparent power of the supply source connected in the non-linear load condition. S_{l120} is the total power consumed by the non-linear load, and S_{f20} is the total power injected by the shunt active power filter under source and non-linear loads. Hence, the effective value of the unbalanced power is determined on both sides of the source and load. Therefore, the SAF required to inject the grid power is determined by:

$$S_{l120} = S_{s120} + S_{h120} \quad (6.a)$$

$$S_{l120} = p_{s120}(t) + q_{s120}(t) + p_{h120}(t) + q_{h120}(t) \quad (6.b)$$

where, S_{h120} is the harmonic power loss component due to the non-linear load. p_{s120} and q_{s120} are the active and reactive powers of the load consumed from the source. $p_{h120}(t)$ and $q_{h120}(t)$ are the real and reactive power losses of the load harmonics component.

B. Fundamental Transform Theory

The proposed method of a DDSRF based instantaneous PQ theory with a state delay control technique for the five level cascaded multilevel inverter configurations in a SAF is given in Fig. 1.

The proposed DDSRF theory transforms an unbalanced three-phase power abc into αβ0 using Clark's transformation theory.

$$V_{\alpha\beta 0} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} V_s \quad (7)$$

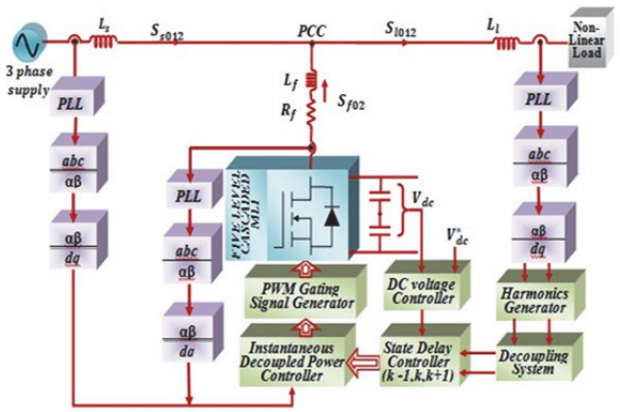


Fig. 1. Proposed DDSRF-PQ with SDC for a FLC-MLI SAF.

$$I_{\alpha\beta0} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} I_s \quad (8)$$

where:

$V_{\alpha\beta0}$, $I_{\alpha\beta0}$ – Clark's transformation voltage and current of the alpha, beta and zero components.

The αβ origination describes the instantaneous voltage vector by considering the positive sequence reference. It can be obtained by neglecting the zero-sequence component of the voltage vector in αβ0.

$$V_{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} V_s \quad (9)$$

$$I_{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} I_s \quad (10)$$

From Equ. (4), using the instantaneous power theory, the real and imaginary power (pq) of the stationary reference is obtained as follows:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (11)$$

The resultant voltage in the αβ reference frame is determined from:

$$V_{\alpha\beta} = V_1 \begin{bmatrix} \cos(\omega t + \varphi_1) \\ \sin(\omega t + \varphi_1) \end{bmatrix} + V_2 \begin{bmatrix} \cos(-\omega t + \varphi_2) \\ \sin(-\omega t + \varphi_2) \end{bmatrix} \quad (12)$$

III. DDSRF Power Theory

A. Decoupled Double SRF Theory in PQ Calculation

The angular frequency of the rotating coordinate system is same as the frequency of the voltage vector in the stationary reference frame. The state of the decoupled double synchronous rotating reference frame is derived from a Park's transformation by separating the positive and negative sequence components. The transformed dq_{12} is given by:

$$V_{dq1} = V_{\alpha\beta} \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \quad (13a)$$

$$V_{dq2} = V_{\alpha\beta} \begin{bmatrix} -\cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & -\cos(\omega t) \end{bmatrix} \quad (13b)$$

From Equ. 13a and Equ. 13b, it can be concluded that:

$$V_{dq1} = -V_{dq2} \quad (14)$$

$$V_{dq1} = V_1 \begin{bmatrix} \cos(\varphi_1) \\ \sin(\varphi_1) \end{bmatrix} + V_2 \begin{bmatrix} \cos(\varphi_2) & \sin(\varphi_2) \\ -\sin(\varphi_2) & \cos(\varphi_2) \end{bmatrix} \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} \quad (15)$$

$$V_{dq1} = V_1 \begin{bmatrix} \cos(\varphi_1) \\ \sin(\varphi_1) \end{bmatrix} + V_{d2} \begin{bmatrix} \cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix} + V_{q2} \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \quad (16)$$

$$V_{dq2} = V_2 \begin{bmatrix} \cos(\varphi_2) \\ \sin(\varphi_2) \end{bmatrix} - V_{d1} \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} + V_{q1} \begin{bmatrix} \sin(2\omega t) \\ -\cos(2\omega t) \end{bmatrix} \quad (17)$$

Equ. 16 and Equ. 17 represent the positive and negative sequences from the Park's transformation. By substituting the decoupled voltage and current values obtained from the Park's transformation, the following instantaneous PQ theory equations are obtained:

$$P_1 = \frac{3}{2}\begin{bmatrix} v_{d1} & -v_{q1} & -v_{d2} & v_{q2} \end{bmatrix} \begin{bmatrix} i_{q2} \\ i_{d2} \\ i_{q1} \\ i_{d1} \end{bmatrix}$$

$$Q_1 = P_2 = \frac{3}{2}\begin{bmatrix} v_{d1} & v_{q1} & v_{d2} & v_{q2} \end{bmatrix} \begin{bmatrix} i_{d2} \\ i_{q2} \\ i_{d1} \\ i_{q1} \end{bmatrix}$$

$$Q_2 = \frac{3}{2}\begin{bmatrix} v_{d1} & -v_{q1} & v_{q2} & -v_{d2} \end{bmatrix} \begin{bmatrix} i_{q2} \\ i_{d2} \\ i_{d1} \\ i_{q1} \end{bmatrix} \quad (18)$$

The reference signal generated from the decoupled voltage and current is given by:

$$P_0 = \frac{3}{2}\begin{bmatrix} v_{d1} & -v_{q1} & -v_{d2} & v_{q2} \end{bmatrix} \begin{bmatrix} i_{q2} \\ i_{d2} \\ i_{q1} \\ i_{d1} \end{bmatrix}$$

$$Q_0 = P_2 = \frac{3}{2}\begin{bmatrix} v_{d1} & v_{q1} & v_{d2} & v_{q2} \end{bmatrix} \begin{bmatrix} i_{d2} \\ i_{q2} \\ i_{d1} \\ i_{q1} \end{bmatrix} \quad (19)$$

where:

V_{d1}, V_{d2} - direct axis voltages for the positive and negative sequence components

V_{q1}, V_{q2} - quadrature axis voltages for the positive and negative sequence components

The positive sequence component in the q axis contains oscillations. To reduce these oscillations, a digital controller is implemented by providing the feedback angular frequency in terms of 'θ' angular error for the decoupling mechanism. The main advantage of the DDSRF when compared to the traditional SRF-PLL is that there is no need to limit the

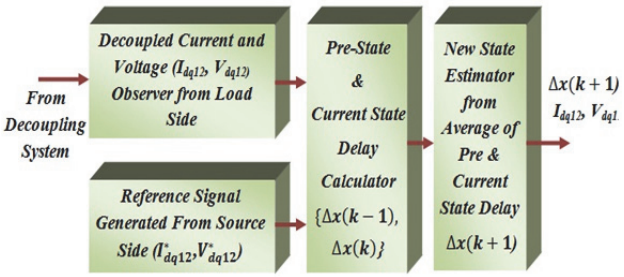


Fig. 2. State Delay Controller (SDC).

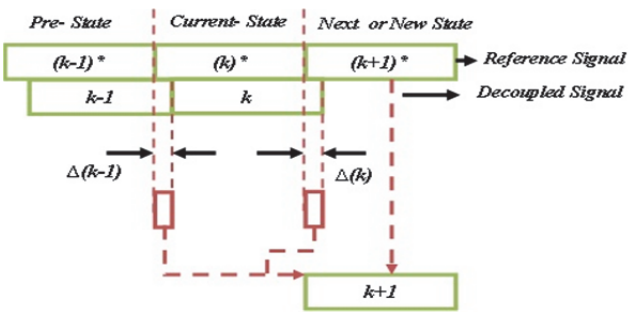


Fig. 3. New state calculation signal diagram.

bandwidth of the PLL to cancel out higher order oscillations [13], [14], [16]-[18]. A Low Pass Filter (LPF) has been implemented to suppress the higher order oscillations in the signal.

B. State Delay Controller

There is a phase delay in the LPF output for producing the signal, due to the unbalanced condition of the operation. To eliminate the phase delay error, fine tuning is required in the entire system [15], [19].

The pre-state determination method, which is called a state delay controller (SDC), was introduced from the current state PQ calculations as shown in Fig. 2. In addition, Equ. (20) explains the procedure for the delay calculations.

The pre-state time is considered as (k-1) and the current state is considered as (k). The next sample signal time is expressed as the (k+1) state as shown in Fig. 3.

The following equation is used to calculate the next-state:

$$\Delta x(k-1) = x(k-1)^* - x(k-1)$$

Current state : $\Delta x(k) = x(k)^* - x(k)$

$$\left.\begin{matrix}\text{Next state}\\ \text{or}\\ \text{New state}\end{matrix}\right\}: \quad \Delta x(k+1) = \frac{\Delta x(k-1) + \Delta x(k)}{2} \qquad (20)$$

where, $x = V_{dq12}, I_{dq12}$ is the decoupled voltage and current.

The error or delay time of the new state (k+1) is determined by the average of the pre-state sample (k-1) when compared to the reference (k-1)* delay, the current state sample (k) and the reference (k)* delay. The voltage and current profile of the positive and negative sequence is calculated, and these values are used to cancel out the signal delay error from the reference to the SAF output.

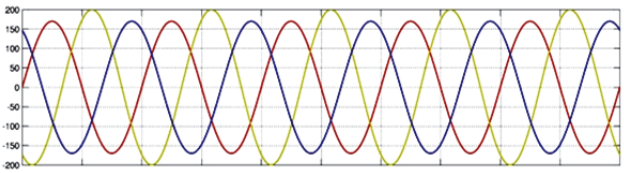


Fig. 4. Three-phase source waveform before the compensation voltage of phase 'abc'.

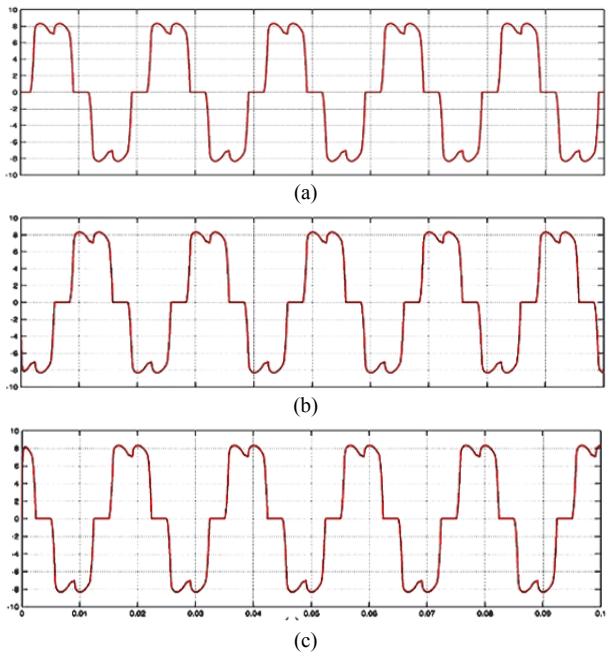


Fig. 5. Three Source current-waveform before compensation. (a) Phase 'a' current. (b) Phase 'b' current. (c) Phase 'c' current.

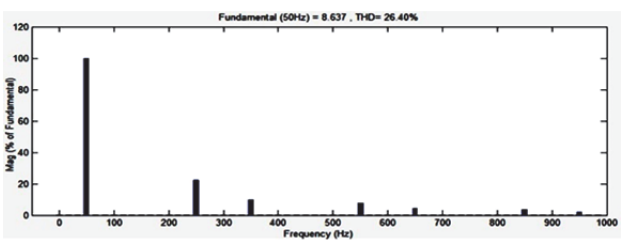


Fig. 6. Current spectrum and harmonics before compensation.

IV. Experimental Results and Discussions

The proposed DDSRF was simulated using MATLAB/ Simulink and was found to be reliable under unbalanced condition.

From Figs. 4-5, it is inferred that an effective ruling method is required to change the non-linear character of the source and the load.

To validate the proposed SAF algorithm a hardware prototype was built using the five level cascaded multi-level inverter structure. The unbalanced load consists of a three-phase diode rectifier circuit and has a Total Harmonic Distortion (THD) of 26.40% without the SAF as shown in Fig. 6.

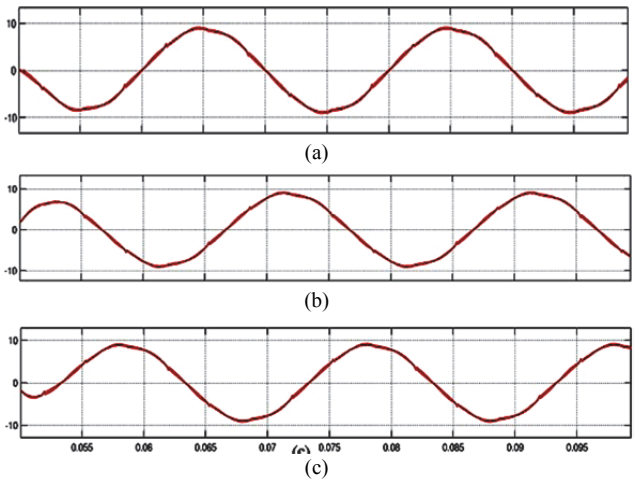


Fig. 7. Three-phase load current phase with the SAF compensation. (a) Current of phase 'a.' (b) Current of phase 'b.' (c) Current of phase 'c'.

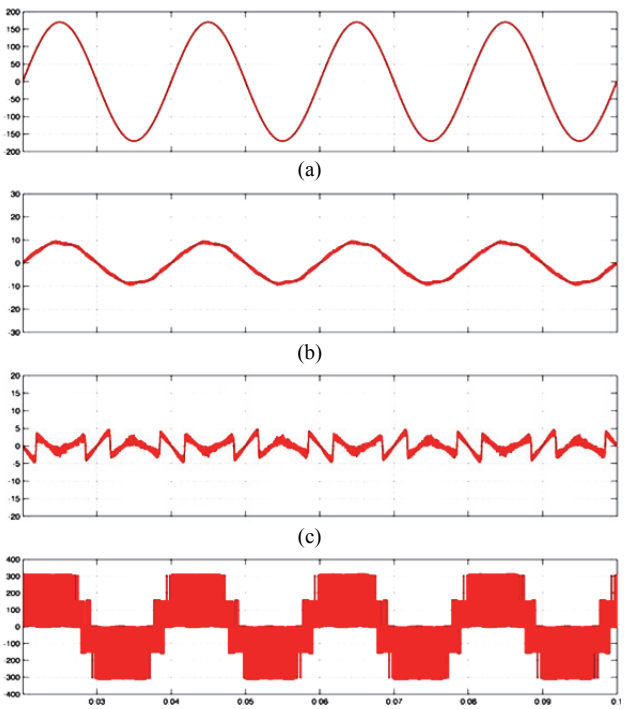


Fig. 8. Unbalanced load compensation performance with the SAF of phase 'a.' (a) Load voltage. (b) Load current. (c) Injected current from the SAF. (d) FLC-MLI output voltage.

The load current and source current with voltage components were shown in Figs. 7-10. Using the DDSRF with the time delay controller technique, the value of the THD was reduced to 1.62%.

Figs. 4-10 show simulated diagrams of the SAF. The performances are compared with an unbalanced load both with and without the SAF.

Figs. 11-13 show unbalanced three phase source voltage and current profiles with the current harmonics THD of phase 'a.'

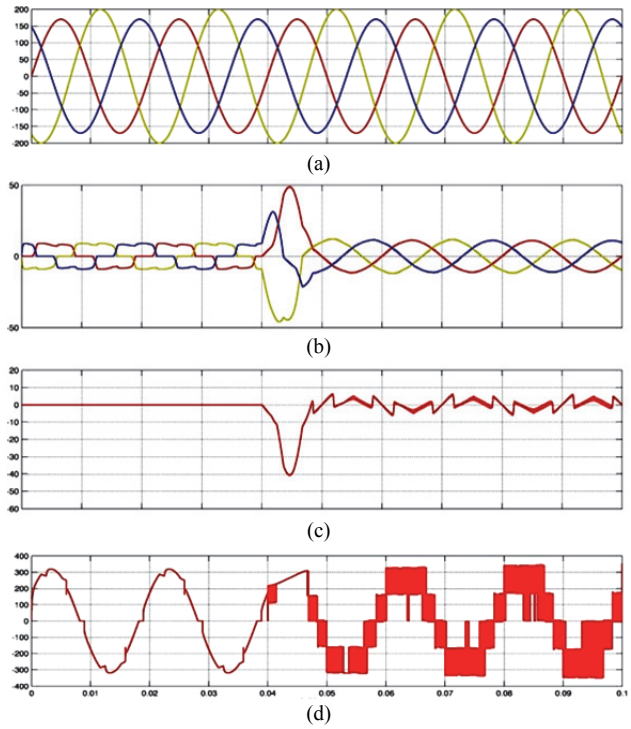


Fig. 9. Three-phase load and with the FLC-MLI based SAF compensation under transient operation at t = 0.04s. (a) Source voltage. (b) Source current. (c) Injected current from the SAF. (d) FLC-MLI output voltage.

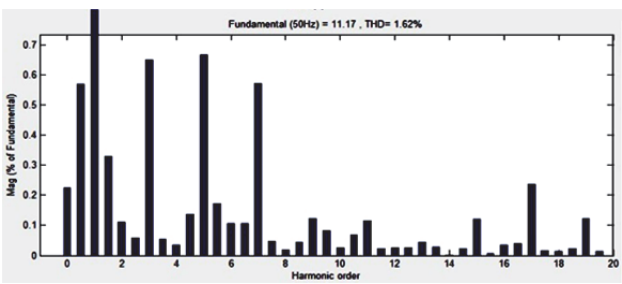


Fig. 10. THD spectrum of the load current after compensation.

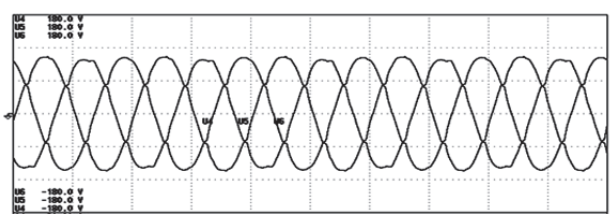


Fig. 11. Unbalanced three-phase source voltage and current of phase 'abc.'

The magnitude of the phase and line voltages of an unbalanced load are measured and tabulated in Fig.14. The load current THD is at its minimum (24.785%) in phase 'c' and at its maximum (26.143%) in phase 'a' without the injection of compensation current in the PCC or without the connection of the SAF. In the unbalanced load condition, the maximum values of the P and Q components are 410.22W and 127.43W, respectively. Under the same conditions, the

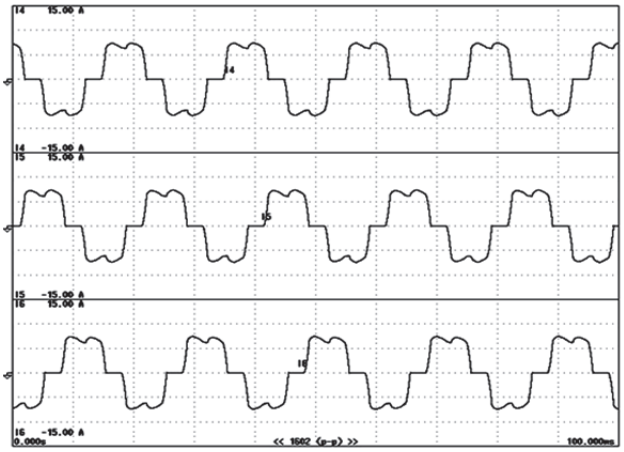


Fig. 12. Three-phase source current of phase 'abc.'

Fig. 13. Source current harmonics spectrum of phase 'a.'

8 change items

		Element 1	Element 2	Element 3	Element 4	Element 5	Element 6
Urms	[V]	123.81	126.67	125.63	71.816	73.529	74.266
Irms	[A]	0.0350	0.0000	0.0323	5.647	5.659	5.756
P	[W]	-0.0007k	-0.0003k	-0.0017k	-389.23	-399.40	-410.22
S	[VA]	0.0043k	0.0000k	0.0040k	407.21	417.85	429.56
Q	[var]	0.0042k	0.0000k	0.0036k	-119.66	-122.80	-127.43
λ	[ ]	-0.1682	Error	-0.4152	-0.9559	-0.9558	-0.9550
S	[VA]	0.0043k	0.0000k	0.0040k	407.21	417.85	429.56
Uthd	[%]	4.949	5.057	5.598	4.218	4.051	3.875
Ithd	[%]	92.578	93.674	91.047	26.143	25.650	24.785

Fig. 14. Three-phase load (L-L) and phase values without the SAF.

minimum values of the P and Q components are 389.23W and 119.66W, respectively. The current waveform is distorted and it consumed more reactive power. In order to reduce the harmonics in an unbalanced source and load, compensation power is injected at the junction of the Point of Common Coupling (PCC).

Fig. 14 and Fig. 17 show numerical values of the voltage, current, active power, reactive power, apparent power, voltage THD and current THD with and without the SAF. These values were obtained from a power quality analyzer.

From Figs. 15-17, it is evident that the harmonic components are considerably reduced by using the DDSRF algorithm with the time delay prediction of the dq1 and dq2 components of the positive and negative sequence PQ powers

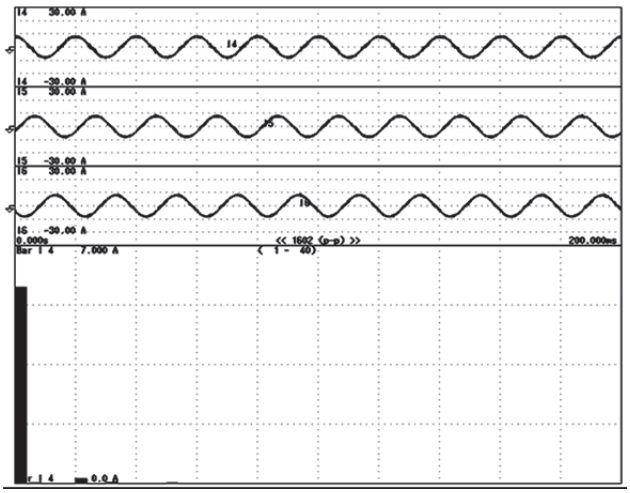
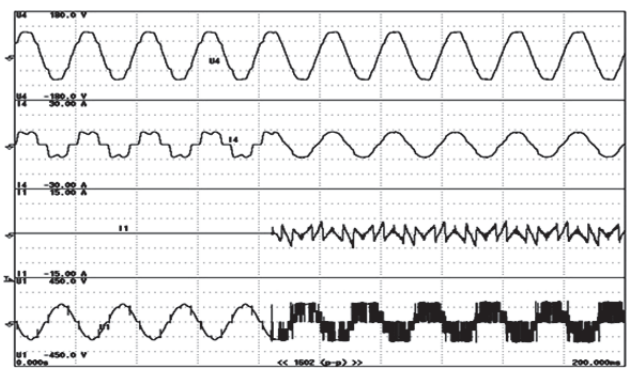
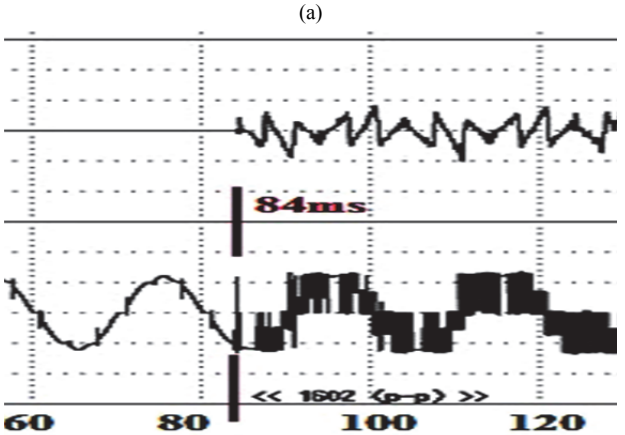


Fig. 15. Three-phase load currents of phases a, b, c and the harmonics spectrum of the phase 'a' load current (with the SAF compensation).



(a)



(b)

Fig. 16. The load voltage and load current before compensation. (a) Load voltage and current, FLC-MLI based SAF compensation current and voltage under transient operating conditions at 84ms. (b) Expanded view at 84ms.

consumed by the unbalanced load. The harmonics are reduced to 1.425% in phase 'c', which is less than the standard value recommended by IEEE. Fig. 16.(a) shows the load voltage and load current before compensation, compensation current and voltage of the SAF under transient

8 change items

		Element 1	Element 2	Element 3	Element 4	Element 5	Element 6
Urms	[V]	154.68	154.74	153.10	73.52	74.07	74.72
Irms	[A]	3.0113	3.0856	2.8030	11.333	12.358	12.024
P	[W]	-0.0589k	-0.1325k	-0.0643k	0.8288k	0.9092k	0.8955k
S	[VA]	0.4149k	0.4288k	0.3872k	0.8326k	0.9133k	0.8980k
Q	[var]	0.4107k	0.4078k	0.3818k	-0.0788k	-0.0868k	0.0664k
λ	[ ]	-0.1420	-0.3090	-0.1660	0.9955	0.9955	0.9973
S	[VA]	0.4149k	0.4288k	0.3872k	0.8326k	0.9133k	0.8980k
Uthd	[%]	20.708	23.014	21.211	3.090	2.266	2.174
Ithd	[%]	91.460	82.980	93.281	2.110	1.938	1.898

Fig. 17. Three-phase load L-L and phase values with SAF injected at 84ms.

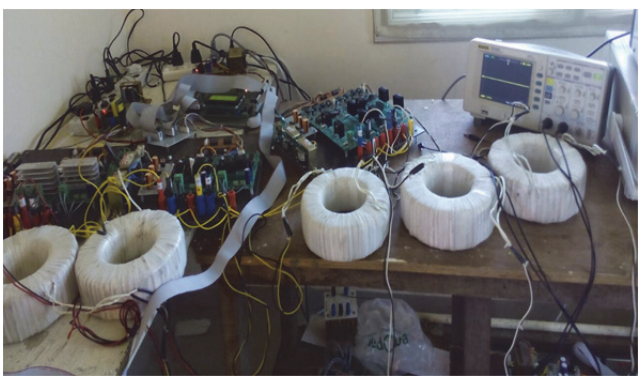


Fig. 18. Experimental setup.

conditions at 84ms. The SAF achieves unbalanced load operation in the transient operating condition. The SAF is tested in the transient condition at 84ms, and the results are shown in Figs. 16(a)-17.

It is observed from Fig. 16 and Fig. 17 that the oscillations in the current waveform are cancelled out when the SAF is connected at 84ms. At this instant, the THD component of the load current is 2.11% and the load voltage is 3.09%. With the SAF, the power consumption is drastically reduced in the proposed system when compared to the unbalanced state operation without the SAF.

An experimental setup of the shunt active filter for a multi-level inverter is shown in Fig 18. The three phase source voltages and dc-link voltages are sensed by a Hall effect voltage sensor (LV25-P), and the three phase source current, load current and filter current are sensed by a Hall effect current sensor (LA25-P), along with three iron core inductors (5mh/15A) that are used as filters. The switching signals for the Insulated-Gate Bipolar Transistors (IGBT-FGA40N120) are derived from the SRF theory. A driver circuit (TLP250IC) is used to drive the Pulse Width Modulation (PWM) pulses to the inverter. For the isolation of the inverter output voltage from the power circuit of the SAF, six toroidal core transformers are used in the hardware setup.

The SRF algorithm has been implemented using a Spartan 6 Field-Programmable Gate Array (FPGA) processor. FPGA technology is suitable for a wider range of applications. The Spartan 6 FPGA controller generates and controls the PWM pulses for the inverter [20]. The FPGA architecture is designed on the basis of the control algorithm. The output results are displayed on a CRO/Power quality analyzer to view the voltage and current waveforms.

V. Conclusion

The DDSRF mathematical models for a cascaded H-bridge five level multilevel inverter have been simulated using MATLAB. The unbalanced condition of the DDSRF with a state delay controller in the instantaneous PQ theory was successfully analyzed. The delay time from the current state sampling time to the next state has effectively increased the speed of the reference signal generation. The transient state operation of the FLC-MLI based SAF was tested under different conditions. It performed satisfactorily under normal operation with a quick frequency response. In addition, it is proved to be the most reliable method. In the proposed method, the maximum value of % THD of voltage and % THD of current are 2.823 and 2.065, respectively. These values are lower than the IEEE standard values.

References

[1] B. Singh, K. Al-Haddad, and A. Chandra, "A review of active filters for power quality improvement," *IEEE Trans. Ind. Electron.*, Vol. 46, No. 5, pp. 960-971, 1999.

[2] F. Blaabjerg, R. Teodorescu, M. Liserre, and A.V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, Vol. 53, No. 5, pp. 1398-409, Oct. 2006.

[3] M. Ucar, S. Özdemir, and E. Özdemir, "A unified series-parallel active filter system for nonperiodic disturbances," *Turkish J. Electr. Eng. Comp. Sci.*, Vol. 19, No. 4, pp. 575-596, Jun. 2011.

[4] R. Arseneau, Y. Baghzouz, J. Belanger, K. Bowes, A. Braun, A. Chiaravallo, M. Cox, S. Crampton, A. Emanuel, P. Filipski, and E. Gunther, "Practical definitions for powers in systems with non-sinusoidal waveforms and unbalanced loads: a discussion," *IEEE Trans. Power Del.,* Vol. 11, No.1, pp. 79-101, Jan. 1996.

[5] S. A. González, R. García-Retegui, and M. Benedetti, "Harmonic computation technique suitable for active power filters," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 5, pp. 2791-2796, Oct. 2007.

[6] K. R. Uyyuru, M. K. Mishra, and A. Ghosh, "An optimization-based algorithm for shunt active filter under distorted supply voltages," *IEEE Trans. Power Electron.*, Vol. 24, No. 5, pp. 1223-1232, May 2009.

[7] P. Garanayak, and G. Panda, "Harmonic elimination and reactive power compensation with a novel control algorithm based active power filter," *J. Power Electron.*,

Vol. 15, No. 6, pp. 1619-1627, Nov. 2015.
[8] C. Zhang, M. Gong, Y. Zhang, and Y. Li, "Multiple-period repetitive controller for selective harmonic compensation with shunt active power filter," *J. Power Electron.*, Vol. 15, No. 3, pp. 819-829, May 2015.
[9] Y. Wang, Y.-X. Xie, and X. Liu, "Analysis and design of dc-link voltage controller in shunt active power filter," *J. Power Electron.,* Vol. 15, No. 3, pp. 763-774, May 2015.
[10] M. K. Mishra, A. Ghosh, A. Joshi, and H. M. Suryawanshi, "A novel method of load compensation under unbalanced and distorted voltages," *IEEE Trans. Power Del.*, Vol. 22, No. 1, pp. 288-295, Jan. 2007.
[11] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R.P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electron.*, Vol. 22, No. 2, pp. 584-592, Mar. 2007.
[12] E. Sundaram and M. Venugopal, "On design and implementation of three phase three level shunt active power filter for harmonic reduction using synchronous reference frame theory," *Electr. Power Energy Syst.*, Vol. 81, pp. 40-47, Feb. 2016.
[13] J. S. Kim and Y. S. Kim, "A new control method for a single-phase hybrid active power filter based on a rotating reference frame," *J. Power Electron.*, Vol. 9, No. 5, pp. 718-25, Sep. 2009.
[14] H. H. Tumbelaka, L. J. Borle, C.V. Nayar, and S. R. Lee, "A grid current-controlling shunt active power filter," *J. Power Electron.*, Vol. 9, No. 3, pp. 365-76, May 2009.
[15] J. H. Lee, J. K. Jeong, B. M. Han, and B. Y. Bae, "New reference generation for a single-phase active power filter to improve steady state performance," *J. Power Electron.*, Vol. 10, No. 4, pp. 412-418, Jul. 2010.
[16] M. Adel, S. Zaid, and O. Mahgoub, "Improved active power filter performance based on an indirect current control technique," *J. Power Electron.*, Vol. 11, No. 6, pp. 931-937, Nov. 2011.
[17] Y. Han and L. Xu, "Design and implementation of a robust predictive control scheme for active power filters," *J. Power Electron.*, Vol. 11, No. 5, pp. 751-758, Sep. 2011.
[18] L. Zhou, M. Yang, Q. Liu, and K. Guo, "New control strategy for three-phase grid-connected LCL inverters without a phase-locked loop," *J. Power Electron.*, Vol. 13, No. 3, pp. 487-96, May 2013.
[19] Q. N. Trinh and H. H. Lee, "Advanced repetitive controller to improve the voltage characteristics of distributed generation with nonlinear loads," *J. Power Electron.*, Vol. 13, No. 3, pp. 409-18, May 2013.
[20] C. Siluvaimuthu and V. Chenniappan, "A low-cost reconfigurable field-programmable gate array based three-phase shunt active power filter for current harmonic elimination and power factor constraints," *Electr. Power Compon. Syst.*, Vol. 42, No. 16, pp. 1811-1826, Nov. 2014.

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