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Optimized Low-Switching-Loss PWM and Neutral-Point Balance Control Strategy of Three-Level NPC Inverters

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Abstract

Power loss reduction and total harmonic distortion(THD) minimization are two important goals of improving three-level inverters. In this paper, an optimized pulse width modulation (PWM) strategy that can reduce switching losses and balance the neutral point with an optional THD of three-level neutral-point-clamped inverters is proposed. An analysis of the two-level discontinuous PWM (DPWM) strategy indicates that the optimal goal of the proposed PWM strategy is to reduce switching losses to a minimum without increasing the THD compared to that of traditional SVPWMs. Thus, the analysis of the two-level DPWM strategy is introduced. Through the rational allocation of the zero vector, only two-phase switching devices are active in each sector, and their switching losses can be reduced by one-third compared with those of traditional PWM strategies. A detailed analysis of the impact of small vectors, which correspond to different zero vectors, on the neutral-point potential is conducted, and a hysteresis control method is proposed to balance the neutral point. This method is simple, does not judge the direction of midpoint currents, and can adjust the switching times of devices and the fluctuation of the neutral-point potential by changing the hysteresis loop width. Simulation and experimental results prove the effectiveness and feasibility of the proposed strategy.

Key words: Hysteresis loop, Neutral-point balance, Switching losses, Three-level inverter, Zero vector

I. INTRODUCTION

The three-level neutral-point-clamped (NPC) inverter is applied extensively in many fields. This topology switches with barely half of the working voltage of two-level inverters and can output a five-level-step-shaped line-to-line voltage without transformers or reactors [1]. With more voltage steps, it can reduce the harmonics in both output voltage and current [2]. Therefore, the three-level NPC inverter is more suitable for high-power application fields than the traditional two-level inverter. However, these inverters also have disadvantages, and the unbalanced capacitor voltage in the DC side is one of the worst ones because it seriously affects operation reliability and performance. The switching losses of devices increase significantly with the inverter capacity and switching frequency. Therefore, the reduction of switching losses of inverters has received significant attention.

As shown in [3] and [4], the discontinuous pulse width modulation (DPWM) strategy keeps one phase switch inactive and two other phase switches active in a certain sector in two-level inverters. This strategy can reduce the switching losses significantly and improve the conversion efficiency compared with the continuous PWM strategy. However, it has more vector redundancy and a more complicated modulation strategy in three-level NPC inverters. To simplify the modulation algorithm of three-level inverters, a simplified strategy was proposed in [5]. The space vector graph of the three-level inverter can be divided into six two-level space vector graphs through vector transformation, and the complexity of the three-level strategy is simplified to the same level as the two-level strategy [6]. However, the switching

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losses under this method are still high. To solve this problem, some strategies and analyses were proposed in [7]-[12]. In [7], the switching performance of the high-power high-frequency three-level active NPC phase was optimized to analyze the switching characteristics. An optimized discontinuous PWM method was proposed in [8] to minimize the switching loss for multilevel inverters. The influence of the modulation method on the switching losses of PWM converters was illustrated in [9], and for PWM voltage source converters, the switching loss optimized PWM strategies were analyzed in [10]. The DPWM and space vector modulation for three-level NPC converters were studied in [11] and [12], respectively, to analyze their effects on switching loss reduction. According to these studies, DPWM has a significant effect on the reduction of switching losses. A DPWM based on the circuit-level decoupling concept was proposed in [13] for three-level NPC inverters by comparing the absolute values of the three phase modulation waves and making the phase with the highest voltage inactive. A DPWM method was introduced to balance the neutral point voltage in the three-level inverter-fed variable frequency drives in [14]. The time-domain DPWM proposed in [15] was studied in the over modulation region to analyze its special use. Similarly, a discontinuous space-vector modulation for three-level PWM rectifiers was investigated in [16]. To determine the difference in power loss generation, the effects of the continuous and discontinuous PWM schemes on power losses in voltage-sourced inverters were compared in [17], proving the advantages of DPWM in reducing switching losses. Finally, a high-performance generalized DPWM algorithm was presented in [18], and a novel approach for evaluating the performance of DPWM schemes was proposed in [19]. The DPWM strategy can reduce switching losses by one-third by eliminating the conventional zero vector and realizing one goal of improvement. These studies mainly focused on switching loss reduction. However, the performance of the neutral-point balance, which has a direct effect on total harmonic distortion (THD), should be considered because of the special topology of three-level NPC inverters.

To analyze the influence caused by the PWM strategy on the DC-link harmonics of three-phase voltage-source converters, [20] illustrated the PMW principle and its effect on THD. The neutral-point control of a three-level NPC inverter at a high modulation index, including the over-modulation region, under a simple space vector PWM scheme was studied in [21], providing further research on the specific modulation region. [22] proposed a hysteresis-band control with PWM whose neutral-point current direction is obtained by the output current of each phase and PWM group. A neutral-point balancing controller for three-level inverters with a full power-factor range and low distortion was studied in [23], providing further understanding on the specific condition. These control strategies, which consider the current direction, complicate the process of neutral-point control. In [24], the low switching loss and the harmonics PWM for three-phase grid-connected PV inverters were analyzed. In [25], a novel reduced switching loss technique that uses a generalized scalar PWM for nine-switch inverters was proposed and briefly analyzed. An optimal six-segment PWM scheme (Type A) was proposed in [26]. The scheme has a low duty-cycle loss, a maximum output inductor current ripple, and a minimum switching loss compared to other PWM schemes when MOSFET devices are employed. A new power device combination that can reduce the total power loss for a single-phase inverter reduced common-mode noise was proposed in [27]. In the proposed common mode voltage reduction PWM, the half bridge connected to the live end of the single-phase power source performs PWM, and the other half bridge connected to the neutral end commutates with the 60Hz line frequency to reduce the common-mode voltage of a single-phase inverter. In [28], a low-loss, auxiliary zero-voltage-transition (ZVT) circuit was proposed to realize zero-voltage switching (ZVS) for all the main switches of a full bridge inverter and the inherent zero-current-switching (ZCS) turn-on and ZCS turn-off for the auxiliary switches. Similarly, a novel loss balancing modulation strategy, splitting switching loss DPWM strategy, was proposed in [29] to achieve an even loss distribution in the 3L-ANPC converter. In the proposed PWM strategy, the switching-on and switching-off losses are separated to improve the loss distribution among power devices. The proposed strategy and other major PWM strategies for loss distribution are also compared in this paper. [30] proposed a method for varying the switching frequency within a fundamental cycle to reduce the switching losses of a two-level inverter while maintaining the peak-peak current ripple within a predefined limit, providing a reference for the three-level inverters studied in the current work.

The studies above did not combine switching-loss reduction and neutral-point balance control, and some are complex. Therefore, we present a detailed analysis on the nature of DPWM in two-level inverters and the relationship between the two-level and three-level modulation algorithms in Section II. The causes of neutral-point voltage deviation and the effects of small vectors that correspond to different zero vectors on the neutral point are presented in Section III. To reduce the switching losses in three-level inverters and balance the neutral point, this paper proposes a new optimized switching loss PWM and a neutral-point balance control strategy in Section IV. The method simplified from the conventional three-level algorithm is easy to implement. When the rational zero vector is selected, only two-phase switch devices are active in every sector, and the switching losses of the devices can be reduced by one-third. The neutral point voltage can also be placed in a certain loop width through hysteresis control, and the switching times and fluctuation of the neutral point can be changed by changing

the width of the hysteresis loop without judging the neutral-point current direction. The hysteresis control of the neutral-point balance control is presented in Section IV to form an optimized low-switching-loss PWM and the neutral-point balance control strategy. The simulation and experiment are discussed in Section V, and the conclusion is presented in Section VI.

II. TWO DPWM STRATEGIES OF TWO-LEVEL INVERTERS

The DPWM strategy is also known as the bus-bar-clamped PWM. It mainly adds a zero-sequence component in the modulation wave to make its amplitude greater than the positive peak of the triangular carrier wave or less than the negative peak in a certain period. Then, the switching states of corresponding devices remain unchanged in this period, and the switching times and losses decrease significantly compared with those of traditional modulation strategies. The difference between continuous SVPWM and DPWM lies in their distribution of zero vectors, and with only one zero vector is used in a specific sector in DPWM strategies.

A. Zero-Vector Distribution of Continuous SVPWM

In two-level inverters, the states of the upper and lower bridge arm are complementary in each phase. If the upper bridge arm switches on, then the lower bridge arm will switch off; the state of this phase is defined as 1.If the upper bridge arm switches off, then the lower bridge arm switches on; the state of this phase is defined as 0.Then, 2^3=8 voltage vectors exist (expressed by an ordered array such as [000], [001]). Fig. 1 is the voltage space vector diagram of two-level inverters. $\boldsymbol{V}'_{1(100)}$, $\boldsymbol{V}'_{2(110)}$, $\boldsymbol{V}'_{3(010)}$, $\boldsymbol{V}'_{4(011)}$, $\boldsymbol{V}'_{5(001)}$, and $\boldsymbol{V}'_{6(101)}$ are the six basic non-zero vectors; and $\boldsymbol{V}'_{0(000)}$ and $\boldsymbol{V}'_{7(111)}$ are the two zero vectors.

Taking sector I as an example, the switching sequence of the traditional SVPWM is shown in Fig. 2(a) in one switching period, T_0. This mode of distribution is also called the method of dispersing the zero vector. Fig. 2(a) shows that the two zero vectors $\boldsymbol{V}_{0(000)}$ and $\boldsymbol{V}_{7(111)}$ are assigned at two ends, and the center of switching period T_0 makesonly one phase state change at every shift time of the vectors. This mechanism aims to minimize the switching losses. However, the states of the three phases are all changed in one switching period, and they generate large switching losses.

B. Two Zero-Vector Distribution Mechanisms of DPWM

In Fig. 2, two kinds of DPWM switching sequences are presented in one switching period, T_0. Unlike the traditional SVPWM, this zero-vector distribution is centralized. Fig. 2(b) only uses zero vector $\boldsymbol{V}'_{7(111)}$, which is assigned to the middle of each switching period T_0. In sector I, the distribution of the zero vector makes phase A maintain the status 1, and only the states of phases B and C change. The voltage of phase A is clamped to the upper bus of the inverter. By contrast, Fig. 2(c) only uses zero vector $\boldsymbol{V}'_{0(000)}$. This distribution of the zero vector makes phase C maintain the status 0, and only the states of phases A and B change. The voltage of phase C is clamped to the lower bus. Similar results can be obtained in other sectors. Therefore, each of the two switching sequences of DPWM can achieve the target of having the devices active only in two phases, thus reducing switching loss by one-third.

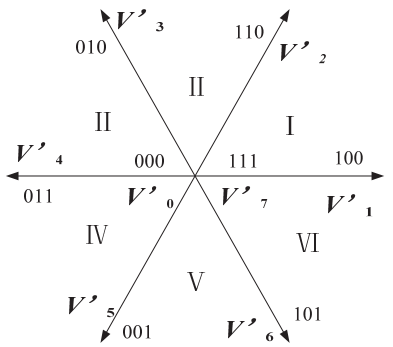

Fig. 1.Voltage space vector diagram of two-level inverters.

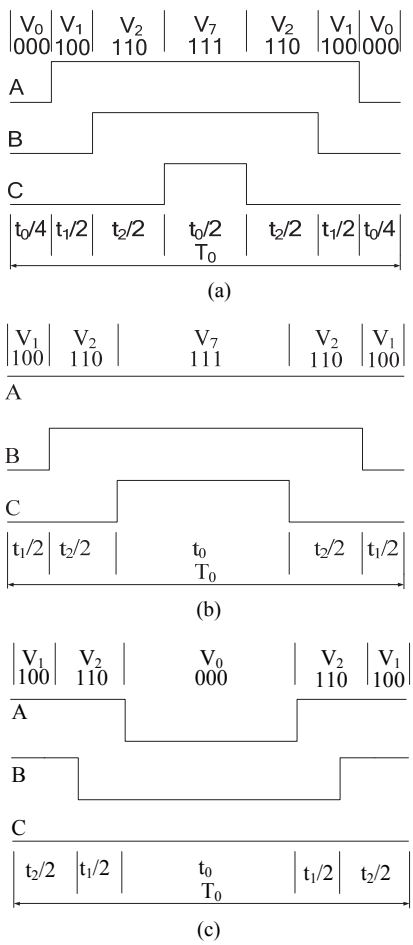

Fig. 2. Switching sequences of two-level inverter (sector I). (a) Traditional SVPWM. (b) DPWM with zero vector V'7(111). (c) DPWM with zero vector V'0(000).

III. PRINCIPLE OF OPTIMIZED MODULATION STRATEGY

Fig. 3 presents the topology of a three-level NPC inverter. In the figure, the neutral point of the capacitors in the DC side is grounded (in the simulation and experiment platform the neutral point is not grounded)for the convenience of analysis.

A. Transformation of Voltage Space Vectors

Taking phase A as an example, when VT_1 and VT_2 switchon and VT_3 and VT_4 switch off, the output voltage will be $U_{dc}/2$. When VT_3 and VT_4 switchon and VT_1 and VT_2 switch off, the output voltage will be $-U_{dc}/2$. When VT2 and VT3 switch on and VT1 and VT2 switch off, the output voltage will be 0. Voltage levels $U_{dc}/2$, $-U_{dc}/2$, and 0 can be defined as 1, –1 and 0, respectively. Therefore, the output levels of each phase are 1, 0, and –1, which make 3^3=27 voltage vectors. The voltage vector diagram of a three-level inverter is as follows:

$$V = \frac{2}{3}\left(V_A + V_B e^{j\frac{2\pi}{3}} + V_C e^{j\frac{4\pi}{3}} \right). \quad (1)$$

Fig. 4 shows that 27 switching states exist and 27 space vectors are generated. According to the vector length, these vectors can be divided into four types: zero, small, middle, and large vectors. $\boldsymbol{V}_0$ belongs to zero vectors, which have three kinds of switching states; $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, $\boldsymbol{V}_3$, $\boldsymbol{V}_4$, $\boldsymbol{V}_5$, and $\boldsymbol{V}_6$ belong to small vectors, which have two kinds of switching states; $\boldsymbol{V}_8$, $\boldsymbol{V}_{10}$, $\boldsymbol{V}_{12}$, $\boldsymbol{V}_{14}$, $\boldsymbol{V}_{16}$, and $\boldsymbol{V}_{18}$ belong to middle vectors; and $\boldsymbol{V}_7$, $\boldsymbol{V}_9$, $\boldsymbol{V}_{11}$, $\boldsymbol{V}_{13}$, $\boldsymbol{V}_{15}$, and $\boldsymbol{V}_{17}$ belong to large vectors. Both middle and large vectors have one switching state.

The voltage vector diagram of a three-level inverter is more complicated than that of a two-level inverter. The traditional realization of SVPWM divides every sector into four small triangles and calculates the action times of each voltage vector in small triangles. However, judging specific triangles is complicated, and the amount of calculation is large. Thus, extending to multi-level inverters is difficult using this method. A strategy that is easy to implement for extending to multi-level inverters is proposed in the following paragraphs.

As shown in Fig. 5, the three-level space vector diagram is six two-level space vectors. The vertices inside the hexagons are the centers of the small hexagons. $\boldsymbol{V}_0$ is the center of the three-level space vector diagram, and the end points of $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, $\boldsymbol{V}_3$, $\boldsymbol{V}_4$, $\boldsymbol{V}_5$, and $\boldsymbol{V}_6$ are the centers of the six small hexagons. When each small hexagon is moved to the center of the large hexagon along the reverse direction of the corresponding small vector, the voltage vector diagram of the three-level inverter will be simplified to a two-level voltage vector diagram.

The key to simplifying the three-level voltage vector diagram is to move the origin point of the synthesized reference vector to the center of the corresponding small hexagon. Thus, the reference vectors require revising.

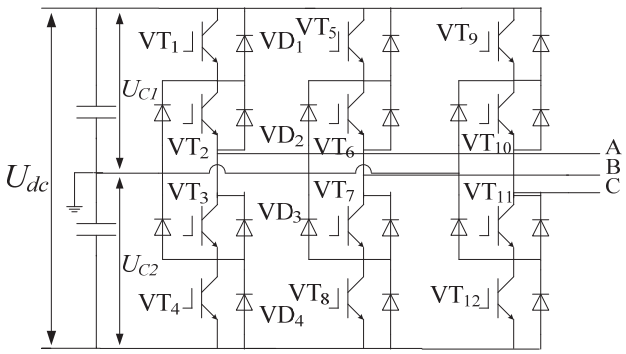

Fig. 3. Topology of three-level NPC inverter.

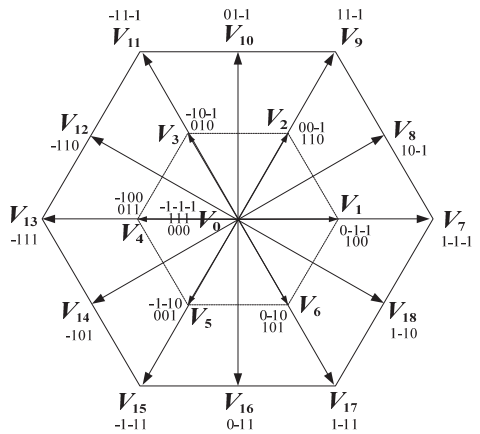

Fig. 4. Voltage vector diagram of three-level inverters.

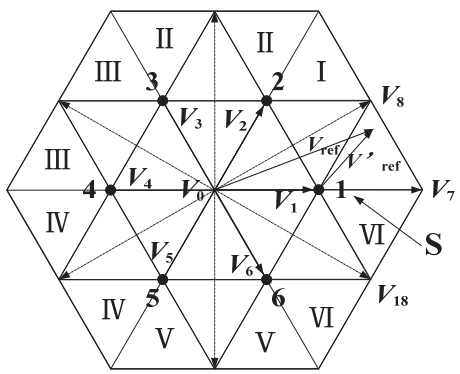

Fig. 5. Simplified vector diagram of three-level inverter.

In Fig. 5, V_{ref} is the synthesized reference vector of the three-level inverter and V'_{ref} is the revised vector. The relationship between V_{ref} and V'_{ref} is $V_{ref}=V_1+V'_{ref}$. That is, V_{ref} is subtracted from V_1 to obtain the revised reference vector V'_{ref}. Therefore, when the reference vectors are in other small hexagons, they should be subtracted from the corresponding small vectors to obtain the revised reference vectors.

A linear relation exists between the three-level and two-level algorithms. V'_{ref} can be regarded as a space vector in a two-level inverter, which is composed of V_1' and V_2'. The volt–second balance principle in a complex plane can be

expressed as follows:

$$\begin{pmatrix} V'_{1x} & V'_{2x} & 0 \\ jV'_{1y} & jV'_{2y} & 0 \\ 0 & 0 & 1 \end{pmatrix}\begin{pmatrix} t'_1 \\ t'_2 \\ T_0 \end{pmatrix} = \begin{pmatrix} V'_{refx}T_0 \\ jV'_{refy}T_0 \\ T_0 \end{pmatrix}, \quad (2)$$

Where t_1 and t_2 are the action times of V_1' and V_2', respectively.

In the case of the three-level algorithm, V_{ref} can be composed of V_7, V_8, and V_1. The expression is as follows:

$$\begin{cases} t_1V_7 + t_2V_8 + t_3V_1 = V_{ref}T_0 \\ t_1 + t_2 + t_3 = T_0 \end{cases}, \quad (3)$$

$$\begin{pmatrix} V_{7x} & V_{8x} & V_{1x} \\ jV_{7y} & jV_{8y} & jV_{1y} \\ 1 & 1 & 1 \end{pmatrix}\begin{pmatrix} t_1 \\ t_2 \\ t_3 \end{pmatrix} = \begin{pmatrix} V_{refx}T_0 \\ jV_{refy}T_0 \\ T_0 \end{pmatrix}, \quad (4)$$

where t_1, t_2, and t_3 are the action times of V_7, V_8, and V_1, respectively.

In sector I, the relationship between the two-level and three-level vectors is

$$\begin{cases} V_7 = a_1V_1' + b_1V_2' = (a_1V'_{1x} + b_1V'_{2x}) + j(a_1V'_{1y} + b_1V'_{2y}) \\ V_8 = a_2V_1' + b_2V_2' = (a_{12}V'_{1x} + b_2V'_{2x}) + j(a_2V'_{1y} + b_2V'_{2y}) \\ V_1 = a_3V_1' + b_3V_2' = (a_3V'_{1x} + b_3V'_{2x}) + j(a_3V'_{1y} + b_3V'_{2y}) \end{cases}. \quad (5)$$

By substituting (5) into (4), we can derive the following expression:

$$\begin{pmatrix} V'_{1x} & V'_{2x} & 0 \\ jV'_{1y} & jV'_{2y} & 0 \\ 0 & 0 & 1 \end{pmatrix}\begin{pmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{pmatrix}\begin{pmatrix} t_1 \\ t_2 \\ t_3 \end{pmatrix} = \begin{pmatrix} V_{refx}T_0 \\ jV_{refy}T_0 \\ T_0 \end{pmatrix}. \quad (6)$$

Therefore, the three-level algorithm can be realized by the vectors of the two-level inverter, significantly simplifying the complex strategy.

B. Switching Sequences of UP-PWM and LOW-PWM

The proposed strategy is simplified by the transformation of the reference vectors and coordinate system, and the two-level modulation algorithm can be used to achieve a three-level one. Therefore, the zero vectors $\boldsymbol{V'}_{0(000)}$ and $\boldsymbol{V'}_{7(111)}$ in the two-level vector diagram will correspond to the small vectors of the three-level inverters.

For convenience of analysis, the three-level voltage vector diagram is divided into six areas, which are represented by the symbol S. These areas are surrounded by the adjacent middle vectors of the three-level vector diagram, as shown in the dotted areas in Fig. 5. To minimize switching losses in the same S value, the state of each phase can only change between 1 and 0 or 0 and –1. The states of each phase do not exist in all (1, 0, and –1) levels. For instance, when S=1, the state of phase A changes between 1and 0, while that of phases B and C change between 0 and –1. Therefore, as shown in Fig. 4, when S=1 in phase A, VT_2 switches on and VT_4 switches off, while only VT_1 and VT_3 are valid for modulation. In phase B, VT_5 and VT_7 switchoff and on, respectively, and only VT_6 and VT_8 are valid for modulation. In phase C, VT_9 and VT_{11} switch off and on, respectively, and only VT_{10} and VT_{12} are valid for modulation.

As shown in Fig. 5, reference vector V_{ref} is in the S=1 region, and revised reference vector V'_{ref} is in sector I at the two-level vector graph through coordinate system transformation. V_{ref} is composed of $\boldsymbol{V}_{7(1\text{-}1\text{-}1)}$, $\boldsymbol{V}_{8(10\text{-}1)}$, and $\boldsymbol{V}_{1(0\text{-}1\text{-}1)}$, in which small voltage vector $\boldsymbol{V}_{1(0\text{-}1\text{-}1)}$ corresponds to zero vector $\boldsymbol{V'}_{0(000)}$ in the two-level voltage vector diagram. Small vector $\boldsymbol{V}_1$ has two kinds of switching states, (0-1-1) and (100). When S=1, the corresponding switching state is (0-1-1).

The two types of two-level DPWM strategies mentioned above distribute zero vectors in the center of the switching sequences. One type only selects $\boldsymbol{V'}_{0(000)}$, and one of the three phases will be clamped to the upper bus of the inverter all the time. This strategy can be called upper-clamped PWM or UP-PWM for short. The other only selects $\boldsymbol{V'}_{7(111)}$, and one of the three phases will be clamped to the lower bus. This strategy is called lower-clamped PWM or LOW-PWM. The switching sequences of UP-PWM and LOW-PWM are shown as follows, with S=1 and V'_{ref} in sector I of the corresponding small hexagon.

Tables I and II show the switching sequences of the two-level strategy and the corresponding three-level strategy, respectively. In Table II, the center of the two switching sequences is small vector $\boldsymbol{V}_1$. LOW-PWM corresponds to $\boldsymbol{V}_{1(0\text{-}1\text{-}1)}$, and this small vector is considered a negative vector. UP-PWM corresponds to $\boldsymbol{V}_{1(100)}$, and this small vector is considered a positive vector.

Then, the switching sequences of the proposed strategy are as follows.

1) S=1, sector VI
   LOW-PWM: [1-10]—[1-1-1]—[0-1-1]—[1-1-1]—[1-10]
   UP-PWM: [1-1-1]—[1-10]—[100]—[1-10]—[1-1-1]
2) S=1, sector I
   LOW-PWM: [10-1]—[1-1-1]—[0-1-1]—[1-1-1]—[10-1]
   UP-PWM: [1-1-1]—[10-1]—[100]—[10-1]—[1-1-1]
3) S=2, sector I
   LOW-PWM: [11-1]—[10-1]—[00-1]—[10-1]—[11-1]
   UP-PWM: [10-1]—[11-1]—[100]—[11-1]—[10-1]
4) S=2, sector II
   LOW-PWM: [11-1]—[01-1]—[00-1]—[01-1]—[11-1]
   UP-PWM: [01-1]—[11-1]—[100]—[11-1]—[01-1]
5) S=3, sector II
   LOW-PWM: [01-1]—[-11-1]—[-10-1]—[-11-1]—[01-1]
   UP-PWM: [-11-1]—[01-1]—[010]—[01-1]—[-11-1]
6) S=3, sector III
   LOW-PWM: [-110]—[-11-1]—[-10-1]—[-11-1]—[-110]
   UP-PWM: [-11-1]—[-110]—[010]—[-110]—[-11-1]

TABLE I
SWITCHING SEQUENCES OF THE TWO-LEVEL STRATEGY
(S=1, SECTOR I)

LOW-PWM	101	100	000	100	101
UP-PWM	100	101	111	101	100

TABLE II
CORRESPONDING SWITCHING SEQUENCES OF THE THREE-LEVEL STRATEGY (S=1, SECTOR I)

LOW-PWM	1-10	1-1-1	0-1-1	1-1-1	1-10
UP-PWM	1-1-1	1-10	100	1-10	1-1-1

7) S=4, sector III
LOW-PWM: [-111]—[-110]—[-100]—[-110]—[-111]
UP-PWM: [-110]—[-111]—[010]—[-111]—[-110]
8) S=4, sectorIV
LOW-PWM: [-111]—[-101]—[-100]—[-101]—[-111]
UP-PWM: [-101]—[-111]—[011]—[-111]—[-101]
9) S=5, sector IV
LOW-PWM: [-101]—[-1-11]—[-1-10]—[-1-11]—[-101]
UP-PWM: [-1-11]—[-101]—[001]—[-101]—[-1-11]
10) S=5, sector V
LOW-PWM: [0-11]—[-1-11]—[-1-10]—[-1-11]—[0-11]
UP-PWM: [-1-11]—[0-11]—[001]—[0-11]—[-1-11]
11) S=6, sector V
LOW-PWM: [1-11]—[0-11]—[0-10]—[0-11]—[1-11]
UP-PWM: [0-11]—[1-11]—[101]—[1-11]—[0-11]
12) S=6, sector VI
LOW-PWM: [1-11]—[1-10]—[0-10]—[1-10]—[1-11]
UP-PWM: [1-10]—[1-11]—[101]—[1-11]—[1-10]

According to the switching sequences above, LOW-PWM corresponds to negative vectors, whereas UP-PWM corresponds to positive vectors.

C. Comparison of Switching Losses

Taking phase A as an example, the device voltage stress is equal to DC-link voltage U_{dc}, and the current stress is equal to output current i_a. Thus, the switching loss for each switch of the traditional SVPWM is

$$P = \frac{1}{2\pi}\frac{U_{dc}(t_{on}+t_{off})}{2T_s}\int_0^{2\pi} f_i(\theta)d\theta \,, \tag{7}$$

$$f_i(\theta) = \begin{cases} |i_a|, & \text{when switch is on.} \\ 0, & \text{when switch is off.} \end{cases}, \tag{8}$$

Where t_{on} and t_{off} are the switch-on and -off times of each switch, respectively.

However, the switching sequence of UP-PWM shows that the switches of phase A are not active in sectors I and VI. Under the action of LOW-PWM, the switches are not active in sectors III and IV. Therefore, their switching losses can be calculated from (9) and (10), respectively, as follows:

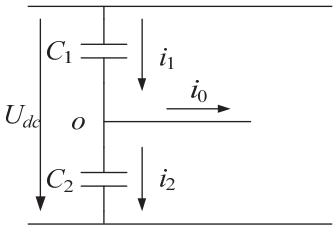

Fig. 6. Analysis graph of neutral point.

$$P = \frac{1}{2\pi}\frac{U_{dc}(t_{on}+t_{off})}{2T_s}\int_{\frac{\pi}{3}}^{\frac{5\pi}{3}} f_i(\theta)d\theta \,, \tag{9}$$

$$P = \frac{1}{2\pi}\frac{U_{dc}(t_{on}+t_{off})}{2T_s}\left(\int_0^{\frac{2\pi}{3}} f_i(\theta)d\theta + \int_{\frac{4\pi}{3}}^{2\pi} f_i(\theta)d\theta\right). \tag{10}$$

UP-PWM and LOW-PWM can shorten the switching times by one-third, and the proposed strategy is the combination of UP-PWM and LOW-PWM. Therefore, compared with the traditional SVPWM, the proposed strategy can reduce switching losses by one-third.

IV. HYSTERESIS CONTROL OF NEUTRAL-POINT BALANCE

A. Principle of Neutral-Point Balance

In Fig. 6, i_1 and i_2 are the charging currents of capacitors C_1 and C_2, respectively, and i_0 is the current of the neutral point in the DC side. The directions of these currents are shown in the graph. The neutral-point imbalance is caused by two factors. The first one is the voltage space vectors, especially the small vectors that may affect the neutral-point potential. The second one is the asymmetry of the three-level inverter [22]. A total of 27 kinds of voltage space vectors correspond to 27 switching states. When the state of one phase islevel0, the external circuit of that phase will inject or extract currents into the capacitors in the DC side, which may cause the fluctuation of the neutral point, while $i_0 \neq 0$.

The 0 level does not appear in the switching states of large vectors, which means that the currents will not be injected to or extracted from the neutral point in the DC side. Thus, no fluctuation of neutral point occurs and i_0=0. There are 0 levels in the switching states of small vectors, and the non-zero levels are the same. Therefore, small vectors will influence the neutral point voltage. For example, $\boldsymbol{V}_1$ has two kinds of switching states, (0-1-1) and (100). (0-1-1) can make the neutral point connect with the negative terminal in the DC side, which will extract currents from the neutral point, and i_0>0 with the decreasing neutral point voltage. That is, negative vectors always decrease the neutral point. On the contrary, (100) can make the neutral point connect with the positive terminal and i_0<0 with the increasing neutral point

voltage. That is, positive vectors can increase the neutral point. The middle vectors also have 0 level states, but their non-zero levels are opposite, which makes the direction of i_0 uncertain. Therefore, they may increase or decrease the neutral point in different situations, and the fluctuation of the neutral point is uncertain.

B. Effects of the Proposed Strategy on Neutral Point

According to the switching sequences of LOW-PWM and UP-PWM, LOW-PWM only uses negative vectors to decrease the neutral point, and UP-PWM only uses positive vectors to increase the neutral point.

As shown in Fig. 7, the voltage of the DC side is 600V, and the two DC capacitors' voltages are balanced at the beginning of the simulation.U_{C1} and U_{C2} are the voltages of the upper and lower capacitors, respectively.

In Fig. 7(a), LOW-PWM makes U_{C1} rise and U_{C2} fall. U_{C1} rises to the bus voltage at 0.2s, while U_{C2} is 0. Therefore, LOW-PWM will decrease the voltage of the neutral point and even make it equal to 0 in some cases. In Fig. 7(b), UP-PWM makes U_{C1} fall and U_{C2} rise. U_{C2} finally rises to the bus voltage. Thus, UP-PWM will increase the voltage of the neutral point and may allow it reach to the bus voltage gradually.

C. Principle of Hysteresis Control

As stated above, UP-PWM or LOW-PWM alone can cause neutral fluctuation, and their fluctuation directions are opposite. To solve this problem, a hysteresis loop control with the required loop width is proposed as follows.

Fig. 8 shows the proposed method for neutral-point balance. U_0 is the voltage of the neutral point in the DC side and the input of the hysteresis loop regulator. The output of the hysteresis loop is 1 or 0, and the PWM generator will output pulses according to the hysteresis output to realize the control of the neutral-point balance.

The specific principle of the hysteresis loop controller is shown in Fig. 9(a). First, the reference value of the hysteresis loop is half of the voltage of the DC side, $U_{dc}/2$. The control target is to limit the neutral point in the range of the loop width. The hysteresis loop has two thresholds, U_{dc}-/2 and U_{dc}+/2. If the initial output of the hysteresis loop controller is 0, then the voltage of the neutral point will increase gradually, while the voltage will reach the first threshold, U_{dc}-/2, without changing the output. Only the voltage reaches the second threshold, U_{dc}+/2, and the output changes to 1. When the voltage decreases, the situation will be the same. The loop width is the difference between U_{dc}+/2 and U_{dc}-/2.

Fig. 9(b) is the principle diagram of the PWM generator. When the output of the hysteresis controller is 0, the neutral point voltage should be improved, and the PWM generator selects UP-PWM. When the output of the hysteresis controller is 1, the PWM generator selects LOW-PWM. Therefore, the neutral-point voltage can be limited in the range of the loop width. Unlike other neutral-point control strategies, the proposed strategy does not need to judge the direction of neutral-point currents, thus greatly simplifying the entire control system.

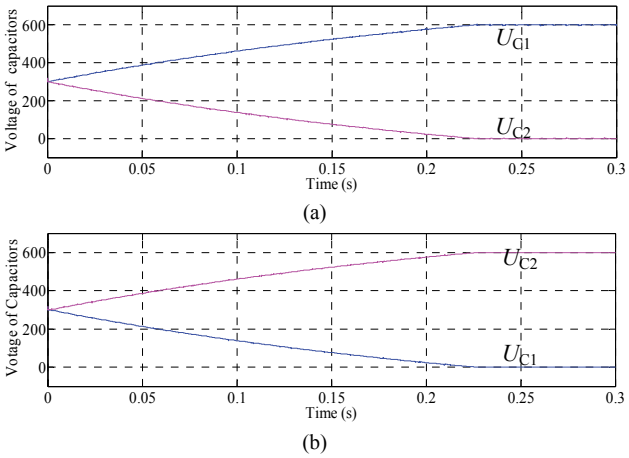

Fig. 7. Simulation of LOW-PWM and UP-PWM effects on neutral point. (a) LOW-PWM. (b) UP-PWM.

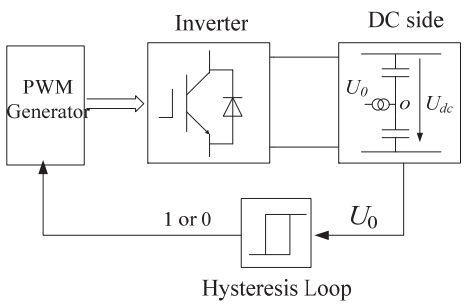

Fig. 8. Block diagram hysteresis loop control.

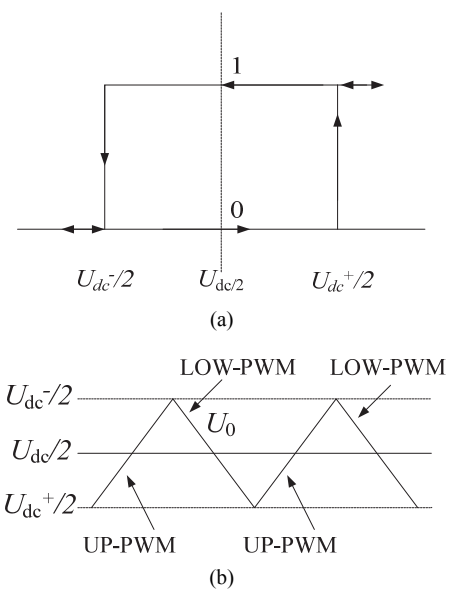

Fig. 9. Principle of hysteresis loop and PWM generator. (a) Hysteresis loop. (b) PWM generator.

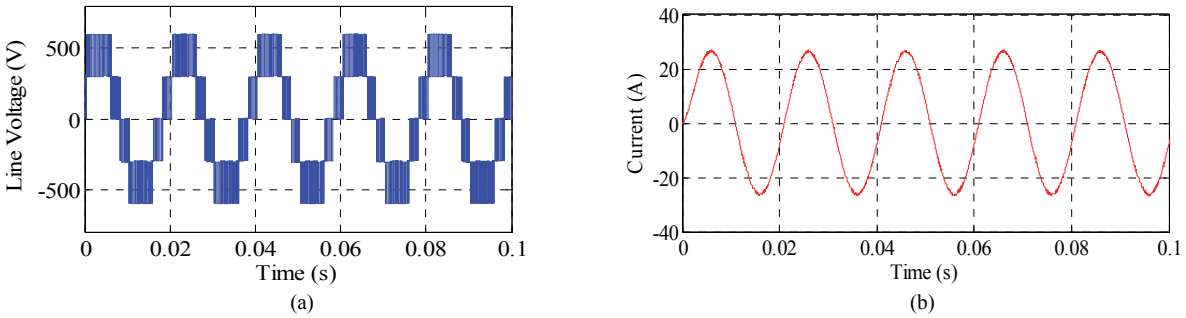

Fig. 10. Output voltage and current of phase A in simulation model. (a) Line voltage VAB. (b) Line current IA.

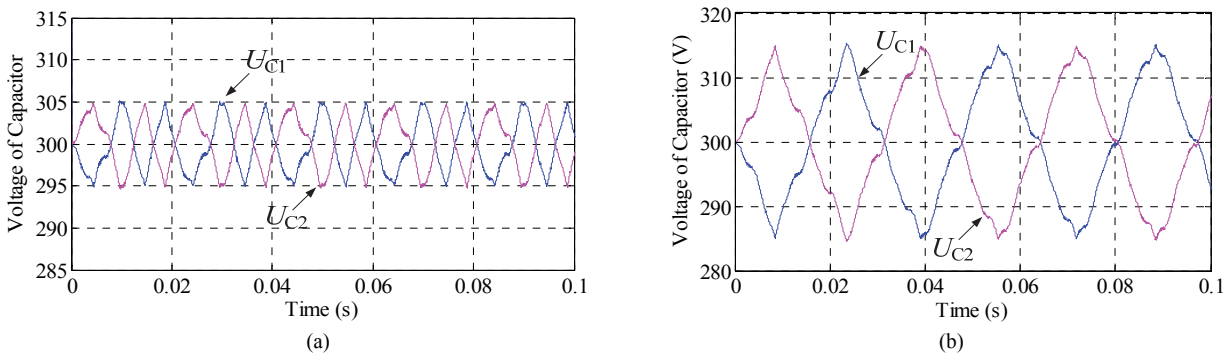

Fig. 11. Voltages of upper and lower capacitors.(a) Loop width is 10V. (b) Loop width is 30V.

V. Simulation and Experiment

The proposed strategy has been verified by simulation and experiment. The parameters of the simulation model are shown in Table III, where the inverter operates with an RL load and the modulation index is 0.8.

Fig. 10 showsthe output voltage and the current of phase A. Different loop widths correspond to different fluctuations of the neutral point and switching times. Fig. 11(a) shows the voltage waveforms of the upper and lower capacitors in the DC side where the loop width is 10V. The voltage of the lower capacitor is also the voltage of the neutral point. Fig. 11(b) presents the voltage waveforms of the upper and lower capacitors where the loop width is 30V. The neutral point voltage is limited by the width of the hysteresis loop. The smaller the loop width is, the smaller the fluctuation of the neutral point will be. However, when the loop width is smaller, the switching times and frequency between UP-PWM and LOW-PWM will be higher as well. This condition means that an extremely small loop width is not the optimal target for hysteresis control, and the other target of output voltage THD should be considered and will be influenced directly by the loop width. Therefore, the optimal strategy must balance the performance between neutral-point control and switching-loss control. The output voltage harmonics of different loop widths are provided in Table IV.

To further testthe proposed optimized switching loss PWM strategy and the hysteresis control of the neutral point,an experimental platform is built as follows.

TABLE III
Parameters of the Simulation Model

Parameters	Value
frequency of three-phase voltage	50 HZ
voltage of DC side	600 V
frequency of triangular carrier	2000 HZ
capacitor of DC side	220 μF
resistor load	10 Ω
inductor load	10 mH

TABLE IV
Output Voltage Harmonics of Different Ring Widths

Loop Width/V	Low Order Harmonic Distortion/%	Total Harmonic Distortion/%
10	0.45	38.43
20	0.35	38.32
30	0.32	19.74
40	0.4	18.90
50	0.55	19.64

The block diagram of the experimental model is shown in Fig. 12(a). The DC voltage is obtained from the three-phase rectifier. DSP TMS320F2812 is the core control chip, which is used to generate the PWM pulses and realize the hysteresis control of the neutral point. CPLD protects the system from incorrect PWM pulses that may damage the switching devices. The sensors of voltage sampling and current sampling are 300V/25mA and 200A/100mA, respectively. The switching

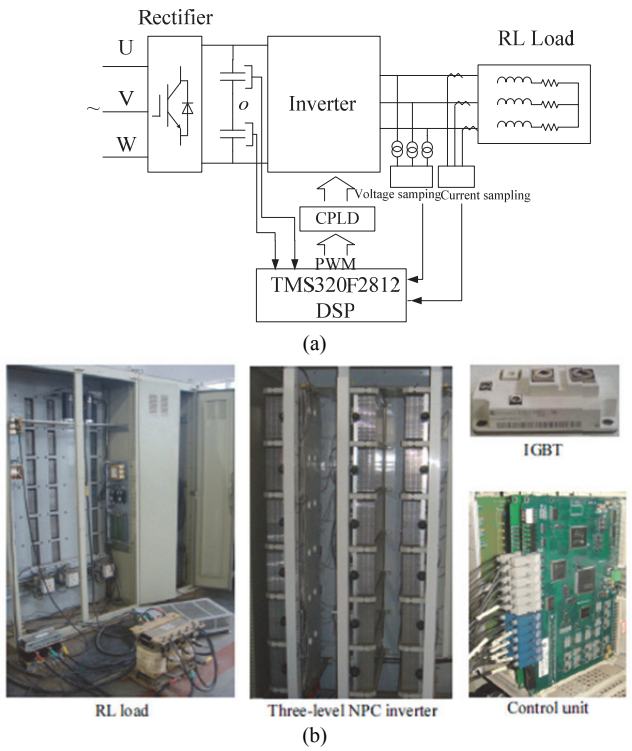

Fig. 12. Block diagram of experiment and platform. (a) Block diagram. (b) Experiment platform.

TABLE V
SPECIFIC PARAMETERS OF THE THREE-LEVEL EXPERIMENTAL PLATFORM

Parameters	Value
Frequency of three-phase voltage	50 HZ
Input of three-phase voltage	380 V
Frequency of triangular carrier	2000 HZ
Capacitor of DC side	10000μF
Resistor load	8Ω
Inductor load	23mH
rated power of resistor	12kW
rated voltage of inductor	400V

device of the inverter is IGBT, and its specification is 1200V/400A.The experiment platform of the entire system is shown in Fig. 12(b), and the parameters of the entire system are shown in Table V.

In verifying the different effects on the neutral points of UP-PWM and LOW-PWM, the three-phase line voltage of the rectifier is decreased to 60V to ensure the safety of the experiment. Otherwise, the great deviation in capacitor voltage may damage the entire experimental platform.

Fig. 13 showsthe modulation waveforms of UP-PWM and LOW-PWM. The modulation wave of the proposed optimized switching loss strategy is the combination of UP-PWM and LOW-PWM and is related to the width of the hysteresis loop. Fig. 14 shows the effects of UP-PWM and LOW-PWM alone on the neutral point. The results show that the neutral point is

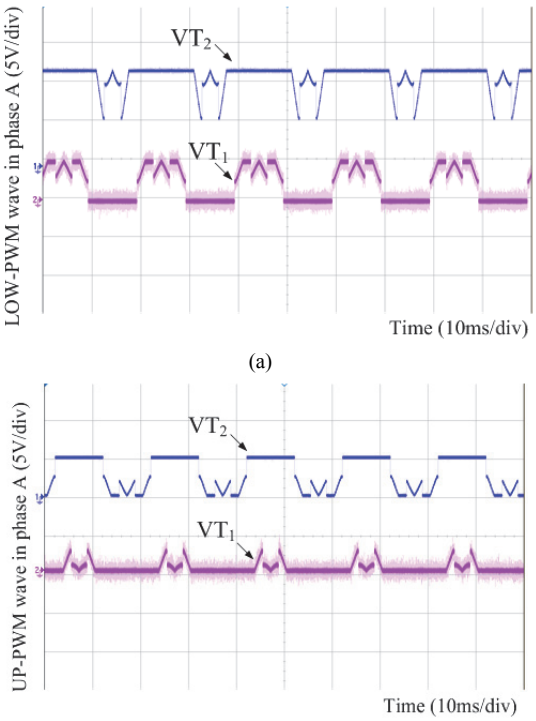

Fig. 13. Modulation waveforms of two PWM strategies. (a) LOW-PWM. (b) UP-PWM.

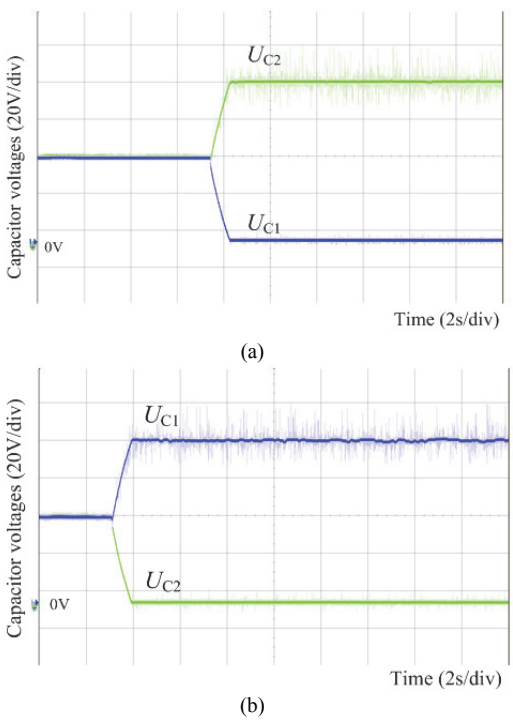

Fig. 14. Different effects of two types of strategies on neutral point. (a) UP-PWM. (b) LOW-PWM.

balanced before the inverter operates. Given that the output voltage of the rectifier is 85V, both capacitor voltages are 42.5V. When UP-PWM operates alone, the upper and lower capacitor voltages will decrease and increase, respectively.

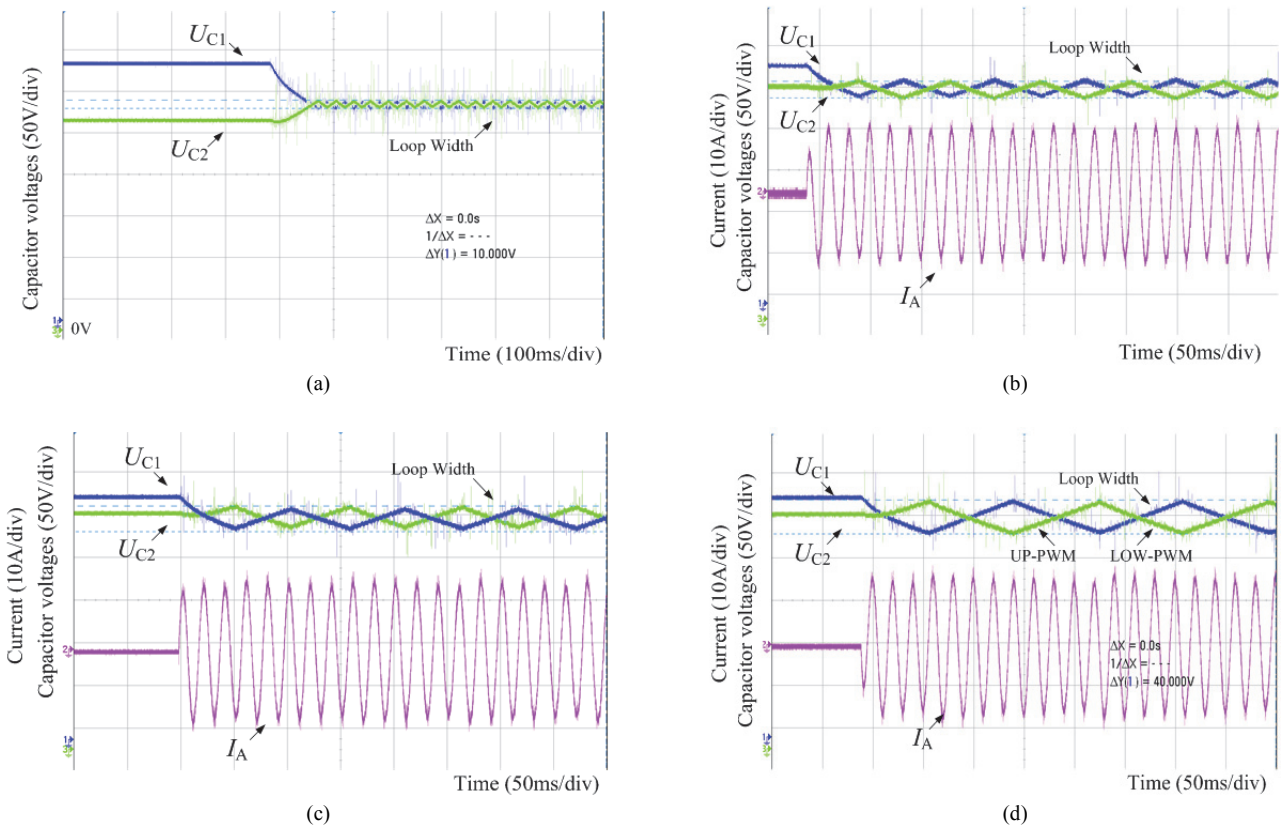

Fig. 15. Neutral point voltage and output line current of different loop widths. (a) 10V width. (b) 20V width. (c) 30V width. (d) 40 V width.

Eventually, the voltage of the neutral point increases to 85 V. When LOW-PWM operates alone, the situation will be the opposite, and the voltage of the neutral point will decrease gradually to 0V.

The proposed hysteresis control strategy can balance the neutral point. In Fig. 15, the initial neutral point is unbalanced, and hysteresis control strategy can balance the neutral point quickly. At this time, the three-phase line voltage of the rectifier is 380V and the output voltage is 538 V. At the beginning, the voltages of the two capacitorsare 298 and 240V, respectively, and the loop width is 10V.

The fluctuations of the neutral point of different loop widths and the corresponding currents of phase A are shown in Fig. 15. The loop widths of Figs. 15(a), 15(b), 15(c), and 15(d) are 10, 20, 30, and 40V, respectively. Thus, the smaller the width is, the smaller the fluctuations of the neutral point and the current amplitude will be. Moreover, the THD of the output voltage is related to the loop width. Fig. 16 is the harmonic distortions of the line voltage under different loop widths, where the modulation index is fixed at 0.8. The results show that although the three-order harmonic (H3), the five-order harmonic (H5), and the seven-order harmonic (H7) are nearly the same under different loop widths, the inverter operating under the 20V width has the smallest THD, which proves that a small loop width is not the best. Comprehensive

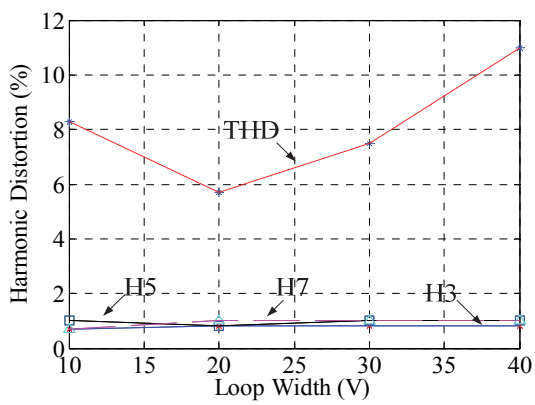

Fig. 16. Harmonic distortion of output voltages with different loop widths.

consideration is required to select the optimal loop width, including switching times, harmonic distortion, and switching losses, to realize the optimized low-switching PWM and a neutral-point balance control strategy. In this experiment, 20V is selected as the optimal loop width. The output line voltage and currents of the proposed strategy are shown in Fig. 17(a), where the loop width is 20V and the modulation index is 0.8. Fig. 17(b) shows the phase voltage of phase A. The experiment results prove the effectiveness and feasibility of the proposed strategy.

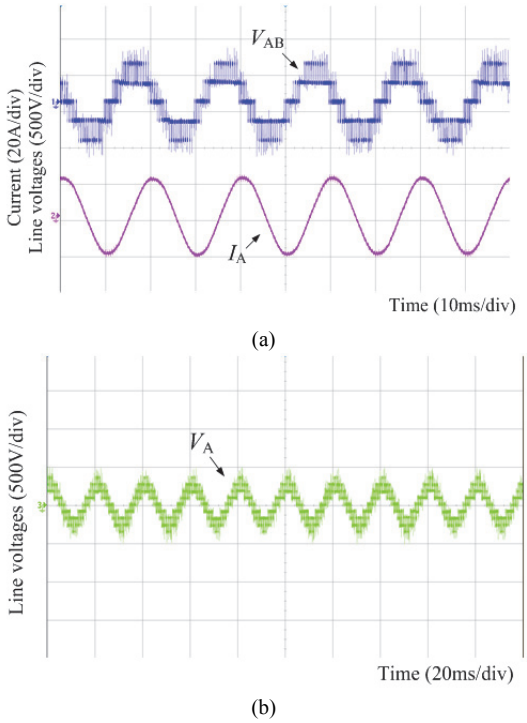

Fig. 17. Output voltage and current with20V width. (a) Line voltage V_{AB} and current I_A. (b) Phase voltage V_A.

VI. Conclusion

This paper proposes an optimized low-switching and neutral-point balance control strategy for three-level NPC inverters. Compared with other traditional strategies, the proposed strategy has the following advantages:

1) Switching losses are reduced by one-third compared with the traditional SVPWM strategy without increasing the harmonic distortions.
2) The neutral-point voltage can be balanced by hysteresis loop control under different loop widths without judging the direction of neutral point currents.
3) The strategy has been simplified, making it easy to implement by processors.

The effectiveness of the proposed strategy in reducing power losses and balancing the neutral point has been validated by simulation and experimental results. Owing to its low switching losses and easy implementation,the proposed strategy is suitable for industrial applications that require high performance and stability, such as AC motor drive systems.

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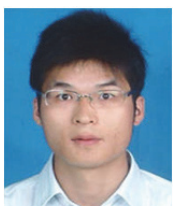
References

[1] Q. Lei and F. Z. Peng, "Space vector pulsewidth amplitude modulation for a buck–boost voltage/current source inverter," *IEEE Trans. Power Electron*., Vol. 29, No. 1, pp, 266-274, Jun. 2013.
[2] H. Sawezyn, N.Idir, and R.Bausiere, "Lowering the drawbacks of slowing down di/dt and dv/dt of insulated gate transistors," *International Conference on Power Electronics, Machines and Drives, IET*, Vol. 2002, pp. 551-556, 2002.
[3] S. An, X. Sun, Y. Chen, Zhong, Y., and B. Ren, "A new generalized implementation method of discontinuous pwm," in *Proc. Csee*, Vol. 32, pp. 59-66, 2012.
[4] O. Ojo, "The generalized discontinuous pwm scheme for three-phase voltage source inverters," *IEEE Trans. Ind. Electron*., Vol. 51, No. 6, pp. 1280-1289, Dec. 2004.
[5] J. H. Seo, H. C. Chang, and S. H. Dong, "A new simplified space-vector pwm method for three-level inverters," *IEEE Trans. Power Electron*., Vol. 16, No. 4, pp. 545-550, Jul. 2001.
[6] W. Jiang, Q. Wang, and Chen, "Svpwm strategy for three-level inverter based on svpwm strategyfor two-level inverter," *Trans. China Electrotechnical Society*, Vol. 24, No. 1, pp. 108-114, 2009.
[7] Y. Jiao, S. Lu, and F. C. Lee, "Switching performance optimization of a high power high frequency three-level active neutral point clamped phase leg," *IEEE Trans. Power Electron.*, Vol. 29, No. 7, PP. 3255-3266, Jul. 2014.
[8] N. V. Nguyen, B. X. Nguyen, and H. H. Lee, "An optimized discontinuous PWM method to minimize switching loss for multilevel inverters," *IEEE Trans. Ind. Electron*., Vol. 58, No. 9, pp. 3958-3966, Sep. 2011.
[9] J. W. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system," *IEEE Trans. Ind. Appl.*, Vol. 27, No. 6, pp. 1063-1075, Nov./Dec. 1991.
[10] M. Bierhoff, H. Brandenburg, and F. W. Fuchs, "An analysis on switching loss optimized PWM strategies for three phase PWM voltage source converters," *Industrial Electronics Society, IECON 2007, Conference of the IEEE*, pp. 1512-1517, 2007.
[11] Y. Wu, C. Y. Leong, and R. A. Mcmahon, "A study of inverter loss reduction using discontinuous pulse width modulation techniques," *International Conference on Power Electronics, Machines and Drives, IET*, Vol.42, pp. 596-600, 2006.
[12] Y. Jiao, F. C. Lee, and S. Lu, "Space vector modulation for three-level npc converter with neutral point voltage balance and switching loss reduction," *IEEE Trans. Power Electron*., Vol. 29, No.10, 1, pp. 5579-5591, Dec. 2014.
[13] Z. Zhang, O. C. Thomsen, and M. A. E. Andersen, "Discontinuous PWM modulation strategy with circuit-level decoupling concept of three-level neutral-point-clamped (npc) inverter," *IEEE Trans. Ind. Electron*., Vol. 60, No. 5, pp. 1897-1906, Nov. 2013.
[14] L. Ben-Brahim, "A discontinuous PWM method for balancing the neutral point voltage in three-level inverter-fed variable frequency drives," *IEEE Trans. Energy Convers.*, Vol. 23, No. 4, pp. 1057-1063, Dec. 2008.
[15] H. J. Park and M. J. Youn, "A new time-domain discontinuous space-vector PWM technique in overmodulation

region," *IEEE Trans. Ind. Electron*., Vol. 50, No. 2, pp. 349-355, Apr. 2003.
[16] L. Dalessandro, S. D. Round, U. Drofenik, and J. W. Kolar, "Discontinuous space-vector modulation for three-level pwm rectifiers," *IEEE Trans. Power Electron*., Vol. 23, No. 2, pp. 530-542, Mar. 2008.
[17] Y. Wu, M. A. Shafi, A. M. Knight, and R. A. Mcmahon, "Comparison of the effects of continuous and discontinuous PWM schemes on power losses of voltage-sourced inverters for induction motor drives," *IEEE Trans. Power Electron*., Vol. 26, No. 12, pp. 182-191, Jul. 2011.
[18] A. M. Hava, R. J. Kerkman, and T. Lipo, "A high-performance generalized discontinuous pwm algorithm," *IEEE Trans. Ind. Appl*., Vol. 2, No. 5, pp. 1059-1071, Oct. 1998.
[19] O. R. Solomon and P. Famouri, "A novel approach for evaluating performance of discontinuous pulse width modulation schemes for three phase voltage source inverter," *IEEE International Symposium on Industrial Electronics*, Vol. 2, pp. 870-875. Jul. 2006.
[20] H. B. Michael and W. F. Friedrich, "Dc-link harmonics of three-phase voltage-source converters influenced by the pulsewidth-modulation strategy – An analysis," *IEEE Trans. Ind. Electron*., Vol. 55, No. 5, pp. 2085-2092, May 2008.
[21] A. K. Gupta and A. M. Khambadkone, "A simple space vector pwm scheme to operate a three-level npc inverter at high modulation index including overmodulation region, with neutral point balancing," *IEEE Trans. Ind. Appl*., Vol. 43, No. 3, pp. 751-760, May 2007.
[22] W. X. Yao, L. Zheng-Yu, W. M. Fei, and Z. M. Qian, "A new three-level neutral point potential hysteresis-band control," *Proc. the Csee*, 2005.
[23] J. Shen, S. Schroder, B. Duro, and R. Roesner, "A neutral-point balancing controller for a three-level inverter with full power-factor range and low distortion," *IEEE Trans. Ind. Appl*., Vol. 49, No. 49, pp. 138-148, Nov. 2012.
[24] K. Y. Chen, Z. Chen, and Y. L. Xie, and X. Mao, "Low switching loss and harmonics PWM for three-phase grid-connected PV inverter," *International Future Energy Electronics Conference and Ecce Asia, IEEE*, pp. 1457-1461, 2017.
[25] F. C. D. Andrade, F. Bradaschia, L. R. Limongi, and M. C. Cavalcanti, "A reduced switching loss technique based on generalized scalar pwm for nine-switch inverters," *IEEE Trans. Ind. Electron*., Vol. 65, No. 1, pp. 38-48. Jun. 2017.
[26] J. Afsharian, D. D. Xu, and B. Wu, B. Gong, and Z. Yang, "The optimal pwm modulation and commutation scheme for three-phase isolated buck matrix type rectifier," *IEEE Trans. Power Electron*., Vol. 33, No. 1, pp. 110-124. Jan. 2017.
[27] S. J. Lee, J. U. Lee, H. W. Kim, and K. Y. Cho, "Power loss minimization of common-mode noise reduced single-phase inverter by power device combination," *Power Electronics Conference, IEEE*, pp. 1-5, 2017.
[28] Y. Xia and R. Ayyanar, "Naturally adaptive, low-loss zero voltage transition circuit for high frequency full bridge inverters with hybrid PWM," *IEEE Trans. Power Electron*., to be published.
[29] G. Zhang, Y. Yang, F. Iannuzzo, K. Li, F. Blaabjerg, and H. Xu, "Loss distribution analysis of three-level active neutral-point-clamped (3L-ANPC) converter with different PWM strategies," *Power Electronics Conference, IEEE*, pp. 1-6, 2017.
[30] S. Bhattacharya, S. K. Sharma, D. Mascarella, and G. Joós, "Sub-fundamental cycle switching frequency variation for switching losses reduction of a two-level inverter traction drive," *IEEE Trans. Transport. Electrific*., Vol. 3, No. 3, pp. 645-655, Apr. 2017.



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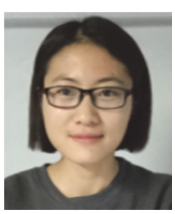

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