

# Analysis and Optimization of Bidirectional Exponential SC Power Conversion Circuits

Yuanmao Ye<sup>†</sup>, Wei Peng<sup>\*</sup>, Bijia Jiang<sup>\*</sup>, and Xianyong Zhang<sup>\*\*</sup>

<sup>†\*</sup> School of Automation, Guangdong University of Technology, Guangzhou, China

<sup>\*\*</sup> College of Automation, Guangdong Polytechnic Normal University, Guangzhou, China

## Abstract

A bidirectional exponential-gain switched-capacitor (SC) DC-DC converter is developed in this paper. When compared with existing exponential SC converters, the number of switches is significantly reduced and its structure is simplified. The voltage transfer features, voltage ripple across capacitors, efficiency and output impedance of the proposed converter are analyzed in detail. Optimization of the output impedance is also discussed and the best type of capacitance distribution is determined. A common function of the voltage gain to the output impedance is found among the proposed converter and other popular SC voltage multipliers. Experimental evaluation is carried out with a 6-24V bidirectional prototype converter.

**Key words:** DC-DC converters, High voltage gain, Output impedance, Switched capacitor

## I. INTRODUCTION

Due to the advantages of the absence of bulky magnetic components and IC compatibility, switched-capacitor (SC) power converters have been receiving a lot of attention from researchers [1]-[22]. The authors of [2]-[7] presented the analysis, design, regulation and control of SC converters in detail, while various modeling methods have been introduced in [8]-[10]. In particular, two-phase SC converters, also known as voltage multipliers [11]-[14], have been widely used in different applications such as flash memory devices, biomedical systems, LCD drivers, etc. [15]-[17]. The most popular SC power converters include the series-parallel (SP) [18], Dickson [13], Fibonacci [19] and exponential-gain SC converters [20], [21].

In this paper, a new exponential-gain SC converter is developed by cascading multiple double-mode switched-capacitor (DMSC) cells. When compared with the existing exponential-gain SC converter shown in Fig. 1, the proposed converter has the advantages of a reduced number of switches and a simple circuit configuration. The voltage transfer features

and voltage ripples across the capacitors as well as the power conversion efficiency are analyzed using Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL). The output impedance is also derived in the two cases where the parasitic resistances are considered and ignored.

For practical applications, the size and cost of a SC converter is dominated by the total capacitance  $C$  and the number of switches. The output impedance is directly related to the total capacitance  $C$  and the switching frequency of the SC converter. However, with the difference distribution manner of the total capacitance, the output impedance is varied. In this paper, the effect of the capacitance distribution on the output impedance is discussed, and an optimized capacitance distribution method is developed for the minimum output impedance. This optimized method is further extended to the aforementioned high order SC converters. Compared with other studies, the proposed SC converter has the advantage of a simpler structure.

Based on the theoretical analysis, a 6-24V bidirectional prototype converter is built to evaluate the performance of the proposed exponential-gain converter.

## II. BIDIRECTIONAL EXPONENTIAL-GAIN SC CONVERTER

### A. Circuit Configuration

Fig. 2 shows the proposed bidirectional exponential-gain

Manuscript received Sep. 13, 2017; accepted Jan. 9, 2018

Recommended for publication by Associate Editor Chun-An Cheng.

<sup>†</sup>Corresponding Author: eeyeym@gdut.edu.cn

Tel: +86-15914689420, Guangdong Univ. of Tech.

<sup>\*</sup>School of Automation, Guangdong University of Technology, China

<sup>\*\*</sup>College of Automation, Guangdong Polytechnic Normal University, China

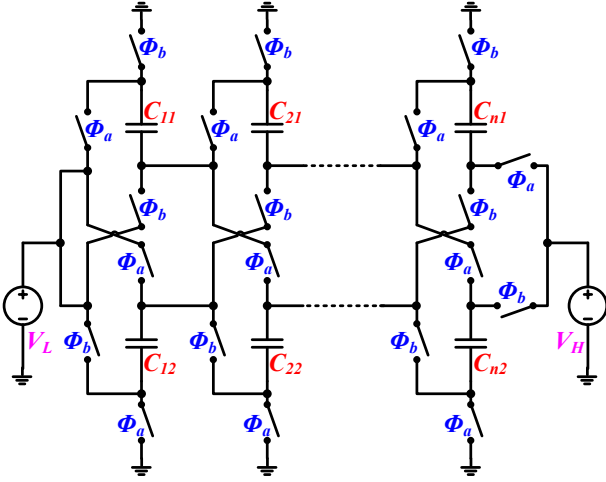


Fig. 1. Conventional exponential-gain SC converter.

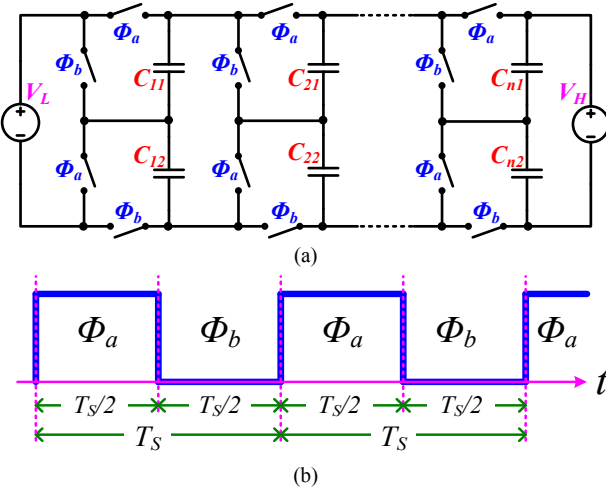


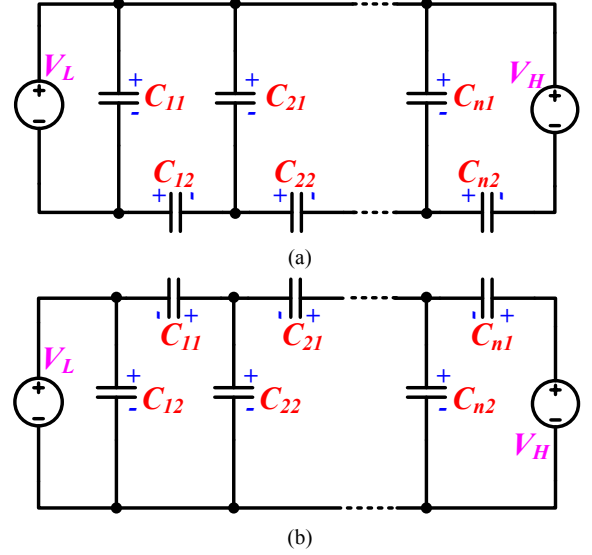
Fig. 2. Proposed bidirectional exponential-gain SC converter: (a) Topology; (b) Time slots.

SC converter. Fig. 2(a) shows the topology which is cascaded by multiple DMSC cells. Each DMSC cell is made up of four transistors and two flying capacitors.  $V_L$  and  $V_H$  represent the low and high voltage terminals, respectively. As indicated in Fig. 2(b), there are two clock phases,  $\Phi_a$  and  $\Phi_b$ , when the switch will be closed. The two phases are fully complementary and equally divide a switching cycle. In practice, a small dead-time is required between the two phases.

### B. No-Load Analysis

For sake of convenience, it is assumed that all of the components are ideal, i.e. there is no on-resistance for the switches, and the equivalent series resistance (ESR) for the capacitors are made for the following analysis.

Fig. 3 gives the two alternate state circuits for the proposed SC converter. For the clock phase  $\Phi_a$ , the positive electrodes of  $V_L$ ,  $V_H$  and  $C_{i1}$  ( $i=1, 2, \dots, n$ ) are connected together as shown in Fig.3(a). By using the KVL for the whole state circuit, the KVL equation can be obtained as:


 Fig. 3. State circuits of the proposed SC converter: (a) Phase  $\Phi_a$ ; (b) Phase  $\Phi_b$ .

$$\text{Phase } \Phi_a: \begin{bmatrix} V_{C11} \\ V_{C21} \\ \vdots \\ V_{Cn1} \\ V_H \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & \dots & 0 \\ 1 & 1 & 0 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & 1 & \dots & 0 \\ 1 & 1 & 1 & \dots & 1 \end{bmatrix} \begin{bmatrix} V_L \\ V_{C12} \\ V_{C22} \\ \vdots \\ V_{Cn2} \end{bmatrix} \quad (1)$$

For the clock phase  $\Phi_b$ , as shown in Fig.3(b), the negative electrodes of  $V_L$ ,  $V_H$  and  $C_{i2}$  ( $i=1, 2, \dots, n$ ) are connected together. Similarly, the KVL equation can be obtained as:

$$\text{Phase } \Phi_b: \begin{bmatrix} V_{C12} \\ V_{C22} \\ \vdots \\ V_{Cn2} \\ V_H \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & \dots & 0 \\ 1 & 1 & 0 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & 1 & \dots & 0 \\ 1 & 1 & 1 & \dots & 1 \end{bmatrix} \begin{bmatrix} V_L \\ V_{C11} \\ V_{C21} \\ \vdots \\ V_{Cn1} \end{bmatrix} \quad (2)$$

According to equations (1) and (2), the ideal voltage transfer relationship for the proposed SC converter can be derived and is given in:

$$\begin{bmatrix} 2^0 \\ 2^1 \\ \vdots \\ 2^{n-1} \end{bmatrix} V_L = \begin{bmatrix} V_{C11} \\ V_{C21} \\ \vdots \\ V_{Cn1} \end{bmatrix} = \begin{bmatrix} V_{C12} \\ V_{C22} \\ \vdots \\ V_{Cn2} \end{bmatrix} = \begin{bmatrix} 1/2^{2^n} \\ 1/2^{2^{n-1}} \\ \vdots \\ 1/2^1 \end{bmatrix} V_H \quad (3)$$

### C. With-Load Analysis

When one terminal ( $V_L$  or  $V_H$ ) of the proposed converter is used as an input terminal and the other is connected with a load, current flows from the input terminal to the output node through all of the DMSC cells. Each capacitor operates alternatively in the charging and discharging states during each switching cycle. Considering the on-resistance of the switches and the ESR of the capacitors, state circuits of the proposed exponential-gain SC converter are depicted in Figs. 4(a) and 4(b) for phases  $\Phi_a$  and  $\Phi_b$ , respectively.  $R_{k1}$  and  $R_{k2}$  ( $k=1, 2, \dots, n$ ) are the ESR of  $C_{k1}$  and  $C_{k2}$ , and the on-resistances of the corresponding switches are regarded as a part of them.

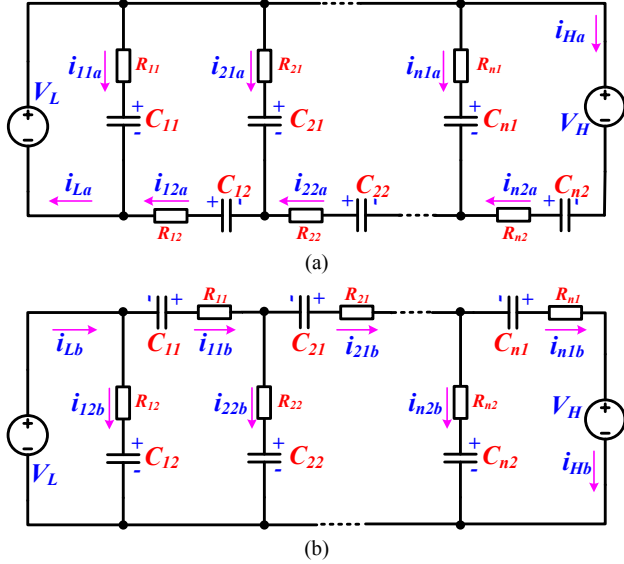


Fig. 4. State circuits with parasitic resistances: (a) Phase  $\Phi_a$ ; (b) Phase  $\Phi_b$ .

When  $V_L$  is the input terminal and  $V_H$  is the output terminal, the SC converter operates in the step-up mode and all of the currents denoted in Figs. 4(a) and 4(b) are positive, and vice-versa. By using the KCL for the state circuits, the KCL equations can be obtained as:

$$\text{Phase } \Phi_a: \begin{bmatrix} i_{La} \\ i_{12a} \\ i_{22a} \\ \vdots \\ i_{n2a} \end{bmatrix} = \begin{bmatrix} 1 & 1 & \dots & 1 & 1 \\ 0 & 1 & \dots & 1 & 1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & 1 & 1 \\ 0 & 0 & \dots & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{11a} \\ i_{21a} \\ \vdots \\ i_{n1a} \\ i_{Ha} \end{bmatrix} \quad (4)$$

$$\text{Phase } \Phi_b: \begin{bmatrix} i_{Lb} \\ i_{11b} \\ i_{21b} \\ \vdots \\ i_{n1b} \end{bmatrix} = \begin{bmatrix} 1 & 1 & \dots & 1 & 1 \\ 0 & 1 & \dots & 1 & 1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & 1 & 1 \\ 0 & 0 & \dots & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{12b} \\ i_{22b} \\ \vdots \\ i_{n2b} \\ i_{Hb} \end{bmatrix} \quad (5)$$

In the stable state, the amount of charge flowing into and out of each capacitor should be the same during one switching cycle. Based on the assumptions that the two capacitors employed in each cell are the same and that both are represented by  $C_k$ , i.e.  $C_{k1}=C_{k2}=C_k$ , the relationship of charge flowing into/out of all of the capacitors and through the two terminals can be derived from (4) and (5), which is expressed as:

$$\begin{bmatrix} \Delta Q_L \\ \Delta Q_1 \\ \vdots \\ \Delta Q_{n-1} \\ \Delta Q_n \end{bmatrix} = \begin{bmatrix} 1 & 0 & \dots & 0 & 0 \\ 0 & 1 & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & 1 & 0 \\ 0 & 0 & \dots & 0 & 1 \end{bmatrix} \begin{bmatrix} 4\Delta Q_1 \\ 2\Delta Q_2 \\ \vdots \\ 2\Delta Q_n \\ \Delta Q_H/2 \end{bmatrix} \quad (6)$$

where  $\Delta Q_L$  and  $\Delta Q_H$  are the charge flowing through the terminals  $V_L$  and  $V_H$ , respectively. In addition,  $\Delta Q_k$  ( $k=1, 2, \dots, n$ ) is the amount of charge transferred into/out of the capacitor  $C_k$ , during one switching cycle.

The voltage ripples across the capacitors can be derived

from equation (6) and is expressed by:

$$\begin{bmatrix} \Delta V_{C1} \\ \Delta V_{C2} \\ \vdots \\ \Delta V_{C(n-1)} \\ \Delta V_{Cn} \end{bmatrix} = \begin{bmatrix} 2^{-1}/C_1 \\ 2^{-2}/C_2 \\ \vdots \\ 2^{-(n-1)}/C_{n-1} \\ 2^{-n}/C_n \end{bmatrix} \frac{I_L}{2f_s} = \begin{bmatrix} 2^{n-1}/C_1 \\ 2^{n-2}/C_2 \\ \vdots \\ 2^1/C_{n-1} \\ 2^0/C_n \end{bmatrix} \frac{I_H}{2f_s} \quad (7)$$

where  $f_s$  is the switching frequency of the converter. In addition,  $I_L$  and  $I_H$  are the average currents flowing through the terminals  $V_L$  and  $V_H$ , respectively.

Additionally, the power conversion efficiency of the proposed converter can be expressed by using the input energy and output energy during one switching cycle. Therefore, according to (6), the efficiency of the SC converter can be expressed as:

$$\text{Step-up mode: } \eta = \frac{\Delta Q_H V_H}{\Delta Q_L V_L} = \frac{V_H}{2^n V_L} \quad (8)$$

$$\text{Step-down mode: } \eta' = \frac{\Delta Q_L V_L}{\Delta Q_H V_H} = \frac{V_L}{2^n V_H} \quad (9)$$

### III. MODELING OF THE PROPOSED SC CONVERTER

#### A. Modeling of a Single DMSC Cell

All of the DMSC cells employed in the proposed converter are made up of two symmetrical phases. There are the same average voltage and ripple, and inverse operation for the two capacitors  $C_{k1}$  and  $C_{k2}$ . During phase  $\Phi_a$ , the voltage across  $C_{k1}$  increases from  $V_{Ck\_min}$  to  $V_{Ck\_max}$ , while the voltage across  $C_{k2}$  decreases from  $V_{Ck\_max}$  to  $V_{Ck\_min}$ . On the other hand, the voltage across  $C_{k1}$  decreases from  $V_{Ck\_max}$  to  $V_{Ck\_min}$ , while the voltage across  $C_{k2}$  increases from  $V_{Ck\_min}$  to  $V_{Ck\_max}$  during the period of phase  $\Phi_b$ . For the two operation stages, the sum voltage  $V_k = V_{Ck1} + V_{Ck2}$  is almost constant and its ripple is far smaller than that for each of the capacitors and can be neglected. The two states can be generally depicted by Fig. 5(a).

Based on the above analysis, the input and output voltages of the DMSC cell,  $V_{k-1}$  and  $V_k$ , can both be regarded as constant. The operation of the DMSC cell, during half of a switching cycle can be mathematically described as:

$$\begin{cases} i_{k\_cr}(t) = \frac{V_{k-1} - V_{Ck\_min}}{R_k} e^{-\frac{t}{R_k C_k}} \\ V_{Ck\_cr}(t) = (V_{k-1} - V_{Ck\_min})(1 - e^{-\frac{t}{R_k C_k}}) + V_{Ck\_min} \end{cases} \quad (10)$$

$$\begin{cases} i_{k\_dr}(t) = \frac{V_{Ck\_max} + V_{k-1} - V_k}{R_k} e^{-\frac{t}{R_k C_k}} \\ V_{Ck\_dr} = V_{Ck\_max} - (V_{Ck\_max} + V_{k-1} - V_k)(1 - e^{-\frac{t}{R_k C_k}}) \end{cases} \quad (11)$$

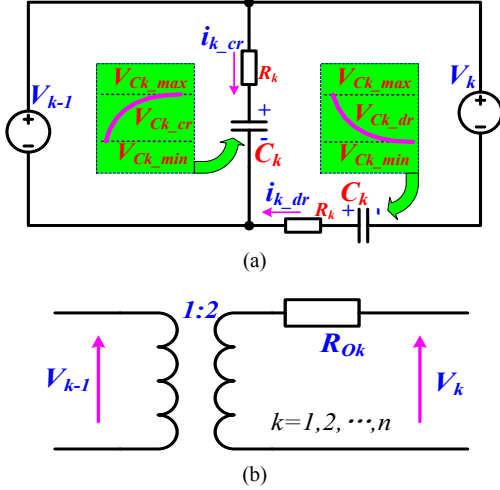


Fig. 5. Single DMSC cell: (a) State circuit; (b) Model.

where  $i_{k,cr}$  and  $i_{k,dr}$  represent the charging and discharging currents of the capacitors, respectively. Both of them have the same average value  $I_k$  since the two phases  $\Phi_a$  and  $\Phi_b$  are fully complementary and evenly divide a switching cycle. Therefore, the voltage transfer relationship can be derived as:

$$V_k = 2V_{k-1} - \frac{I_k(1 + e^{-\frac{1}{2f_s R_k C_k}})}{2f_s C_k(1 - e^{-\frac{1}{2f_s R_k C_k}})} \quad (12)$$

where  $f_s$  is the switching frequency. In addition,  $I_k$  is the average value of both the charging and discharging currents,  $i_{k,cr}$  and  $i_{k,dr}$ , and it is the output average current of the DMSC cell.

Therefore, the output impedance of a single DMSC cell for the step-up mode is expressed by:

$$\text{Step-up mode: } R_{Ok} = \frac{1 + e^{-\frac{1}{2f_s R_k C_k}}}{2f_s C_k(1 - e^{-\frac{1}{2f_s R_k C_k}})} \quad (13)$$

Similarly, the output impedance for the step-down mode can be derived as:

$$\text{Step-down mode: } R'_{Ok} = \frac{1 + e^{-\frac{1}{2f_s R_k C_k}}}{8f_s C_k(1 - e^{-\frac{1}{2f_s R_k C_k}})} \quad (14)$$

An equivalent model of the single DMSC cell in the proposed converter for bidirectional operation can be generally described as shown in Fig. 5(b).

### B. Modeling of the Proposed SC Converter

Considering that the proposed SC converter is cascaded by multiple DMSC cells, the model of the proposed converter can also be developed as shown in the upper half of Fig. 6.

For the step-up operation, the terminal  $V_L$  is used as the input terminal and the load is connected to the terminal  $V_H$ .

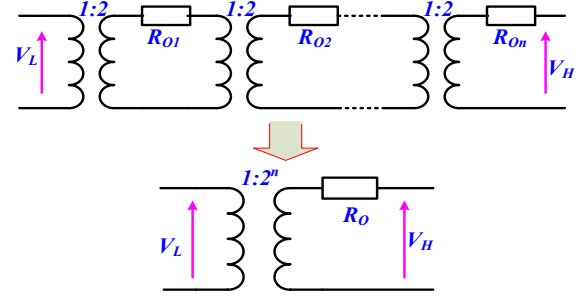


Fig. 6. Model of the proposed converter.

The voltage transfer relationship can be derived from (12), and is given as:

$$\begin{bmatrix} V_n \\ V_{n-1} \\ \vdots \\ V_2 \\ V_1 \end{bmatrix} = \begin{bmatrix} 2V_{n-1} \\ 2V_{n-2} \\ \vdots \\ 2V_1 \\ 2V_{in} \end{bmatrix} - \begin{bmatrix} R_{On} & 0 & \cdots & 0 & 0 \\ 0 & R_{O(n-1)} & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & R_{O2} & 0 \\ 0 & 0 & \cdots & 0 & R_{O1} \end{bmatrix} \begin{bmatrix} I_n \\ I_{n-1} \\ \vdots \\ I_2 \\ I_1 \end{bmatrix} \quad (15)$$

where  $I_k$  and  $R_{Ok}$  ( $k=1, 2, \dots, n$ ) are the average output current and output impedance for each of the SC cells, respectively. In addition,  $V_n$  and  $I_n$  are the actual output voltage and current of the proposed converter in the step-up operation. An equivalent model of the proposed converter for the step-up mode can be further developed as shown in the lower half of Fig. 6, and the voltage transfer relationship is developed as:

$$V_O = 2^n V_{in} - I_O \sum_{k=1}^n 2^{2(n-k)} R_{Ok} \quad (16)$$

This means the output impedance of the whole SC converter can be expressed as:

$$R_O = \sum_{k=1}^n 2^{(n-k)} R_{Ok} = \frac{1}{f_s} \sum_{k=1}^n \frac{2^{2(n-k)-1} (1 + e^{-\frac{1}{2f_s R_k C_k}})}{C_k (1 - e^{-\frac{1}{2f_s R_k C_k}})} \quad (17)$$

Similarly, when  $V_H$  is used as the input terminal, the voltage transfer relationship and the output impedance for the step-down mode can be developed, and they are given as:

$$V_O' = 2^{-n} V_{in}' - I_O' \sum_{k=1}^n 2^{-2(k-1)} R'_{Ok} \quad (18)$$

$$R_O' = \sum_{k=1}^n 2^{-2(k-1)} R'_{Ok} = \frac{1}{f_s} \sum_{k=1}^n \frac{1 + e^{-\frac{1}{2f_s R_k C_k}}}{2^{2k+1} C_k (1 - e^{-\frac{1}{2f_s R_k C_k}})} \quad (19)$$

In the case of ignoring the impact of the parasitic resistors, the output impedance of (17) and (19) can be simplified as:

$$R_{OC} = \frac{1}{f_s} \sum_{k=1}^n \frac{2^{2(n-k)-1}}{C_k} \quad (20)$$

$$R'_{OC} = \frac{1}{f_s} \sum_{k=1}^n \frac{1}{2^{2k+1} C_k} \quad (21)$$

By comparing (17) with (19), (20) and (21), the relationship between the output impedances of both the step-up and step-down operation modes can be expressed as:

$$\frac{R_O}{R_O'} = \frac{R_{OC}}{R_{OC}'} = 4^n \quad (22)$$

Hence, the mode of Fig. 6 can be applied for both the step-up and step-down operation modes of the proposed bidirectional SC converter.

#### IV. OPTIMIZATION OF THE OUTPUT IMPEDANCE

##### A. Impact of the Capacitance Distribution

It can be seen from (20) and (21) that larger capacitances are required for a smaller output impedance. However, in practice, the values of the capacitors cannot be infinitely large and a larger capacitance means a higher cost and a larger size. For the proposed converter, although the two capacitors  $C_{k1}$  and  $C_{k2}$  employed in each of the DMSC cells need to be the same, i.e.  $C_{k1}=C_{k2}=C_k$ , the capacitors for different cells may be varied. Therefore, the method to allocate the total capacitance  $C$  to all of the capacitors for the minimum output impedance is a topic that should be explored.

When the total capacitance  $C$  is evenly distributed to all of the DMSC cells, the value of each capacitor is  $C_k=C/2n$ . According to (7), the voltage ripple across  $C_k$  is decreased exponentially, and is given as:

$$\Delta V_{C_{k-1}} = 2\Delta V_{C_k} \quad (23)$$

Ignoring the impact of the parasitic resistances, the output impedance for the step-up mode can be calculated according to (20), and is given as:

$$R_{OC} = \frac{n(4^n - 1)}{3f_s C} \quad (24)$$

##### B. Minimum Output Impedance

In order to obtain the minimum output impedance for the constant total capacitance  $C$ ,  $C_i$  is described as  $C_i=C/2-C_2-\dots-C_k-\dots-C_n$ . Substituting this into (20) and letting the partials with respect to the capacitance  $C_k$  equal to zero, i.e.

$$\frac{\partial R_{OC}}{\partial C_k} = \frac{1}{f_s} \left[ \frac{2^{2n-3}}{(C/2 - C_2 - \dots - C_k - \dots - C_n)^2} - \frac{2^{2(n-k)-1}}{C_k^2} \right] = 0 \quad (25)$$

As a result, the capacitance  $C_k$  can be expressed as:

$$C_k = 2^{1-k} C_1 \quad (26)$$

Considering that the total capacitance is  $C$  and  $k$  is ranged from 1 to  $n$ , the capacitance  $C_k$  can be further expressed by:

$$C_k = \frac{2^{n-k-1} C}{2^n - 1} \quad (27)$$

Then the minimum output impedance can be obtained by

substituting (27) into (20), and is given as:

$$R_{OC} = \frac{(2^n - 1)^2}{f_s C} \quad (28)$$

The analysis above is mainly discussed for the step-up operation mode of the proposed converter. Similarly, according to (22), the minimum output impedance for the step-down operation mode is obtained in the same case.

#### V. COMPARISON WITH OTHER WORKS

In practice, the size and cost of a SC converter is dominated by the total capacitance  $C$  and the number of switches. As mentioned before, a smaller output impedance means a higher power efficiency. With the assumption that all of the parasitic resistances are ignored, the output impedance of a SC converter is determined by the switching frequency, the total capacitance  $C$  and the capacitance distribution. For different high order SC converters like the SP, Dickson and Fibonacci, there are different capacitance distribution laws for their minimum output impedances.

Table I lists the characteristics of the proposed and other high order SC converters with  $n$  stages. These characteristics include the voltage gain  $m$ , the best capacitance distribution law, the number of switches, the minimum output impedance and the relationship between the minimum output impedance and the voltage gain. This shows there are the same voltage gains and the same best capacitance distribution law as well as the same minimum output impedance for both the SP and Dickson converters. Common characteristics are also found in both the conventional and proposed exponential-gain SC converters. However, the number of switches required in the Dickson and the proposed converters is far less than that for the SP and conventional exponential-gain converters.

A noticeable characteristic is that there is a common relationship between the minimum output impedance and the voltage gain for all of the high order SC converters listed in Table I. This means that with the same total capacitance  $C$  and switching frequency  $f_s$ , using different topologies to obtain the same voltage gain, the same output impedance and power conversion efficiency can be developed. The more intuitive relationship is depicted in Fig. 7.

Additionally, the number of switches required for different DC converters is listed in the fourth column of Table I. In addition, the relationships between the number of switches and the voltage gain are depicted in Fig. 8. This figure shows that the minimum and maximum numbers of switches are required in the proposed exponential-gain and SP converters, for the same voltage gain.

Overall, the proposed SC converter is more suitable for high-voltage-gain applications. However, its flexibility is inferior to the Dickson SC converter.

TABLE I  
 CHARACTERISTICS OF DIFFERENT TWO-PHASE SC CONVERTERS

Types of converters	Gain $m$	Cap. distribution	No. of switch	Output impedance	$R_{oc} = f(m)$
SP	$n+1$	$C_k = \frac{C}{n}$	$3n+1$	$\frac{n^2}{f_s C}$	$\frac{(m-1)^2}{f_s C}$
Dick.			$n+5$	$\frac{n^2}{f_s C}$	
Fib.	$F_{n+1}$	$C_k = \frac{F_{n-k} C}{F_{n+1} - 1}$	$3n+1$	$\frac{(F_{n+1} - 1)^2}{f_s C}$	
Fig.1	$2^n$	$C_k = \frac{2^{n-k-1} C}{2^n - 1}$	$6n+2$	$\frac{(2^n - 1)^2}{f_s C}$	
Fig.2			$4n$	$\frac{(2^n - 1)^2}{f_s C}$	

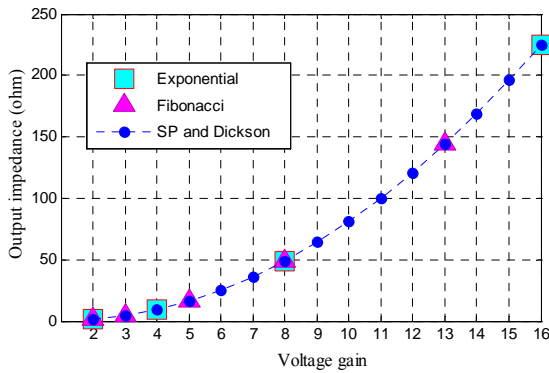
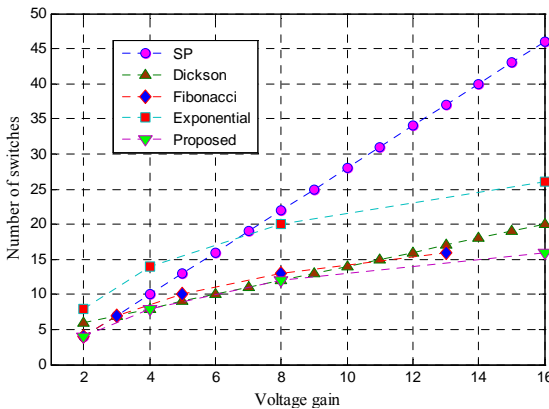

 Fig. 7. Output impedance versus the voltage gain when  $f_s C = 1 (\text{Hz} \times \text{F})$ .


Fig. 8. Number of switches as function of the voltage gain.

## VI. EXPERIMENTAL RESULTS

In order to analyze the properties of the proposed exponential-gain SC converter, a 6-24V bidirectional prototype has been built by cascading two DMSC cells, as shown in Fig. 9. Eight MOSFETs with on-resistances of 11m $\Omega$  are selected for the switches. In the first DMSC cell, both of the capacitors  $C_{11}$  or  $C_{12}$  are made up of two 1000 $\mu\text{F}/55\text{m}\Omega$  electrolytic capacitors connected in parallel. The capacitors  $C_{21}$  and  $C_{22}$  in the second DMSC cell are both single 1000 $\mu\text{F}/55\text{m}\Omega$  electrolytic capacitors. Additionally, a 1000 $\mu\text{F}$  electrolytic capacitor is used in the low voltage terminal as a filter. The controller is developed by IR2153 and the isolated

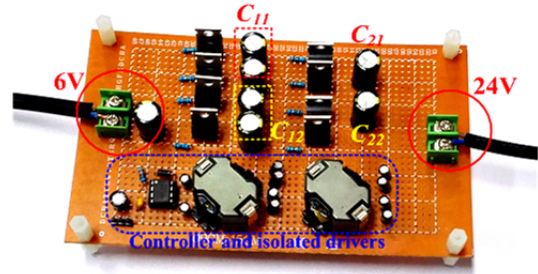


Fig. 9. Prototype of a 6-24V bidirectional converter.

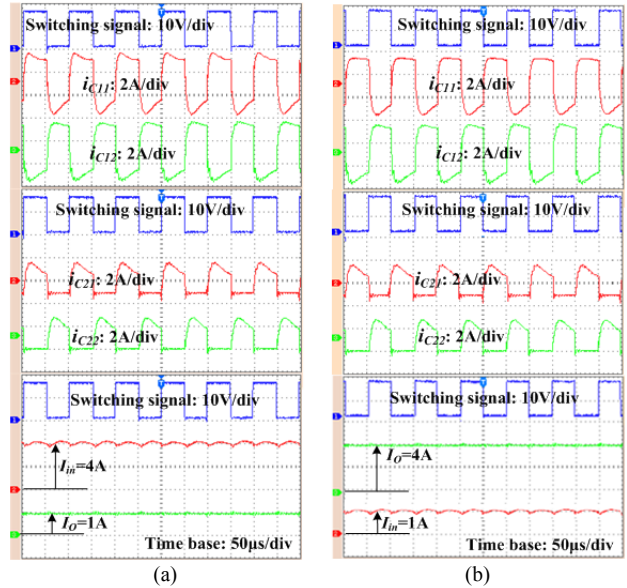


Fig. 10. Current waveforms of the prototype converter: (a) Step-up operation; (b) Step-down operation.

gate driver is completed based on pulse transformers. In order to reduce the effect of the ESL and switching losses, the prototype works at a 10 kHz switching frequency. To improve the power density, the isolated pulse transformer driver can be replaced by an optocoupler or another floating gate driver. In addition, ceramic capacitors and a higher switching frequency can be used in practical industrial applications.

When the low voltage terminal of the prototype circuit is connected with a 6V voltage source and the high voltage terminal is connected to an electronic load with constant output current  $I_o = 1\text{A}$ , the currents flowing through the capacitors as well as the power source current  $I_{in}$  are captured as shown in Fig. 10(a). Similarly, when the high voltage terminal of the prototype circuit is connected with a 24V voltage source and the low voltage terminal is connected to an electronic load with a constant current 4A, the current waveforms are shown in Fig. 10(b). It can be seen that the average charging and discharging currents are about 2A for  $C_{11}$  and  $C_{12}$ , and about 1A for  $C_{21}$  and  $C_{22}$ . The average current of the low voltage terminal is almost four times that in the high voltage terminal.

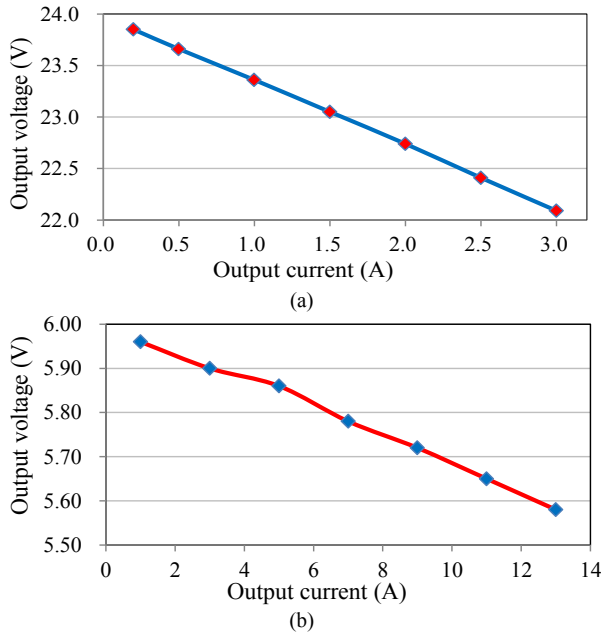


Fig. 11. Output voltage versus output current: (a) Step-up operation (6V to 24V); (b) Step-down operation (24V to 6V).

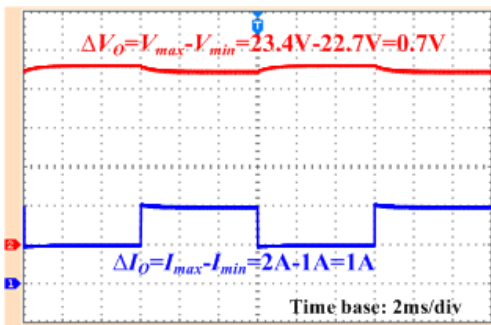


Fig. 12. Output voltage transient waveform of the prototype versus the output current.

As mentioned in (16) and (18), increasing the output current decreases the output voltage. For the bidirectional prototype converter, the load regulations for the step-up and step-down operations are measured as shown in Figs. 11(a) and 11(b), respectively. The output voltage falls from 23.85V when the output current is 0.2A to 22.09V when the output current increases to 3A for the step-up operation. Similarly, it decreases from 5.96V to 5.58V when the output current rises from 1A to 13A, for the step-down operation. The practical output impedances of the prototype converter are 0.64 $\Omega$  for the step-up mode and 33m $\Omega$  for the step-down mode, which are slightly larger than the theoretical values of 0.51 $\Omega$  and 31m $\Omega$ , respectively.

Fig. 12 shows output voltage transient waveforms of the prototype operating in the step-up mode when the output current changes between 1A and 2A. As mentioned before, the voltage drop caused by the output impedance of the converter reduces the output voltage while a higher output current means a lower output voltage.

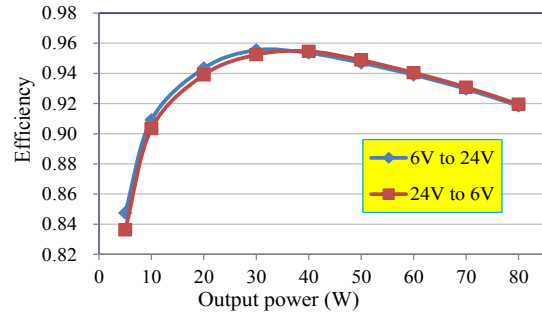


Fig. 13. Measured efficiency of the prototype converter.

Fig. 13 shows the efficiency of the bidirectional prototype converter with different output powers. This indicated that there is almost the same power conversion efficiency for both the step-up and step-down operation modes under the same output power. In addition, the maximum efficiencies for the step-up and step-down operations are 95.5% and 95.3%, respectively. Both of them are achieved at round 30W output power.

## VII. CONCLUSIONS

A new exponential-gain DC-DC converter for a bidirectional power flow is developed based on the SC technique. The voltage conversion characteristics and model are derived using the KVL and KCL principles for the proposed converter. The effect of the capacitance distribution on the output impedance is discussed. This indicates there is the same minimum output impedance between the proposed converter and other existing two-phase SC converters for the same voltage transfer ratio. Of course, there is a shortcoming in the proposed converter since the input and output terminals cannot share a common neutral. A two-stage prototype converter designed for a 6-24V bidirectional power flow was built based on the theoretical analysis. Experimental results support the theoretical analysis and the practical output impedance since the step-up and step-down operations are both just slightly larger than their theoretical values.

## ACKNOWLEDGMENT

This work was supported in part by the Natural Science Foundation of Guangdong Province (No.2017A030313316), in part by the Science and Technology Planning Project of Guangdong Province (No.2017A010102013), and in part by the Guangdong University of Technology under Grant from the Financial and Education Department of Guangdong Province 2016[202]: Key Discipline Construction Program.

## REFERENCES

- [1] G. Villar-Pique, H. J. Bergveld, and E. Alarcon, "Survey and benchmark of fully integrated switching power converters: Switched-capacitor versus inductive approach," *IEEE Trans. Power Electron.*, Vol. 28, No. 9, pp. 4156-4167, Sep. 2013.

- [2] S. V. Cheong, H. Chung, and A. Ioinovici, "Inductorless DC-to-DC converter with high power density," *IEEE Trans. Ind. Electron.*, Vol. 41, No. 2, pp. 208-215, Apr. 1994.
- [3] F. Ueno, T. Inoue, I. Oota, and I. Harada, "Novel type DC-AC converter using a switched-capacitor transformer," *Proc. European Conference on Circuit Theory and Design*, pp. 1181-1184, Sep. 1993.
- [4] H. S.-H. Chung, "Design and analysis of a switched-capacitor-based step up DC/DC converter with continuous input current," *IEEE Trans. Circuits Syst. I, Fundam. Theory*, Vol. 46, No. 6, pp. 722-730, Jun. 1999.
- [5] S. Xiong, Y. Huang, S.-C. Tan, and S. Y. R. Hui, "Morphing switched-capacitor converters with variable conversion ratio," *IEEE Trans. Power Electron.*, Vol. 31, No. 8, pp. 5680-5693, Aug. 2016.
- [6] Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-phase control: Achieving complete soft-charging operation of a Dickson switched-capacitor converter," *IEEE Trans. Power Electron.*, Vol. 31, No. 1, pp. 770-782, Jan. 2016.
- [7] Y. C. Fong, K.W.E. Cheng, Y. Ye, and Y. C. Chan, "Centralized regulation scheme for a parallel-mode switched-capacitor converter system with simple unit commitment," *IEEE Trans. Ind. Electron.*, Vol. 64, No. 8, pp. 6149-6158, Aug. 2017.
- [8] Y. Ye and K.W.E. Cheng, "Voltage-gap modeling method for single-stage switched-capacitor converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, Vol. 2, No. 4, pp. 808-813, Dec. 2014.
- [9] Y. Ye and K. W. E. Cheng, "Analysis and optimization of switched capacitor power conversion circuits with parasitic resistances and inductances," *IEEE Trans. Power Electron.*, Vol. 32, No. 3, pp. 2018-2028, Mar. 2017.
- [10] B. Wu, L. Wang, L. Yang, K. M. Smedley, and S. Singer, "Comparative analysis of steady-state models for a switched-capacitor converter," *IEEE Trans. Power Electron.*, Vol. 32, No. 2, pp. 1186-1197, Feb. 2017.
- [11] S. Iqbal, "A hybrid symmetrical voltage multiplier," *IEEE Trans. Power Electron.*, Vol. 29, No. 1, pp. 6-12, Jan. 2014.
- [12] C.-M. Young, M.-H. Chen, T.-A. Chang, C.-C. Ko, and K.-K. Jen, "Cascade cockcroft-walton voltage multiplier applied to transformerless high step-up DC-DC converter," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 2, pp. 523-537, Feb. 2013.
- [13] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, pp. 374-378, 1976.
- [14] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated DC-DC converters," *IEEE Trans. Power Electron.*, Vol. 23, No. 2, pp. 871-887, Feb. 2008.
- [15] O.-Y. Wong, H. Wong, W.-S. Tam, and C.-W. Kok, "An overview of charge pumping circuits for flash memory applications," *IEEE 9th International Conference on ASIC (ASICON)*, pp. 116-119, 2011.
- [16] T. Tanzawa and S. Atsumi, "Optimization of word-line booster circuits for low-voltage flash memories," *IEEE J. Solid-State Circuits*, Vol. 34, No. 8, pp. 1091-1098, Aug. 1999.
- [17] J. Shin, I.-Y. Chung, Y. J. Park, and M. H. Shick, "A new charge pump without degradation in threshold voltage due to body effect," *IEEE J. Solid-State Circuits*, Vol. 35, No. 8, pp. 1227-1230, Aug. 2000.
- [18] J. S. Brugler, "Theoretical performance of voltage multiplier circuits," *IEEE J. Solid-State Circuits*, Vol. SSC-6, No. 3, pp. 132-135, Jun. 1971.
- [19] F. Ueno, T. Inoue, I. Oota, and I. Harada, "Emergency power supply for small computer systems," in *Proc. IEEE Int. Conf. Circuits Syst.*, pp. 1065-1068, 1991.
- [20] L. K. Chang and C. H. Hu, "High efficiency MOS charge pumps based on exponential-gain structure with pumping gain increase circuits," *IEEE Trans. Power Electron.*, Vol. 21, No. 3, pp. 826-831, May 2006.
- [21] C. Y. Tsui, H. Shao, W. H. Ki, and F. Su, "Ultra-low voltage power management and computation methodology for energy harvesting applications," *Proc. IEEE Symp. VLSI Circuit*, pp. 316-319, 2005.
- [22] L. Gobbi, A. Cabrini, and G. Torelli, "A discussion on exponential-gain charge pump," *18th European Conference on Circuit Theory and Design*, pp. 615-618, 2007.



**Yuanmao Ye** received his B.S. degree from University of Jinan, Jinan, China, in 2007; his M.S. degree from the South China University of Technology, Guangzhou, China, in 2010; and his Ph.D. degree from the Hong Kong Polytechnic University, Hong Kong, China, in 2016. From 2010 to 2014, he was a Researcher in the Department of Electrical

Engineering, Hong Kong Polytechnic University. He is presently working as a Professor in the School of Automation, Guangdong University of Technology, Guangzhou, China. His current research interests include various dc-dc power converters, switched-capacitor techniques and their applications, multilevel inverters, power conversion and energy management for smart-grids, protection and control techniques for DC distribution, and wireless charging technique for EVs.



**Wei Peng** was born in Hunan, China, in 1995. He received his B.S. degree from the Hunan University of Humanities, Science and Technology, Loudi, China, in 2017. He is presently working towards his M.S. degree at Guangdong University of Technology, Guangzhou, China. His current research interests include multilevel inverters, power

converters and intelligent control.



**Bijia Jiang** was born in Hunan, China, in 1994. She received her B.S. degree from the Hunan Institute of Engineering, Xiangtan, China, in 2013. She is presently working towards her M.S. degree at the Guangdong University of Technology, Guangzhou, China. Her current research interests include DC/DC converters and the control of DC

microgrids.





**Xianyong Zhang** received his B.S. degree from the Changchun University of Science and Technology, Changchun, China, in 1999; and his M.S. and Ph.D. degrees from the South China University of Technology, Guangzhou, China, in 2002 and 2007, respectively. From 2007 to 2014, he was with the Solar Power Generation and Microgrid Lab, Guangzhou Institute of Energy Conversion, Chinese Academy of Sciences, Guangzhou, China. He is presently working as an Associate Professor in the College of Automation, Guangdong Polytechnic Normal University, Guangzhou, China. His current research interests include the control and power electronics technology in renewable energy.