

Novel Single Switch DC-DC Converter for High Step-Up Conversion Ratio

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Abstract

This paper presents a new structure for a step up dc-dc converter, which has several advantageous features. Firstly, the input dc source and the clamped capacitor are connected in series to transfer energy to the load through dual voltage multiplier cells. Therefore, the proposed converter can produce a very high voltage and a high conversion efficiency. Secondly, a double voltage clamped circuit is introduced to the primary side of the coupled inductor. The energy of the leakage inductance of the coupled inductor is recycled and the inrush current problem of the clamped circuits can be shared equally by two synchronous clamped capacitors. Therefore, the voltage spike of the switch tube is solved and the current stress of the diode is reduced. Thirdly, dual voltage multiplier cells can absorb the leakage inductance energy of the secondary side of the coupled inductor to obtain a higher efficiency. Fourthly, the active switch turns on at almost zero current and the reverse-recovery problem of the diodes is alleviated due to the leakage inductance, which further improves the conversion efficiency. The operating principles and a steady-state analysis of the continuous, discontinuous and boundary conduction modes are discussed in detail. Finally, the validity of this topology is confirmed by experimental results.

Key words: Clamp circuits, DC-DC, Dual voltage multiplier cells, Floating active switch, Switched-coupled-inductor

I. INTRODUCTION

In recent years, some problems such as fossil energy depletion, global warming and environmental pollution have become more and more serious. Therefore, distributed generation (DG) systems based on renewable energy sources have attracted considerable attention around the world, including photovoltaic (PV) generation systems, wind generation, fuel cell systems, etc. [1]-[8]. However, the output voltage of renewable energy sources is low and variable. Therefore, high step up dc-dc converters with a high efficiency are generally required as the front-end stage for renewable energy generation systems.

Although the basic boost converter theoretically has the function for lifting input voltage, it cannot obtain a very large conversion ratio with a high power and high efficiency due to its extreme duty cycle. This is because the extreme duty cycle causes large conduction losses and a serious diode reverse

recovery problem, which leads to a sharp decline in conversion efficiency [9]-[11]. In addition, a forward or flyback dc-dc converter can be used to increase the voltage gain by adjusting the turns ratio of the isolation transformer. However, the primary switch and secondary diode suffer from a high voltage spike, which greatly affects the efficiency of the converter. In order to solve this problem, active-clamp and non-dissipative snubber technologies are employed. However, an extra power switch and driver are needed, and the energy of the primary leakage inductance is still not easy to recycle, which makes the pursuit of a high conversion efficiency very difficult. In recently published studies [12], [13], some high gain boost converters have been presented based on diverse technologies, including the cascaded types, the switched capacitor/inductor types, the voltage-lift types [14]-[19], and the coupled inductor types [20]-[37]. These technologies play a positive role in raising the voltage gain. However, they have their advantages and disadvantages. Therefore, it makes sense to combine several technologies for putting forward high efficiency and high step up converters.

This paper proposes a new single switch dc-dc converter topology that adopts the switched capacitor and coupled inductor techniques. On the basis of a Zeta converter, this

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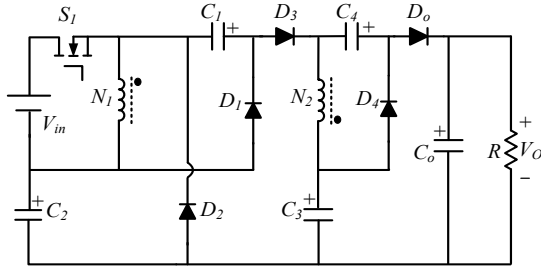


Fig. 1. Circuit configuration of the proposed converter.

topology substitutes a coupled inductor for the input inductance of the Zeta converter. Furthermore, two clamped circuits are introduced to the primary side of the coupled inductor. The single switch dc-dc converter topology, as shown in fig. 1, is configured from a floating active switch S_1 and a coupled inductor, two passive clamped circuits, and dual voltage multiplier cells. It should be added that the two passive clamp circuits are composed of the active switch S_1 , the clamped capacitor C_1 and the clamped capacitor C_2 . In addition, it should be added that dual voltage multiplier cells are composed of the coupled inductor secondary side winding, the capacitor C_4 , the diode D_4 , the capacitor C_3 and the diode D_3 . The features of the proposed converter are as follows. 1) Dual passive clamped circuits recycle the leakage inductor energy of the coupled inductor, share the inrush current and clamp the voltage stress of the active switch to a lower level. Moreover, the clamp capacitors are connected in series to discharge for the purpose of extending the voltage gain. 2) The switched capacitors in the voltage multiplier cells are synchronously charged from different flows, and they are discharged in series to obtain a higher voltage gain. 3) Power switch turn on occurs with almost zero current, which significantly reduces the conduction loss. In addition, the current variation ratio (di/dt) presented by all of the diodes is limited due to the leakage inductance of the coupled inductor.

II. OPERATIONAL PRINCIPLE OF THE PROPOSED CONVERTER

Fig. 2 shows an equivalent circuit of the proposed converter. The circuit model of the coupled inductor includes the magnetizing inductor L_m , the primary and secondary leakage inductors L_{k1} and L_{k2} , and the ideal transformer primary and secondary windings N_1 and N_2 .

In order to simplify the circuit analysis, the following assumptions are made.

- 1) All of the power devices are ideal. However, the leakage inductance of the coupled inductor is taken into consideration.
- 2) The capacitors $C_4 \sim C_0$ are sufficiently large. Therefore, the voltages across these capacitors are constant during one period.

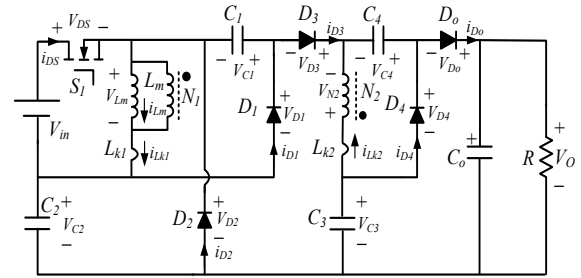


Fig. 2. Equivalent circuit of the proposed converter.

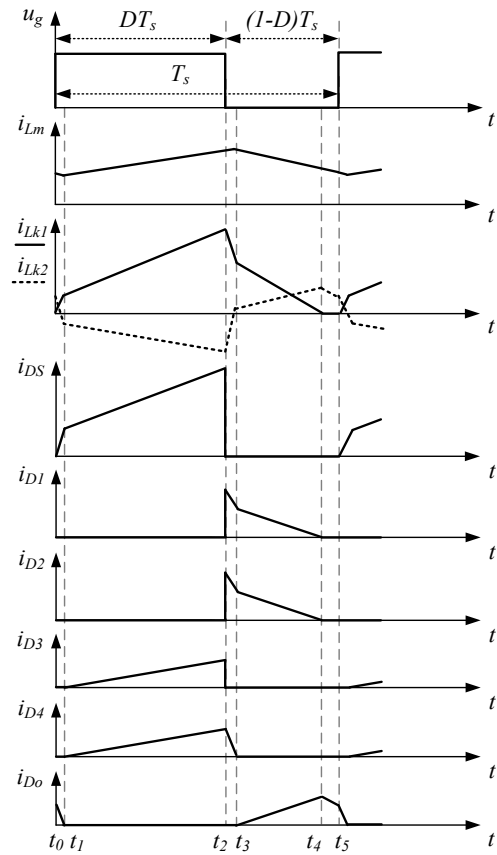


Fig. 3. Key waveforms of the proposed converter during the CCM operation.

- 3) The turns ratio n of the coupled inductor is equal to N_2 / N_1 .

The working principles of the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) are described as follows.

A. CCM Operation

This section presents the CCM operation principle of the proposed converter. Fig. 3 represents several key waveforms during one switching period. The five operating modes are depicted in Fig. 4.

Mode I $[t_0-t_1]$: At $t=t_0$, the switch S_1 is turned on, Fig. 4(a) depicts the current flow path of this stage. Only the diode D_0

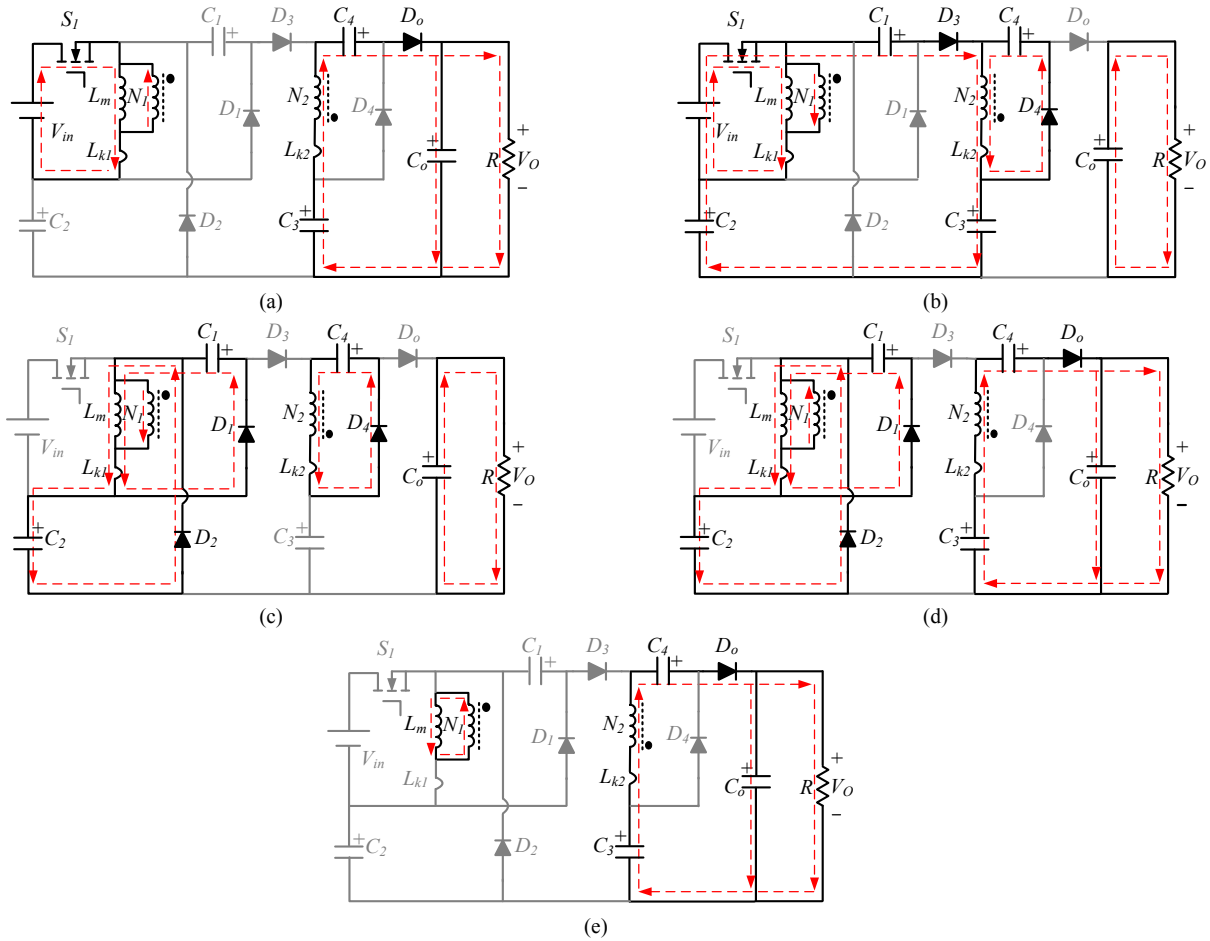


Fig. 4. Current flow paths during one switching period under the CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

is conducting. The diodes D_1 , D_2 , D_3 and D_4 are reverse-biased by $V_{C1}+V_{in}$, $V_{C2}+V_{in}$, $V_O-V_{C4}-V_{C2}-V_{C1}-V_{in}$ and V_O-V_{C3} . It can be seen that the source voltage V_{in} transfers energy to the magnetizing inductor L_m and the primary leakage inductor L_{k1} . Meanwhile, the magnetizing inductor L_m is series connected with C_3 and C_4 to delivering their energy to the charge output capacitor C_o and the load R . The secondary leakage inductor current i_{Lk2} of the coupled inductor is decreased linearly. This stage ends when the current $i_{Lk1} = i_{Lm}$ at $t=t_1$.

Mode II [t_1-t_2]: During this time interval, S_1 remains turned on, and the diodes D_3 and D_4 are turned on. The diodes D_1 and D_2 are still blocked by $V_{C1}+V_{in}$ and $V_{C2}+V_{in}$. The diode D_o is blocked by V_O-V_{C3} . Fig. 4(b) shows the current flow path of this mode. As can be seen, the inductors L_m and L_{k1} are still charged by V_{in} . In the meantime, some of the energy of the magnetizing inductor L_m is delivered to the secondary side via the coupled inductor to charge the capacitor C_4 . Moreover, the source energy V_{in} is serially connected with the capacitor C_1 , the secondary winding N_2 and the capacitor C_2 to charge the capacitor C_3 through the diode D_3 . The load energy is supplied by the output capacitor C_o . This mode ends when the switch S_1 is turned off at $t=t_2$.

Mode III [t_2-t_3]: At $t=t_2$, the switch S_1 is turned off, and the diodes D_1 , D_2 and D_4 are turned on. The diodes D_3 and D_o are reverse-biased by $V_{C3}-V_{C4}-V_{C1}$ and V_O-V_{C3} . The current flow path of this period is shown in Fig. 4(c). Once S_1 is switched off, the energy stored in L_{k1} is rapidly discharged to the capacitor C_1 through the diode D_1 . Simultaneously, the energy stored in L_{k1} is also discharged to the capacitor C_2 through the diode D_2 . Therefore, the capacitor C_1 and the capacitor C_2 are charged in parallel. At the same time, the secondary leakage inductor L_{k2} keeps the same current direction for charging the capacitor C_4 through the diode D_4 . These energy transfers bring about decreases in i_{Lk1} and i_{Lk2} but increases in i_{Lm} , because L_{k1} and L_{k2} are significantly smaller than L_m , and i_{Lk2} rapidly declines. Therefore, the magnetizing inductor L_m receives energy from L_{k1} , the energy stored in the capacitor C_o is discharged to the load R . This mode ends when the current i_{Lk2} drops to zero at $t=t_3$.

Mode IV [t_3-t_4]: During this interval, S_1 is kept turned off. Only the diodes D_1 , D_2 and D_o are conducting. The diodes D_3 and D_4 are blocked by $V_O-V_{C4}-V_{C1}$ and V_O-V_{C3} . Fig. 4(d) illustrates the current flow path of this stage. The energy stored in L_m and L_{k1} continue to release to the capacitors C_1

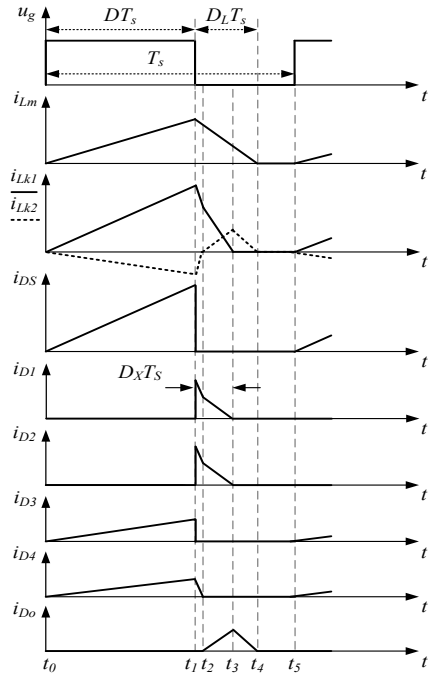


Fig. 5. Key waveforms of the proposed converter during the DCM operation.

and C_2 . The voltage stress of the active switch is limited by the double clamp circuits, and the leakage inductor energy can be effectively recycled. In the meantime, the energy stored in L_m is released to the capacitor C_o and R via the secondary side N_2 of the coupled inductor, and in series with C_3 and C_4 to charge the capacitor C_o and R . Therefore, the currents of i_{Lk1} and i_{Lm} are rapidly decreased but i_{Lk2} is linearly increased. Once the current i_{Lk1} declines to zero, this mode ends at $t = t_4$.

Mode V [t_4-t_5]: At $t=t_4$, S_1 is still turned off. Since $i_{Lk1}=0$ at $t=t_4$, the diodes D_1 and D_2 are naturally turned off, and only the diode D_o is conducting. The current flow path of this period is shown in Fig. 4(e). The magnetizing inductor L_m and the capacitors C_3 and C_4 are still series connected to deliver their energy to the capacitor C_o and R . This mode ends when the switch S_1 is turned on at $t = t_5$, which is the start of the next switching period.

B. DCM Operation

The detailed operating principle of the discontinuous conduction mode (DCM) is presented in this section. There are five operating modes during one switching period. Fig. 5 shows key waveforms for some of the components. The operating modes are presented as follows.

Mode I [t_0-t_1]: At $t=t_0$, S_1 is turned on. The diodes D_3 and D_4 are turned on, and the diodes D_1, D_2 and D_o are turned off. The current flow path is shown in Fig. 6(a). In this mode, i_{Lm} , i_{D2} and i_{D3} increase because the capacitor C_3 is charged from the source energy V_{in} , and the capacitors C_1 and C_2 . In addition, the magnetizing inductor L_m is receiving energy

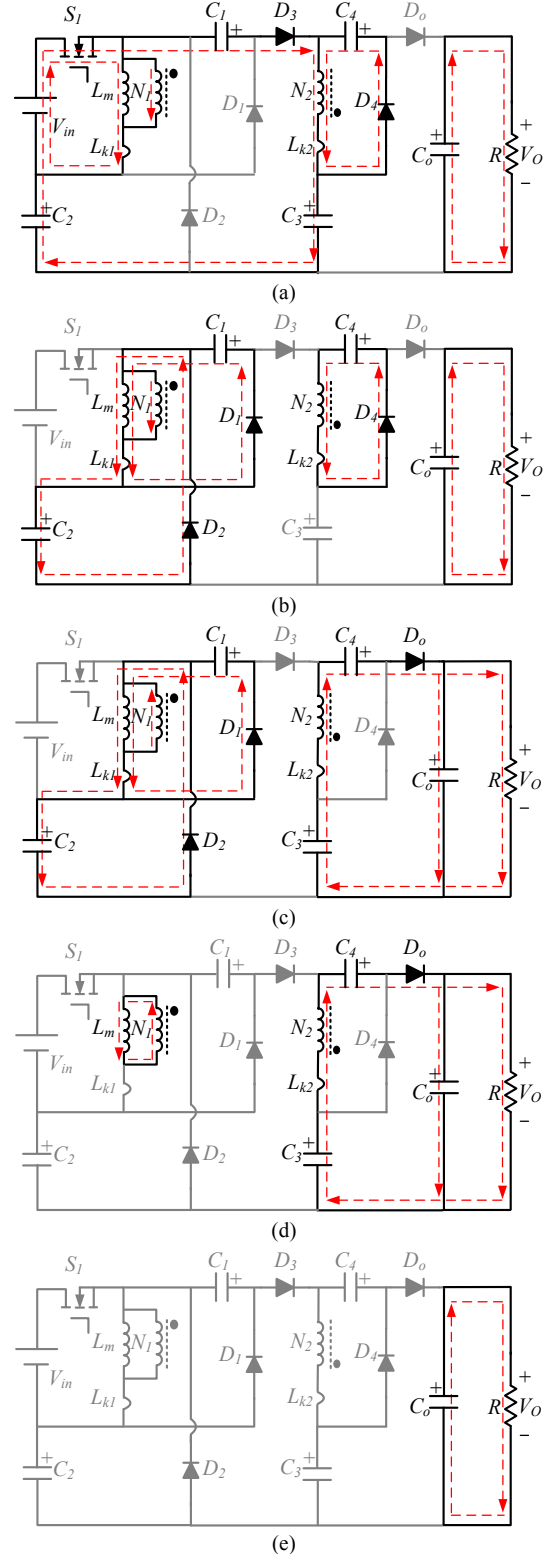


Fig. 6. Current paths during one switching period under the DCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

from V_{in} . Meanwhile, some of the energy stored in L_m is released to the capacitor C_4 through the diode D_4 . The output capacitor C_o provides its energy to the load R . Once the

switch S_1 is switched off, this mode ends at $t = t_1$.

Mode II [t_1-t_2]: At $t = t_1$, S_1 is turned off. The diodes D_1 and D_2 start to turn on, and the diodes D_3 and D_0 are turned off. Fig. 6(b) depicts the current flow path of this period. The energy stored in the coupled inductor is delivered to the capacitors C_1 and C_2 through the diodes D_1 and D_2 . Meanwhile, the capacitor C_4 is still charged by the magnetizing inductor L_m . Thus, the currents of i_{L_m} , i_{D1} and i_{D2} are linearly decreased. The energy stored in the capacitor C_0 is released to the load R . This mode ends when the current i_{D4} reaches zero at $t = t_2$.

Mode III [t_2-t_3]: In this mode, S_1 remains turned off. The diodes D_1 , D_2 and D_0 start to turn on, and diodes D_3 and D_4 are turned off. Fig. 6(c) depicts the current flow path of this period. The energy stored in the magnetizing inductor L_m is delivered to the capacitors C_1 and C_2 through the diodes D_1 and D_2 . At the same time, i_{D0} increases because L_m is in series with C_3 and C_4 to charge the capacitor C_0 and R . This mode ends at $t = t_3$ when $i_{D1} = i_{D2} = 0$.

Mode IV [t_3-t_4]: During this interval, S_1 remains turned off. Only the diode D_0 is conducting. The current flow path is shown in Fig. 6(d). The magnetizing inductor L_m continues to linearly discharge. The energies stored in L_m , and the capacitors C_3 and C_4 are series connected, and release their energy to the capacitor C_0 and R through the diode D_0 . This stage ends when the energy stored in the magnetizing inductor L_m is equals to zero at $t = t_4$.

Mode V [t_4-t_5]: At $t = t_4$, All of the power devices are turned off. Fig. 6(e) illustrates the current flow path of this stage. Because the energy stored in L_m is already depleted, the energy stored in the capacitor C_0 is released to the load R . This mode ends when the switch S_1 is turned on at $t = t_5$, which is the start of the next switching period.

III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

A. CCM Operation

To simplify the steady-state analysis, only modes II and IV are considered for the CCM operation because the times of modes I, III and V are too short to ignore, and all of the leakage inductances of the coupled inductor are neglected.

In mode II, the following equations can be expressed from Fig. 4(b).

$$V_{L_m} = V_{in} \quad (1)$$

$$V_{N2} = nV_{in} = V_{C4} \quad (2)$$

In addition, the voltage of the capacitor C_3 can be obtained as:

$$V_{C3} = V_{in} + V_{C1} + V_{C2} + V_{C4} \quad (3)$$

During Mode IV, the following equations can be written:

$$V_{L_m} = -V_{C1} = -V_{C2} \quad (4)$$

$$V_o = V_{C3} + V_{C4} - V_{N2} \quad (5)$$

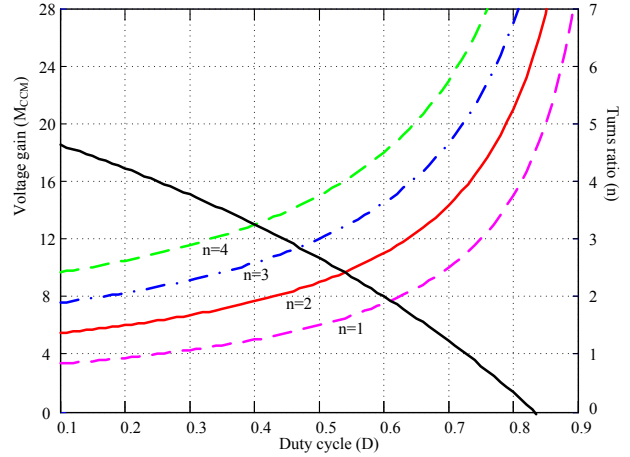


Fig. 7. Voltage gain of the proposed converter and the turns ratio versus duty cycle when the voltage conversion is 11.

Applying the inductor volt-second balance principle to the magnetizing inductor L_m and binding the above equations, the voltage across the capacitors C_1 , C_2 , C_3 and the secondary-side voltage V_{N2} of the coupled inductor are derived as:

$$V_{C1} = V_{C2} = \frac{D}{1-D} V_{in} \quad (6)$$

$$V_{C3} = (1+n + \frac{2D}{1-D}) V_{in} \quad (7)$$

$$V_{N2} = -\frac{nD}{1-D} V_{in} \quad (8)$$

Substituting (2), (7) and (8) into (5), the dc voltage gain M_{CCM} can be obtained as:

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{V_{C3} + V_{C4} - V_{N2}}{V_{in}} = \frac{1+n+D}{1-D} + n \quad (9)$$

Fig. 7 shows the voltage gain extension effect with different turns ratios at various duty cycles. In addition, the curve of an approximately straight line accounts for the relationship between the turns ratio and the duty cycle under the voltage gain $M_{CCM}=11$.

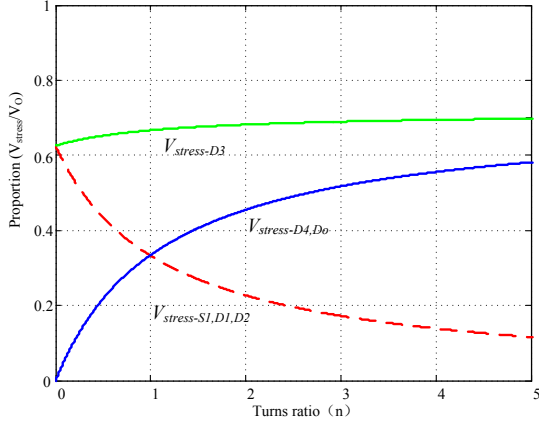
B. Voltage Stress Analysis

During the CCM operation, the voltage and current stresses on the power devices are discussed as follows, and the leakage inductances L_{k1} and L_{k2} of the coupled inductor are neglected. The voltage stresses on the switch S_1 and the diodes $D_1 \sim D_0$ are given as:

$$V_{DS} = \frac{V_{in}}{1-D} = \frac{V_o}{1+2n+(1-n)D} \quad (10)$$

$$V_{D1} = V_{D2} = \frac{V_{in}}{1-D} = \frac{V_o}{1+2n+(1-n)D} \quad (11)$$

$$V_{D3} = \frac{n+1}{1-D} V_{in} = \frac{(1+n)V_o}{1+2n+(1-n)D} \quad (12)$$


 Fig. 8. Voltage stress curve of power devices when $D=0.6$.

$$V_{D4} = V_{D_o} = \frac{nV_{in}}{1-D} = \frac{nV_o}{1+2n+(1-n)D} \quad (13)$$

According to the operating principles, the current ripples on the magnetizing inductor can be derived as:

$$\Delta I_{L_m} = \frac{V_{in}DT_S}{L_m} \quad (14)$$

The average currents of I_{C1} , I_{C2} , I_{C3} and I_{C4} are zero in the steady state. Thus, the average currents that flow through the diodes $D_1 \sim D_o$ are each equal to the average current of I_o . The current stresses on the switch S_1 and the diodes $D_1 \sim D_o$ are expressed as follows:

$$i_{D1(peak)} = i_{D2(peak)} = \frac{1}{2}(I_{L_m} + \frac{\Delta I_{L_m}}{2} + ni_{D4(peak)}) \quad (15)$$

$$i_{D3(peak)} = i_{D4(peak)} = \frac{2I_o}{D} \quad (16)$$

$$i_{D_o(peak)} = \frac{2I_o}{1-D} \quad (17)$$

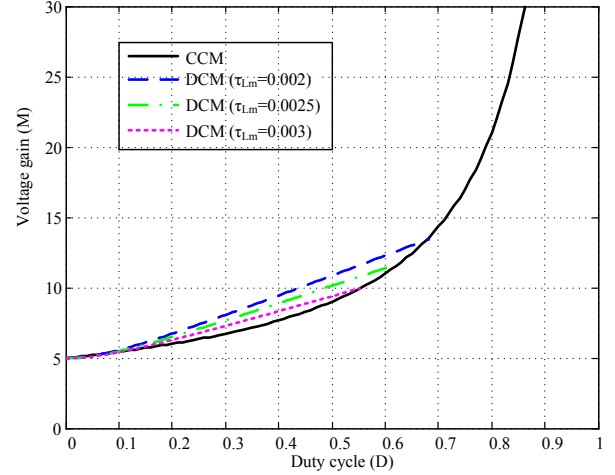
$$i_{D_S(peak)} = i_{L_{mp}} + ni_{D4(peak)} + i_{D3(peak)} = I_{L_m} + \frac{\Delta I_{L_m}}{2} + \frac{2I_o(n+1)}{D} \quad (18)$$

Fig. 8 shows the relationship between the normalized power device voltage stresses and the turns ratio of the coupled inductor when $D=0.6$. It can be seen that the voltage stresses of the power device are always lower than the output voltage. Therefore, a switch with a low resistance $R_{DS(ON)}$ and a high performance can be employed to increase efficiency.

C. DCM Operation

To simplify the analysis, all of the leakage inductances of the coupled inductor are neglected, and only modes I, III and IV are considered for the DCM operation. When the switch S_1 is turned on, the following equations can be written from Fig. 6(a).

$$V_{L_m} = V_{in} \quad (19)$$


 Fig. 9. Voltage gain versus the duty cycle during the DCM operation under various τL_m and during the CCM operation under $n=2$.

$$V_{N2} = nV_{in} = V_{C4} \quad (20)$$

$$V_{C3} = V_{in} + V_{C1} + V_{C2} + V_{C4} \quad (21)$$

When the switch S_1 is turned off, the following equations can be obtained from Fig. 6(c) and Fig. 6(d).

$$V_{L_m} = -V_{C1} = -V_{C2} \quad (22)$$

$$V_o = V_{C3} + V_{C4} - V_{N2} \quad (23)$$

$D_L T_S$ is defined as the time during which the current i_{L_m} travels from the peak point to zero, when the switch S_1 is turned off. By applying the volt-second balance principle to the coupled inductor and binding equations (19)-(23), the voltages of the capacitors C_1 , C_2 , C_3 and the secondary-side voltage V_{N2} of the coupled inductor can be obtained as:

$$V_{C1} = V_{C2} = \frac{D}{D_L} V_{in} \quad (24)$$

$$V_{C3} = \frac{(1+n)D_L + 2D}{D_L} V_{in} \quad (25)$$

$$V_{N2} = -\frac{nD}{D_L} V_{in} \quad (26)$$

Substituting (20), (25) and (26) into (23), D_L can be obtained as:

$$D_L = \frac{(2+n)DV_{in}}{V_o - (1+2n)V_{in}} \quad (27)$$

According to the steady operating principle, the average currents of I_{D1} and I_{D_o} are equal to the average current of I_o , D_X which is defined as the duration of the current i_{D1} decline from the peak value to zero. The peak current of the magnetizing inductor $i_{L_{mp}}$ is given as:

$$i_{L_{mp}} = \frac{V_{in}DT_S}{L_m} \quad (28)$$

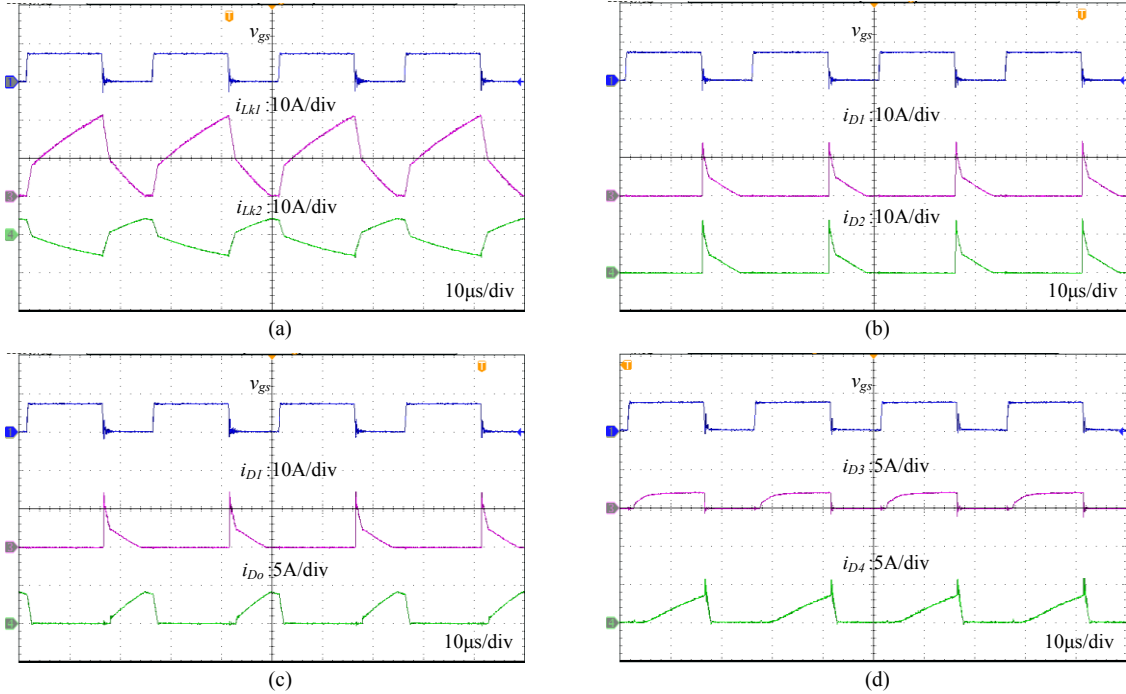


Fig. 10. Experimental current waveforms: (a) v_{gs} , i_{Lk1} , i_{Lk2} ; (b) v_{gs} , i_{D1} , i_{D2} ; (c) v_{gs} , i_{D1} , i_{Do} ; (d) v_{gs} , i_{D3} , i_{D4} .

The average currents of the diodes D_1 and D_o are expressed as follows:

$$I_{D1} = \frac{(1/4)i_{Lmp}D_X T_S}{T_S} \quad (29)$$

$$I_{Do} = \frac{i_{Lmp}(D_L - D_X)T_S}{2nT_S} \quad (30)$$

From (27) and (28), the following equations are derived as:

$$D_X = \frac{2D_L}{2+n} \quad (31)$$

$$I_O = \frac{D_L i_{Lmp}}{2(2+n)} \quad (32)$$

The normalized magnetizing inductor time constant τ_{Lm} is defined as:

$$\tau_{Lm} = \frac{L_m}{RT_S} = \frac{L_m f_s}{R} \quad (33)$$

Since $I_O = V_O/R$, by substituting (27), (28) and (33) into (32), the voltage gain of the proposed converter in the DCM can be obtained as:

$$M_{DCM} = \frac{V_O}{V_{in}} = \frac{(1+2n) + \sqrt{(1+2n)^2 + (2D^2 / \tau_{Lm})}}{2} \quad (34)$$

Equation (34) can be used to illustrate the DCM voltage gain lines under different τ_{Lm} . Fig. 9 shows the curve of the voltage gain against the duty cycle under various τ_{Lm} .

D. BCM Condition

When the proposed converter is operating in the BCM, the

voltage gains of M_{CCM} are equal to those of M_{DCM} .

The boundary normalized magnetizing inductor time constant τ_{LmB} can be derived from (12) and (34).

$$\tau_{LmB} = \frac{D(1-D)^2}{2(1+2n+D-nD)(2+n)} \quad (35)$$

IV. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the theoretical analysis, a 200W experimental prototype circuit of the proposed converter has been built and tested in the laboratory. The basic parameters of the converter are listed as follows:

- 1) input voltage V_{in} : 18-24V;
- 2) output voltage V_O : 200V;
- 3) maximum output power P_O : 200W;
- 4) switching frequency f_s : 40kHz;
- 5) coupled inductor: EE-55, core pc40, $N_2/N_1=14:7$, $L_m=66\mu\text{H}$, and $L_k=2.4\mu\text{H}$;
- 6) power switch S_1 : IRFB4410PbF;
- 7) diodes D_1/D_2 : MUR810, D_3 : MUR840, D_4/D_o : MUR820;
- 8) capacitors $C_1/C_2/C_4$: 100 $\mu\text{F}/100\text{V}$, C_3 : 47 $\mu\text{F}/200\text{V}$,
- 9) C_o : 220 $\mu\text{F}/400\text{V}$.

Fig. 10(a) shows the gate signal of the switch S_1 and the current waveforms of the primary-side current i_{Lk1} and the secondary-side current i_{Lk2} of the coupled inductor. It can be seen that the proposed converter is operated in the CCM operation. It can also be seen that it has five modes during the CCM operation. Fig. 10(b) gives the gate signal of S_1 and the

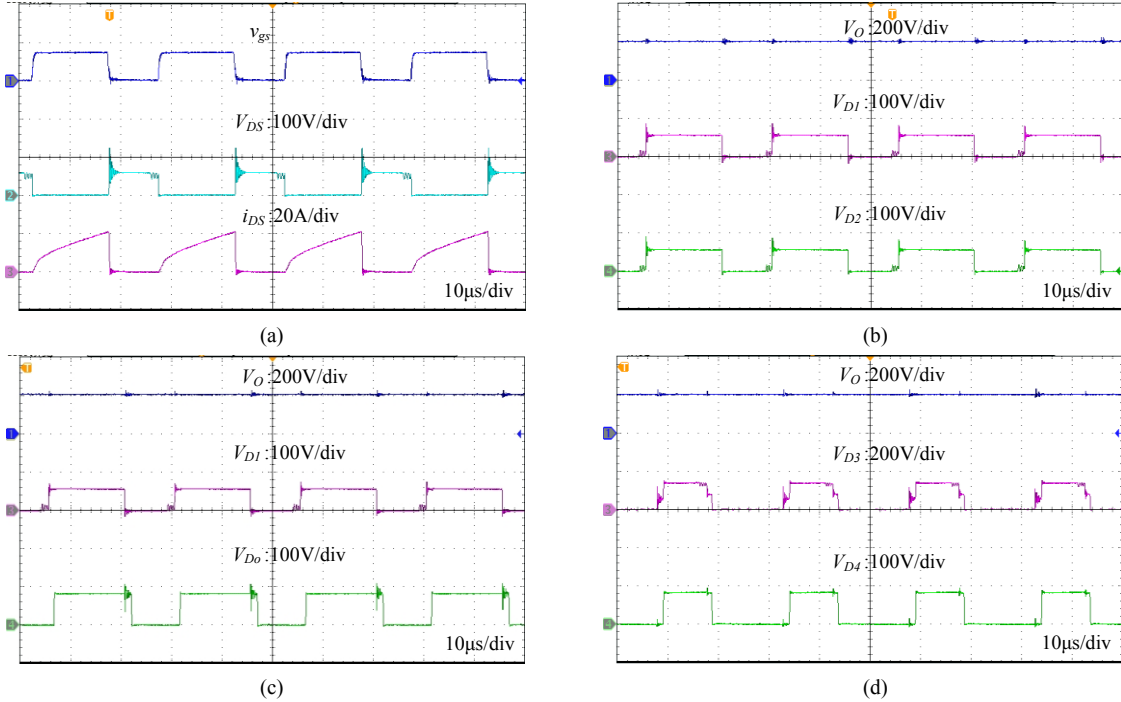


Fig. 11. Experimental voltage stress waveforms: (a) v_{gs} , V_{DS} , i_{DS} ; (b) V_O , V_{D1} , V_{D2} ; (c) V_O , V_{D1} , V_{D0} ; (d) V_O , V_{D3} , V_{D4} .

current waveforms through the diodes D_1 and D_2 . It can be seen that the currents i_{D1} and i_{D2} are nearly synchronous, which confirms that the clamp diodes D_1 and D_2 are conductive and charged in parallel by the primary leakage inductor L_{k1} when the switch S_1 is turned off. Fig. 10(c) illustrates the gate signal and waveforms of i_{D1} and i_{D0} . The diode D_0 starts to turn on when the current i_{Lk2} declines to zero. In addition, the secondary side of the coupled inductor is series connected with the capacitors C_3 and C_4 to transfer their energy to the load. Fig. 10(d) shows the gate signal and waveforms of i_{D3} and i_{D4} . It can be seen that the secondary leakage inductor L_{k2} is transferring its energy to the capacitor C_4 through the diode D_4 when the switch S_1 is turned off.

Fig. 11(a) represents the gate signal of S_1 and waveforms including V_{DS} and i_{DS} . Since the switch S_1 is turned on, the current of i_{DS} is very small, which makes the switch approximately zero current conduction. In addition, the voltage stress of the switch S_1 is only a quarter of the output voltage during the steady-state period, which is about 50V. Therefore, a low voltage rating and low on-state resistance level active switch can be selected for high efficiency. In Fig. 11(b), voltage stress waveforms of the diodes D_1 , D_2 and the output voltage are presented. The measured voltage through the diodes D_1 and D_2 are found to be about 50V, which is only a quarter of the output voltage. Waveforms of V_{D1} and V_{D0} are shown in Fig. 11(c). The voltage value of the diode D_0 is approximately 90V, which lowers to half the output voltage in the steady-state period. Fig. 11(d) illustrates the output voltage and voltage stress of the diodes D_3 and D_4 . The voltage stress of the diode D_4 is the same as that of the

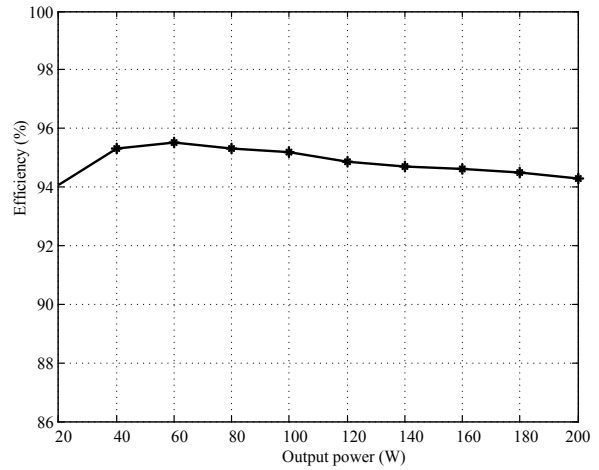


Fig. 12. Measured efficiency of the proposed converter at various output powers.

diode D_0 , and the value of the diode D_3 is about 140V, which shows good agreement with the theoretical analysis. It can be seen that the voltage stresses of these diodes are far lower than the output voltage. Therefore, low-voltage-rated diodes with high performance can be adopted for the presented converter.

Fig. 12 summarizes the efficiency of the proposed converter under various output powers. Under the premise of keeping the output voltage constant, the corresponding output power is achieved by changing the load value. The input voltage and input current are recorded at the same time. Through the efficiency formula operation, the efficiency points of different output powers are obtained. Finally, the

efficiency curve is drawn through the efficiency point. The maximum efficiency is up to 95.7%, and the efficiency is about 94.3% at a full-load.

V. CONCLUSION

A novel DC-DC converter structure is proposed for high voltage gain applications. The clamp capacitor and switch capacitor recycle leakage inductance energy to improve the conversion efficiency and to effectively reduce the peak voltage of the main switch. Moreover, the voltage stresses of the power devices are greatly reduced, and the problem of reverse recovery on the diodes is greatly alleviated. Experimental results have been obtained and they are in agreement with the theoretical analysis. In addition, the topology characteristics of the proposed DC-DC converter have been verified.

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