J Electr Eng Technol.2018; 13(3): 1251-1264
http://doi.org/10.5370/JEET.2018.13.3.1251

ISSN(Print) 1975-0102
ISSN(Online) 2093-7423

Implementation of Zero-Ripple Line Current Induction Cooker using Class-D Current-Source Resonant Inverter with Parallel-Load Network Parameters under Large-Signal Excitation

Chainarin Ekkaravarodome†, Phatiphat Thounthong* and Kamon Jirasereeamornkul**

Abstract – The systematic and effective design method of a Class-D current-source resonant inverter for use in an induction cooker with zero-ripple line current is presented. The design procedure is based on the principle of the Class-D current-source resonant inverter with a simplified load network model that is a parallel equivalent circuit. An induction load characterization is obtained from a large-signal excitation test-bench based on parallel load network, which is the key to an accurate design for the induction cooker system. Accordingly, the proposed scheme provides a systematic, precise, and feasible solution than the existing design method based on series-parallel load network under low-signal excitation. Moreover, a zero-ripple condition of utility-line input current is naturally preserved without any extra circuit or control. Meanwhile, a differential-mode input electromagnetic interference (EMI) filter can be eliminated, high power quality in utility-line can be obtained, and a standard-recovery diode of bridge-rectifier can be employed. The step-by-step design procedure explained with design example. The devices stress and power loss analysis of induction cooker with a parallel load network under large-signal excitation are described. A 2,500-W laboratory prototype was developed for 220-V_{rms}/50-Hz utility-line to verify the theoretical analysis. An efficiency of the prototype is 96% at full load.

Keywords: Induction heating, Induction cooker, Class-D current-source resonant inverter, Zero-ripple line current, Lumped-parameter.

1. Introduction

Induction heating (IH) technology have favorable features of the contactless energy transfer due to the fact that it provides faster heating time, cleanliness, safety, and higher efficiency [1,2] when comparison with the traditional heating methods, such as resistance heating, halogen heating, and flame heating. As a consequence, the IH technology has become increasingly common in our daily lives. These are well suited to domestic appliances such as induction water heater, induction tea maker, induction pressure rice cooker, and induction cooker, which the induction cookers have a main domestic application of the IH technology. Meanwhile, a resonant power inverter is commonly utilized to generate a medium-frequency alternating current (AC), normally operated between 20-100 kHz to supply the pan inductor-vessel. This vessel is directly heated by causes magnetic hysteresis and an eddy current circulating through the bottom of the vessel. The resonant power inverter architectures for the induction cooker implementations can be divided into three categories as a function of a number of an active switch: first; the one-switch Class-E resonant inverter [3-5] has been proposed for low-power applications (<2,000W), second; the two-switch Class-D voltage-source resonant inverter with series load network [6-15] and Class-D current-source resonant inverter with series-parallel load network [16-19] have been proposed for medium-power applications (<5,000 W), and third; the four-switch Class-D voltage-source resonant inverter with series load network [20-27] and Class-D current-source resonant inverter with series-parallel load network [28-30] have been proposed for high-power applications (>5,000 W).

The major drawbacks of the medium-power induction cooker based on the Class-D voltage-source resonant inverter with series load network are requires a large differential mode EMI filter to meet electromagnetic compatibility (EMC) regulation requirements for attenuate the large high frequency ripple utility-line input current and it needed to design of a driver circuit for high-side switch, which would reduce reliability of the system. To overcome these problems, the Class-D current-source resonant inverter with series-parallel load network for the

† Corresponding Author: Advanced Power Electronics and Experiment Laboratory (APEx Lab), Dept. of Instrumentation and Electronics Engineering, King Mongkut's University of Technology North Bangkok, Thailand. (chainarin.e@eng.kmutnb.ac.th)
* Renewable Energy Research Centre (RERC), Dept. of Teacher Training in Electrical Engineering, King Mongkut's University of Technology North Bangkok, Thailand. (phatiphat.t@fte.kmutnb.ac.th)
** Dept. of Electronic and Telecommunication Engineering, King Mongkut's University of Technology Thonburi, Thailand. (kamon.jir@mail.kmutt.ac.th)
Received: March 22, 2017; Accepted: January 26, 2018

induction cooker applications has been presented. However, the analysis and design are difficult and inaccurate because the induction load parameters have been provided from low-signal excitation with complexity of induction-load parameters, which is not suitable for this application.

To solve aforementioned problem, a step-by-step design procedure explained with design example for the Class-D current-source resonant inverter with a simplified load network model that is a parallel resonant equivalent circuit under large-signal excitation for the zero-ripple line current domestic induction cooker application. An alternative lumped-parameter of coil and vessel using a parallel load network is presented for the induction-load equivalent circuit instead of the common series-parallel *R-L* and *C* load network. Furthermore, in order to get the circuit parameters, the induction-load characterization must be achieved under large-signal excitation using test-bench. As a result, the proposed scheme provide a more accurate, systematic, and feasible solution. The differential mode EMI filter can be eliminated because the zero-ripple condition of the utility-line input current can be achieved rather easily. As a result, a high utility-line input power-factor (PF) and a low total harmonic distortion of the utility-line input current (THD_i) can be obtained. Moreover, the standard-recovery diodes can be employed as bridge-rectifier.

The description of the proposed resonant power converter and its operating mode are presented in Section 2. Section 3 illustrates the design procedure. In Section 4 show the design example, simulation, and experimental results to verify the theoretical analysis. Finally, the conclusions are given in Section 5.

2. Proposed Topology

2.1 Schematic diagram

Fig. 1 shows a schematic diagram with key waveforms of the Class-D current-source resonant inverter using a parallel load network under large-signal excitation for the zero-ripple line current domestic induction cooker. First, a bridge-rectifier diode is used to convert the low-frequency utility-line input voltage into a full-wave rectified sinusoidal voltage. Finally, a resonant power converter block, which is the main part of the system, supplies the medium-frequency AC to the pan inductor-vessel with the 2,500-W output power. Typically, the EMI filter should be bulky and costly in order to decrease the high-frequency current of the inverter stage from entering into the utility-line to satisfy the requirement of the low-ripple current condition. The differential-mode EMI filter is not needed for the proposed topology because the zero-ripple condition of the utility-line input current can be achieved. The analysis of the Class-D current-source resonant inverter using a parallel load network under large-signal excitation for the zero-ripple line current domestic induction cooker is carried out under the following assumptions to simplify the analysis:

1. The active switch and the series power diode form an ideal switch with an on-state voltage equal to zero, an off-state is modeled by an infinite resistance, and a switching time of zero.
2. The choke inductance is large enough that its current is approximately constant over one switching cycle.
3. The components of the parallel load network are passive, linear, and do not have parasitic components.
4. The switching frequency is less than the resonant frequency.
5. The vessel is considered as a load resistor with fixed resistance for a specific operating frequency. If this frequency changed, the load resistance is also changed.

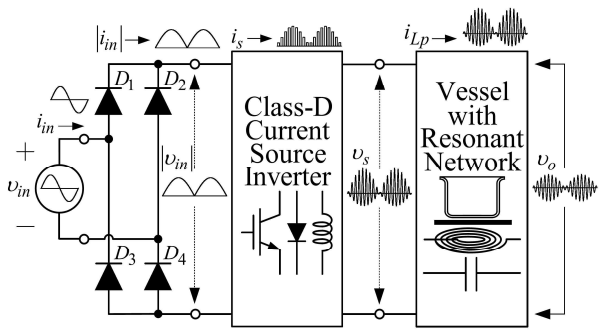


Fig. 1. Schematic diagram of the Class-D current-source resonant inverter for the zero-ripple line current domestic induction cooker

2.2 Circuit description

Fig. 2(a) shows a circuit of the proposed topology. It consists of the standard-recovery bridge-rectifier diodes D_1-D_2-D_3-D_4. The cost of the proposed topology can be reduced because standard-recovery diodes can be used for the bridge-rectifier and the EMI filter is not needed because the zero-ripple condition of the utility-line input current can be achieved. The proposed Class-D current-source resonant inverter consists of a choke inductor L_i, a parallel resonant circuit R_p-L_p-C_p, and two unidirectional switches S_1-S_2. The unidirectional switch comprises an insulated- gate bipolar transistor (IGBT) in series with a diode D_{Q1}-Q_1-D_{Q2}-Q_2. Therefore, the switch can operate only a positive current and can block either positive or negative voltage. The IGBTs are driven by rectangular gate-to-emitter voltages υ_{GE1} and υ_{GE2} to act periodically as a switch, with a switching frequency $f_s = \omega_s / 2\pi$, where ω_s is a switching angular frequency in radians per second. To provide the path for the input current source i_i either one or both switches should be ON. Thus, the on-duty ratio D is slightly more than 50%. A lumped-parameter transformer model of the coil and the vessel [31]-[33] of Fig. 2(a) is shown in Fig. 2(b), where R_w, L_l,

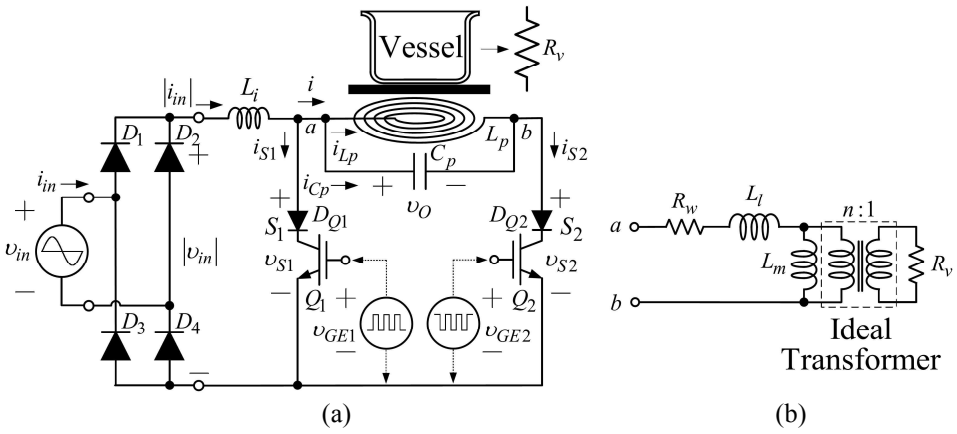


Fig. 2. Circuit topology of the proposed induction cooker: (a) and lumped-parameter transformer model for coil and vessel set (b)

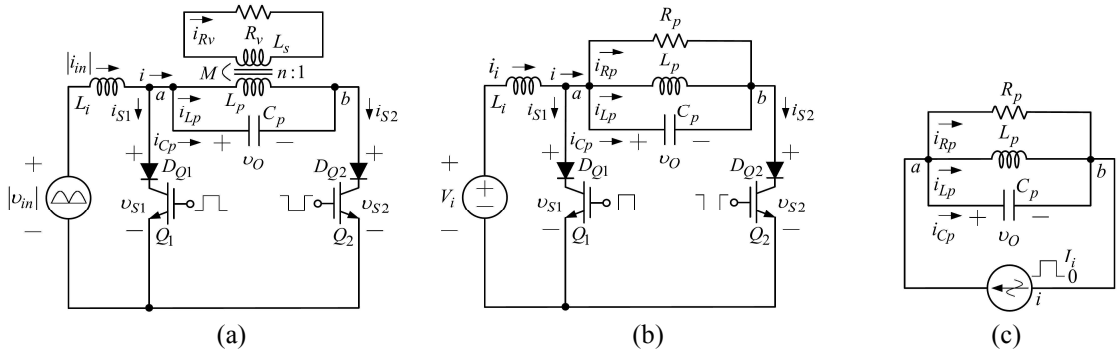


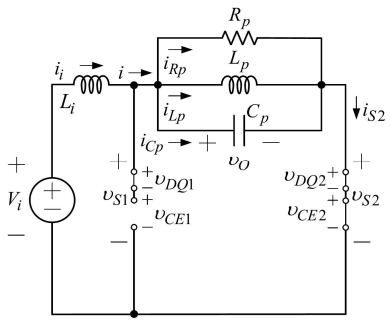
Fig. 3. Equivalent circuit of the proposed domestic induction cooker: (a) Equivalent circuit with simplest form of the transformer; (b) Vessel is replaced by the equivalent resistor R_p with *RLC* parallel resonant circuit; (c) Simplified equivalent circuit

and L_m are presented the winding resistance, the leakage inductance, and the magnetizing inductance of the ideal transformer, respectively. n is the number of turns of the primary coil and R_v is the equivalent vessel resistance.

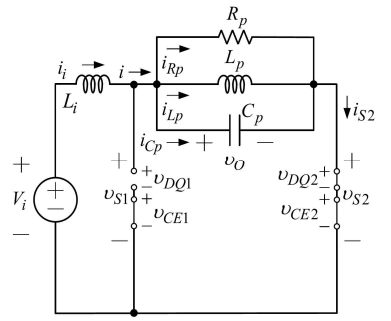
2.3 Circuit operation

Fig. 3 shows the operation of the proposed is explained by an equivalent circuit. The diodes D_1 and D_4 of the bridge-rectifier operate during the positive half-cycle of the utility-line input voltage. This is represented as $\upsilon_{in} = V_{in} \sin \omega_L t$, where ω_L is a line angular frequency in radians per second. The diodes D_2 and D_3 operate during the negative half-cycle of the utility-line input voltage. The model of the rectifier output is a full-wave rectified sinusoidal voltage source $|\upsilon_{in}| = V_{in} |\sin \omega_L t|$. Alternatively, the transformer model with magnetic coupling M can also be used to model the planar coil and the vessel, as shown in Fig. 3(a). To simplify the analysis, the DC input voltage $V_i = V_{in} / \sqrt{2}$ is equal to the root-mean-square (rms) value of the input voltage, replaces the full-wave rectified sinusoidal voltage source $|\upsilon_{in}|$. The magnetic coupling M is *assumed to equal* $\sqrt{L_p L_s}$. The coupling coefficient k is unity. The equivalent vessel resistance R_v is reflected to the primary side as an equivalent resistor R_p and is connected in parallel with a primary inductance L_p and capacitor C_p as shown in Fig. 3(b). Consequently, the simplest type of load network is the parallel resonant circuit. The simplified equivalent circuit of the proposed topology is shown in Fig. 3(c), the circuit composed of the input voltage V_i, the choke inductor L_i, and the switches S_1 and S_2 can be modeled by a square-wave current source i which is equal to active switch current of S_2, i_{S2}.

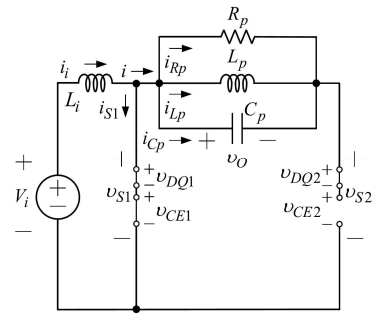
The input current source i of the parallel resonant circuit is a square wave of magnitude I_i. If the loaded quality factor Q_L of the parallel resonant circuit is high enough, the voltage across this circuit υ_O is nearly a sine wave. For $f_s < f_r$ the parallel resonant circuit represents an inductive load and the fundamental component i_{i1} of the input current source i lags behind the voltage across the parallel resonant circuit υ_O by the phase angle ψ, where $\psi > 0$. Thus, the switch voltage is negative after turn-on and positive before turn-off. The conduction sequence of the semiconductor devices is D_{Q1}-Q_1-D_{Q2}-Q_2. The working modes of the equivalent circuit of the proposed domestic induction cooker in a one-switching cycle are depicted in Fig. 4(a)-



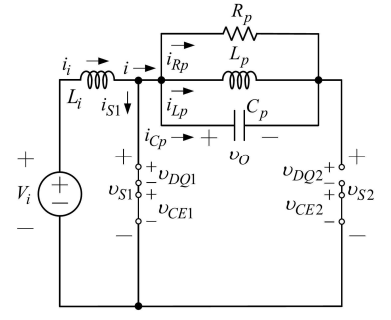
(a) Mode 1



(b) Mode 2



(c) Mode 3



(d) Mode 4

Fig. 4. Working modes of the equivalent circuit in one-switching cycle: (a) D_{Q1} is ON, Q_1 is OFF, and S_2 is ON; (b) D_{Q1} is OFF, Q_1 is ON, and S_2 is ON; (c) S_1 is ON, D_{Q2} is ON, and Q_2 is OFF; (d) S_1 is ON, D_{Q2} is OFF, and Q_2 is ON

(d). The schematic current and voltage waveforms in a one-switching cycle near the peak of the utility-line input voltage of the proposed circuit are shown in Fig. 5. A detailed analysis of the complete operation including four modes is described as follows:

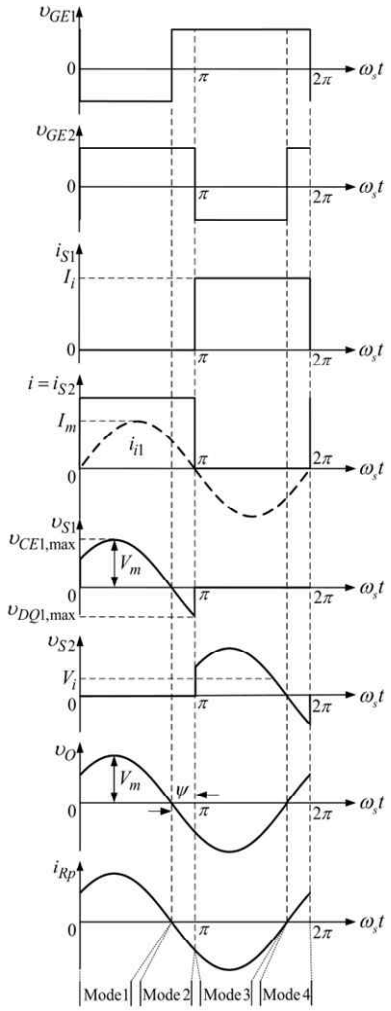


Fig. 5. Schematic voltage and current waveforms during one-switching cycle

Mode 1: The switch S_2 is turned on, when IGBT Q_2 is turned on by the drive voltage υ_{GE2}, the switch current of S_2, i_{S2} is the magnitude of choke inductor current I_i and the switch voltage of S_2, υ_{S2} is zero. At the same time, the drive voltage υ_{GE1} is reduced from high to low level, the IGBT Q_1 is turned off and the series diode D_{Q1} is turned on. During the time interval, the switch voltage of S_1, υ_{S1} is positive is equal to the voltage across the parallel resonant circuit υ_O.

Mode 2: When the switch voltage of S_1, υ_{S1} is decreased to zero, the series diode D_{Q1} is turned off, the drive voltage υ_{GE1} is increased from low to high level, the IGBT Q_1 is turned on. Then the reverse voltage of the series diode D_{Q1} is equal to the voltage across the parallel resonant circuit υ_O and supports the switch voltage when the switch voltage is negative.

Mode 3: The switch S_1 is turned on, when IGBT Q_1 is turned on by the drive voltage υ_{GE1}, the switch current of S_1, i_{S1} is the magnitude of choke inductor current I_i and the switch voltage of S_1, υ_{S1} is zero. At the same time, the drive voltage υ_{GE2} is reduced from high to low level, the IGBT Q_2 is turned off and the series diode D_{Q2} is turned on.

During the time interval, the switch voltage of S_2, υ_{S2} is positive is equal to the voltage across the parallel resonant circuit υ_O .

Mode 4: When the switch voltage of S_2, υ_{S2} is decreased to zero, the series diode D_{Q2} is turned off, the drive voltage υ_{GE2} is increased from low to high level, the IGBT Q_2 is turned on. Then the reverse voltage of the series diode D_{Q2} is equal to the voltage across the parallel resonant circuit υ_O and supports the switch voltage when the switch voltage is negative.

The schematic current and voltage waveforms in one-line cycle of the proposed topology are presented in Fig. 6. A sinusoidal utility-line input voltage waveform is displayed in Fig. 6(a). The full-wave rectified utility-line input voltage $|\upsilon_{in}|$ and the full-wave rectified utility-line input current $|i_{in}|$ waveforms are depicted in Fig. 6(b) and (c), respectively. Fig. 6(d) shows the output voltage, which is across the parallel resonant circuit υ_O . The switch voltage and switch current waveforms of S_1 over a one-switching cycle are shown in Fig. 6(e) and (f), respectively.

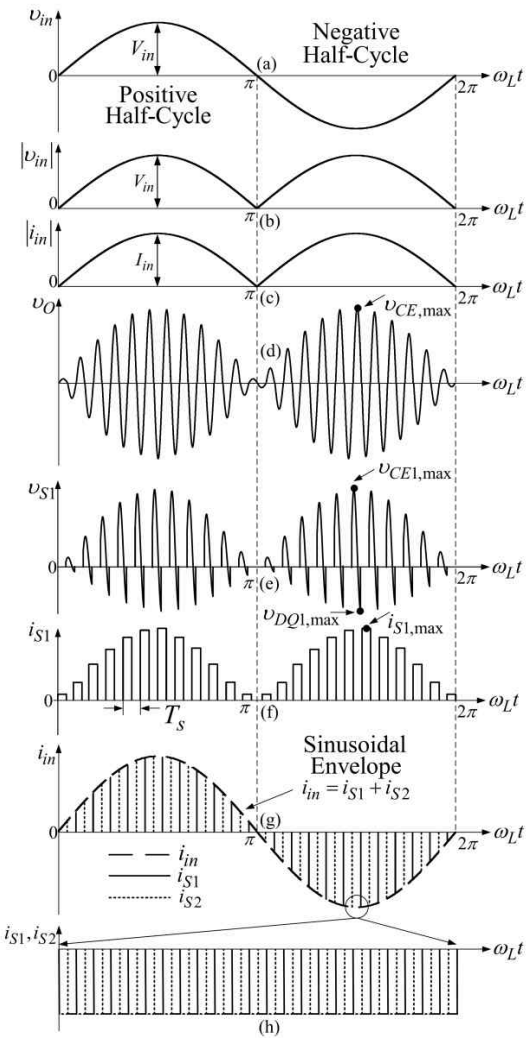


Fig. 6. Schematic waveforms in one-line cycle

The utility-line input current waveform i_{in} is filtered average switch current waveforms of S_1 and S_2 or sum of i_{S1} and i_{S2}, which is equal to sinusoidal envelope of the switch current waveforms of S_1 and S_2 as shown in Fig. 6(g). Fig. 6(h) depicts the switch current waveforms of S_1 and S_2 as zoomed-in views of Fig. 6(g). Thus, the zero-ripple line current can be achieved. Consequently, the differential mode EMI filter can be eliminated and high power quality in utility-line can be obtained.

2.4 Induction load parameter

Fig. 7 illustrates the experimental circuit was used to determine the induction load parameter under low-signal excitation with programmable automatic LCR meter (FLUKE model PM6306). However, the key to an accurate design of the induction cooker system is the induction load parameter, which is composes of the parallel inductance L_p and the parallel load resistance R_p. The experimental circuit was employed to obtain the induction load parameter under large-signal excitation as illustrated in Fig. 8. The inductor coil L_p consists of 25 turns of copper wire, which is litz-wire that made from 18 stands of 27 AWG magnet wires. The ferrite bar was made by using seven I cores of the 3C90 ferrite core. The dimension of I core is $72 \times 15 \times 5$ mm. The diameter of the inductor coil L_p is 180 mm.

The bottom diameter of the vessel is 170 mm, and the thickness of the glass-ceramic spacer is 4 mm. The current-source Class-D inverter with a parallel resonant circuit and

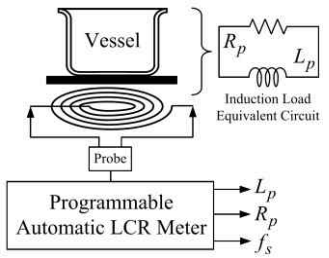


Fig. 7. Induction load parameter under low-signal excitation condition with LCR meter

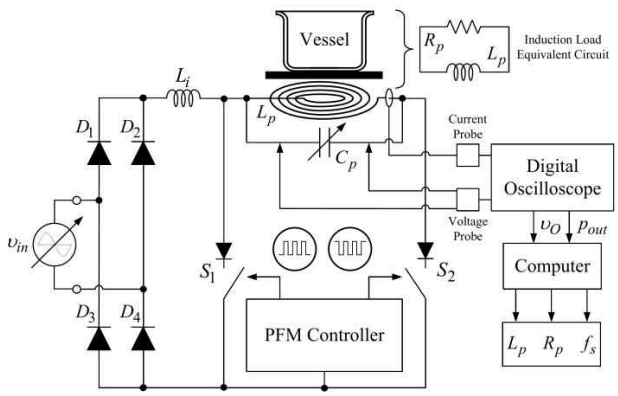


Fig. 8. Induction load parameter under large-signal excitation condition with test-bench

operated at $f_s = f_r$ has been chosen. This topology has been proposed for the other applications [34] and [35]. The output power control is obtained by adjusting utility-line input voltage and resonant capacitor, while resonant condition was fixed for each switching frequency by using pulse-frequency modulation techniques (PFM). The calculation of induction load parameter was carried out in a computer by using experimental data from a digital oscilloscope.

Fig. 9 depicts the equivalent inductances L_p of the induction load network as a function of frequency for various situations. It can be observed that the equivalent inductance L_p decreases when the vessel is added and frequency increases due to the opposing magnetic field of the eddy current in the vessel increases [36]. The equivalent resistance R_p of the induction load network as a function of frequency for various situations is shown in Fig. 10.

The resistance R_p increases when the frequency increases because the skin effect in the vessel. It can be seen that the induction load parameter under large-signal excitation condition is very different from LCR meter ones.

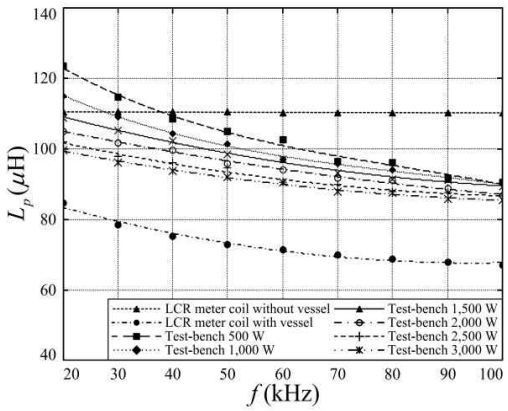


Fig. 9. Curves of the equivalent inductance L_p of the induction load network with load changing

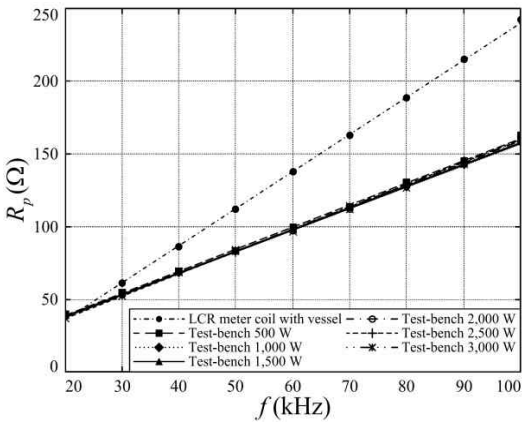


Fig. 10. Curves of the equivalent resistance R_p of the induction load network with load changing

3. Design of Proposed Topology

3.1 Design procedure

In this section, the step-by-step design method for the proposed topology will be briefly explained. The design flowchart of the proposed topology is depicted in Fig. 11 and the design procedures are given as follows:

1. By selecting the desired resonant frequency f_r, the parallel inductance L_p from Fig. 9 and the parallel load resistance R_p from Fig. 10 will be obtained and one can calculate a loaded quality factor Q_L. In addition, a near-sinusoidal utility-line input current was assumed, and expected inverter efficiency η_I, the expected resonant circuit efficiency $\eta_r = R_p/R$ and angular frequency ratio ω_s/ω_r were approximately, where R is the load resistance without parasitic resistance of the resonant circuit and ω_r is resonant angular frequency in radians per second.
2. Specified the utility-line rms voltage $\upsilon_{in,\mathrm{rms}}$ and determine the output power P_{out}. If this determined P_{out} is higher that the desired one, the higher switching frequency must be selected and recalculate the parameters from procedure 1 again. In the other way, if the calculated P_{out} is lower than the desired value, the switching frequency must be decreased.
3. Determine the parallel capacitance C_p from the result of procedure 1.

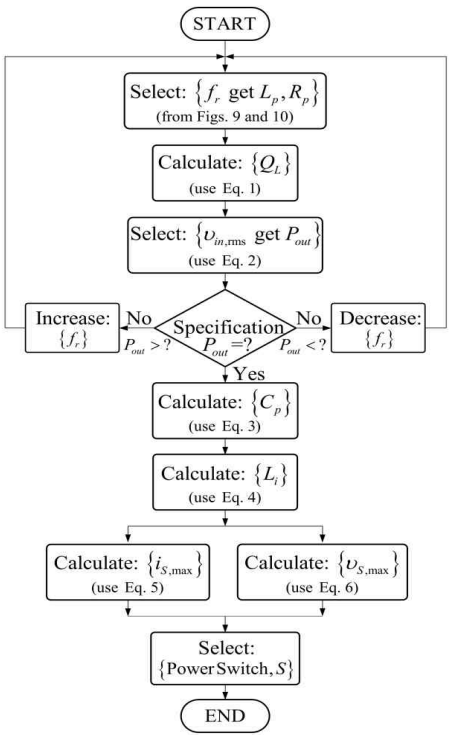


Fig. 11. Design flowchart of the Class-D current-source resonant inverter using a parallel load network under large-signal excitation for the zero-ripple line current domestic induction cooker

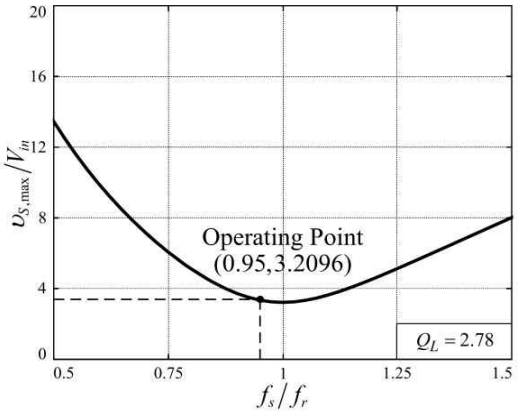


Fig. 12. Normalized maximum switch voltage $\upsilon_{S,\max}/V_{in}$ is plotted as a function of frequency ratio f_s/f_r

4. Find the choke inductance L_i, the expected maximum ripple utility-line input current $i_{rip,\max}$ was approxi-mately.
5. Find the maximum switch current $i_{S,\max}$, which is equal to amplitude of the utility-line input current I_{in}.
6. Calculate the maximum switch voltage $\upsilon_{S,\max}$. The normalized maximum switch voltage $\upsilon_{S,\max}/V_{in}$ is plotted as a function of the frequency ratio f_s/f_r as shown in Fig. 12.

3.2 Design of the Class-D current-source inverter

The 2,500-W Class-D current-source resonant inverter using a parallel load network under large-signal excitation for the zero-ripple line current domestic induction cooker was designed to handle a utility-line rms voltage $\upsilon_{in,\text{rms}}$ of 220 V and a line frequency f_L of 50 Hz. It was assumed that the domestic induction cooker drew a sine wave utility-line input current, the inverter efficiency η_I was equal to 0.96. It were assumed that the resonant circuit efficiency $\eta_r = R_p/R = 0.98$ and the frequency ratio $\omega_s/\omega_r = 0.95$. The resonant frequency f_r = 60 kHz is selected. From Figs. 9 and 10 at 2,500 W situation line, we achieve the parallel inductance L_p = 90.35 μH and the load resistance R_p = 96.56 Ω, respectively. The loaded quality factor Q_L value is given by

$$Q_L = \frac{R}{\omega_r L_p} = \frac{94.63}{2\pi \times 60 \times 10^3 \times 90.35 \times 10^{-6}} = 2.78 \tag{1}$$

The utility-line rms voltage $\upsilon_{in,\text{rms}}$ = 220 V is specified. Thus, the output power P_{out} is calculated by

$$P_{out} = \frac{\pi^2 \eta_I^2 \upsilon_{in,\text{rms}}^2 \left[1 + \left(Q_L\left(\frac{\omega_s}{\omega_r} - \frac{\omega_r}{\omega_s}\right)\right)^2\right]}{2R_p \eta_{rc}^2}$$

$$= \frac{\pi^2 \times 0.96^2 \times 220^2 \left[1 + \left(2.78\left(0.95 - \frac{1}{0.95}\right)\right)^2\right]}{2 \times 96.56 \times 0.98^2} \tag{2}$$

$$= 2{,}566.83 \text{ W}$$

The value of the parallel capacitor C_p is determined by

$$C_p = \frac{Q_L}{\omega_r R} = \frac{2.78}{2\pi \times 60 \times 10^3 \times 94.63} = 77.93 \text{ nF} \tag{3}$$

The minimum value of the choke inductor L_i is given by

$$L_i = \frac{V_{in}}{2 f_s i_{rip,\max}} = \frac{311}{2 \times 57 \times 10^3 \times 0.2} \geq 13.65 \text{ mH} \tag{4}$$

Let us assume that the maximum ripple utility-line input current $i_{rip,\max}$ in the choke inductor less than 0.2 A. The maximum switch current $i_{S1,\max} = i_{S2,\max} = i_{S,\max}$ is equal to amplitude of the induction cooker utility-line input current I_{in}, which is calculated from

$$i_{S,\max} = \frac{\sqrt{2} P_{out}}{\eta_I V_{irms}} = \frac{\sqrt{2} \times 2{,}566.83}{0.96 \times 220} = 17.19 \text{ A} \tag{5}$$

The maximum switch voltage $\upsilon_{S1,\max} = \upsilon_{S2,\max} = \upsilon_{S,\max}$ is given by

$$\upsilon_{S,\max} = \frac{\sqrt{2}\upsilon_{in,\text{rms}} \pi \eta_I \sqrt{1 + Q_L^2\left(\frac{\omega_s}{\omega_r} - \frac{\omega_r}{\omega_s}\right)^2}}{\eta_r}$$

$$= \frac{\sqrt{2} \times 220 \times \pi \times 0.96 \sqrt{1 + 2.78^2\left(0.95 - \frac{1}{0.95}\right)^2}}{0.98} \tag{6}$$

$$= 995.70 \text{ V}$$

Therefore, a 1,400-V/20-A IGBT part number IRG7PK35UD1PBF from IR series with 600-V/15-A fast recovery diode part number DSEC30-60A from IXYS are used for the unidirectional switches S_1 and S_2.

3.3 Conduction loss analysis

The proposed topology is composed of six major components. These six components are the power IGBTs, power diodes, capacitor, and inductors. The equivalent circuit of the proposed topology for a conduction loss analysis is shown in Fig. 13. The IGBTs are modeled by switch with the constant voltage source V_{FQ} and the on-resistance r_{FQ}. The power diodes are modeled by the series connection of the constant voltage source V_{FD} and the on-

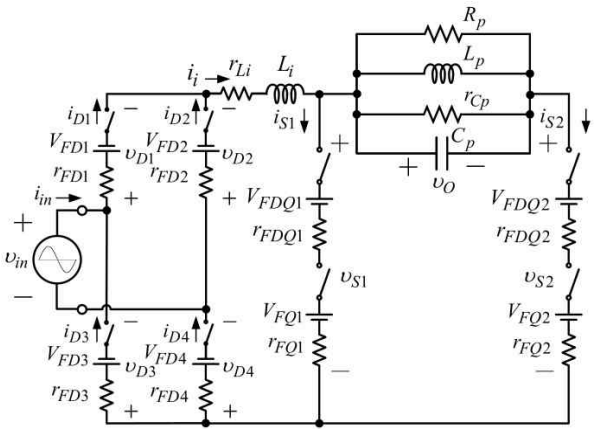


Fig. 13. Equivalent circuit for the conduction loss analysis

resistance r_{FD}. The series and parallel resistances r_{Li}, r_{Cp} represent the equivalent resistances of the filter inductor L_i and parallel capacitor C_p, respectively. The average value of the bridge-rectifier diode currents i_{D1}-i_{D4} is equal to the average value of the half-wave rectified utility-line input current. Consequently, the power loss in the diodes D_1-D_4 due to the forward voltage V_{FDB} is obtained as

$$P_{D,Bridge} = \frac{V_{FDB} i_{in,\max}}{\pi} = \frac{1.1 \times 17.19}{\pi} = 6.02\,\text{W} \tag{7}$$

The bridge-rectifier was built using a (D20SB60, LRC) standard-recovery diode with a *pn* junction voltage (V_{FDB} = 1.1 V). The average value of the switch current $i_{S,\text{avg}}$ is given by (8). Therefore, the power loss in the diodes D_{Q1}, D_{Q2} and the IGBTs Q_1, Q_2 due to the forward voltage V_{FDQ}, V_{FQ} are given by

$$i_{S,\text{avg}} = \frac{i_{S,\max}}{\pi} = \frac{17.19}{\pi} = 5.47\,\text{A} \tag{8}$$

$$P_{CE,\text{on}} = V_{CE,\text{on}} i_{S,\text{avg}} = 1.8 \times 5.47 = 9.84\,\text{W} \tag{9}$$

$$P_{DQ} = V_{FDQ} i_{S,\text{avg}} = 1.8 \times 5.47 = 9.84\,\text{W} \tag{10}$$

The unidirectional switches were built using the (IRG7PK35UD1PBF, IR) IGBT with a collector-to-emitter saturation voltage ($V_{CE,\text{on}}$=1.8 V) and the (DSEC30-60A, IXYS) fast-recovery diode with a forward voltage (V_{FDQ} = 1.8 V). The parasitic series resistance of the filter inductor r_{Li} is 220 mΩ and the rms value of the full-wave rectified sinusoidal current $i_{i,\text{rms}}$ is given by (11). Thus, the conduction loss in the inductor L_i is obtained by

$$i_{i,\text{rms}} = \frac{i_{S,\max}}{\sqrt{2}} = \frac{17.19}{\sqrt{2}} = 12.16\,\text{A} \tag{11}$$

$$P_{Li} = i_{i,\text{rms}}^2 r_{Li} = 12.16^2 \times 0.22 = 32.53\,\text{W} \tag{12}$$

The measured quality factor of the parallel capacitor $Q_{Cp} \approx 1{,}000$ is measured by using the precision LCR meter. The parasitic parallel resistance of the parallel capacitor C_p and the rms value of the output voltage υ_O are given by (13) and (14). Thus, the conduction loss in the parallel capacitor C_p is calculated by

$$r_{Cp} = \frac{Q_{Cp}}{\omega_s C_p} = \frac{1{,}000}{2\pi \times 57 \times 10^3 \times 75 \times 10^{-9}} = 37.23\,\text{k}\Omega \tag{13}$$

$$\begin{aligned} \upsilon_{O,\text{rms}} &= \sqrt{\frac{\pi^2 \eta_I^2 \upsilon_{in,\text{rms}}^2 \left[1 + \left(Q_L\left(\frac{\omega_s}{\omega_r} - \frac{\omega_r}{\omega_s}\right)\right)^2\right]}{2\eta_r^2}} \\ &= \sqrt{\frac{\pi^2 \times 0.96^2 \times 220^2 \left[1 + \left(2.78\left(0.95 - \frac{1}{0.95}\right)\right)^2\right]}{2 \times 0.98^2}} \\ &= 497.85\,\text{V} \end{aligned} \tag{14}$$

$$P_{Cp} = \frac{\upsilon_{O,\text{rms}}^2}{r_{Cp}} = \frac{497.85^2}{37.23 \times 10^3} = 6.66\,\text{W} \tag{15}$$

The total conduction loss P_C is obtained by

$$\begin{aligned} P_C &= 2P_{D,Bridge} + 2P_{CE,\text{on}} + 2P_{DQ} + P_{Li} + P_{Cp} \\ &= 2 \times 6.02 + 2 \times 9.84 + 2 \times 9.84 + 32.53 + 6.66 \\ &= 90.59\,\text{W} \end{aligned} \tag{16}$$

The efficiency of the inverter η_I associated with the conduction loss is calculated by

$$\begin{aligned} \eta_I &= \frac{P_{out}}{P_{in}} \times 100\% = \frac{P_{out}}{P_{out} + P_C} \times 100\% \\ &= \frac{2{,}566.83}{2{,}566.83 + 90.59} \\ &= 96.59\% \end{aligned} \tag{17}$$

The switching losses in the bridge-rectifier diodes and the active switch are very small. Thus, their effects were neglected. The copper loss of the planar coil winding and the core loss of the ferrite bars are included in parallel resistance R_p. These losses are considered to be very small

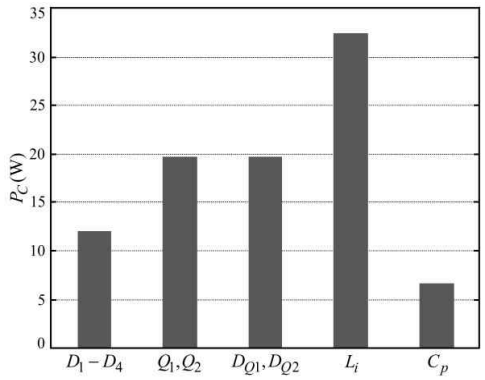


Fig. 14. Conduction loss distribution

when compared with work load of vessel. For simplicity's sake, we omit them in this current stage. Fig. 14 depicts the conduction loss distribution of the proposed topology in steady state.

4. Simulation and Experimental Results

4.1 Simulation results

Table 1 shows a comparison of the circuit parameters between theoretical and simulation, which are calculated from 2,500-W test-bench and LCR meter. It can be observed that the difference of these parameters from low-signal excitation is quite large when compared with the above analysis in Section 3 and the parameters from large-signal excitation. Fig. 15 shows the simulated waveforms of the output voltage υ_O the parallel inductor current i_{Lp}, and the parallel capacitor current i_{Cp}, which is calculated by using the coil-vessel induction load network from the 2,500-W test-bench and the LCR meter, respectively. The switch voltage υ_{S1} and current i_{S1} waveforms, which is calculated by using the coil-vessel induction load network from the 2,500-W test-bench and the LCR meter as illustrated in Fig. 16. It can be noticed that these waveforms in accordance with the circuit parameters shown in Table 1.

Table 1. Comparison of the circuit parameters between theoretical and simulations (calculated from 2,500-W test-bench and LCR meter)

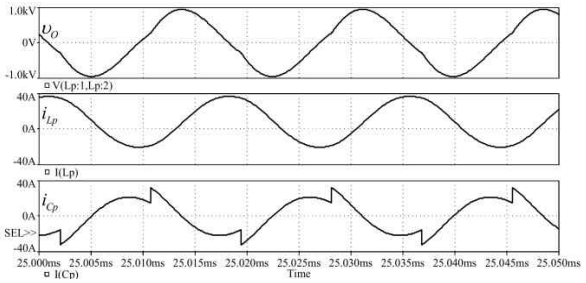
Parameter	Theoretical	Simulation	
		Test-bench (2,500 W)	LCR meter (Coil-Vessel)
P_{in}	2,673.78 W	2,751.5 W	2,063.3 W
P_{out}	2,566.83 W	2,668.1 W	2,012 W
f_r	60 kHz	60.52 kHz	60 kHz
R_p	96.56 Ω	96.56 Ω	137 Ω
L_p	90.35 μH	90.35 μH	71.32 μH
C_p	77.93 nF	77.93 nF	98.59 nF
$\upsilon_{O,\mathrm{rms}}$	497.85 V	499.79 V	525.021 V
$i_{S,\mathrm{avg}}$	5.47 A	6.08 A	4.4219 A
$\upsilon_{S,\max}$	995.7 V	951.55 V	1,024.5 V
$i_{S,\max}$	17.19 A	16.87 A	12.937 A

Table 2. System parameters and devices type of the experimental prototype

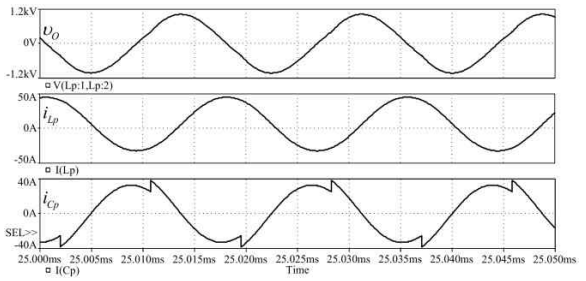
Parameter	Value and part number	Type
D_1-D_4	D20SB60	Standard-recovery diode, LRC
Q_1, Q_2	IRG7PK35 UD1PBF	IGBT, IR
D_{Q1}, D_{Q2}	DSEC30-60A	Fast-recovery diode, IXYS
L_i	20 mH	T184-26, Micrometal Cores
R_p	93.62 Ω	Equivalent resistance of vessel at f = 60 kHz
L_p	86.64 μH	Diameter 180 mm, 25 turns
C_p	75 nF	Polypropylene

4.2 Experimental results

According to the above analysis in Section 3, the proposed domestic induction cooker with the Class-D current-source resonant inverter using a parallel load network under large-signal excitation for the zero-ripple line current induction cooker was constructed. Table 2 shows the system parameters and devices type of the

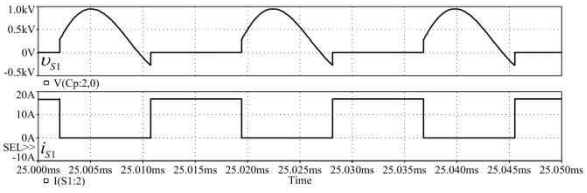


(a)

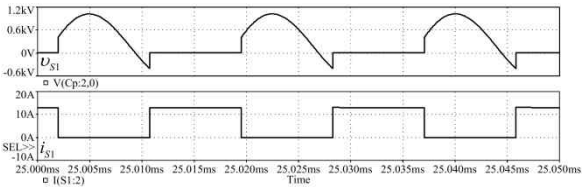


(b)

Fig. 15. Simulated waveforms of the output voltage υ_O, parallel inductor current i_{Lp}, and parallel capacitor current i_{Cp}, which is calculated by using coil-vessel induction load network from: (a) 2,500-W test-bench, (b) LCR meter



(a)



(b)

Fig. 16. Simulated switch voltage υ_{S1} and switch current i_{S1} waveforms of S_1, which is calculated by using the coil-vessel induction load network from: (a) 2,500-W test-bench. (b) LCR meter

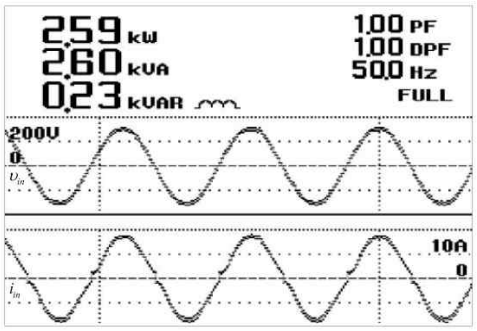


Fig. 17. Experimental waveforms of the utility-line input voltage and the utility-line input current

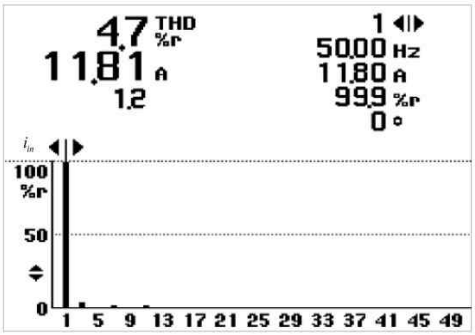


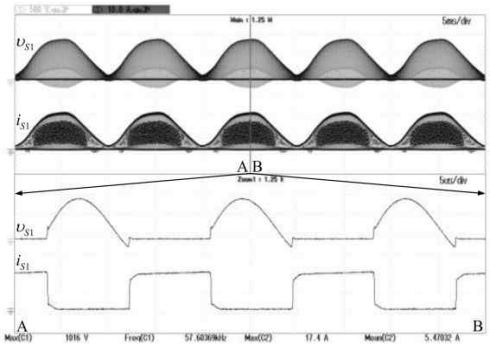
Fig. 18. Harmonic content of the utility-line input current

Table 3. Comparison of circuit parameters calculated by using coil-vessel induction load network from 2,500-W test-bench and LCR meter

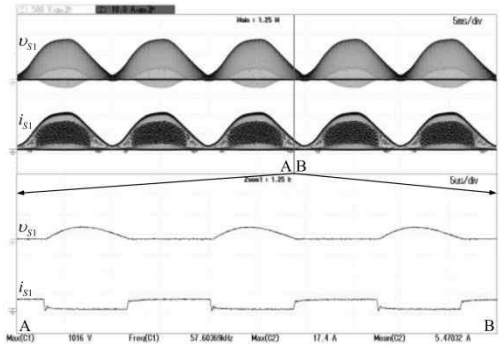
Parameter	Test-bench (2,500 W)	LCR meter (Coil-Vessel)	Difference
P_{in}	2,673.78 W	2,199.73 W	-17.73%
P_{out}	2,566.83 W	2,111.74 W	-17.73%
f_r	60 kHz	60 kHz	0%
R_p	96.56 Ω	137 Ω	41.88%
L_p	90.35 μH	71.32 μH	-21.06%
C_p	77.93 nF	98.59 nF	26.51%
$\upsilon_{O,\text{rms}}$	497.85 V	537.87 V	8.04%
$i_{S,\text{avg}}$	5.47 A	4.5 A	-17.73%
$\upsilon_{S,\text{max}}$	995.7 V	1,075.75 V	8.04%
$i_{S,\text{max}}$	17.19 A	14.14 A	-17.74%

experimental prototype. The switching frequency f_s is fixed at 57 kHz, and the utility-line rms voltage is set to 220 V with a line frequency f_L of 50 Hz. The utility-line input power, utility-line input PF, and THD_i were measured with a power analyzer (FLUKE model 43B). The measured utility-line input power was about 2.59 kW, while the utility-line input PF was close to 1 as shown in Fig. 17. The THD_i was 4.7% as displayed in Fig. 18.

The oscilloscope, differential probe, and current probe used in this experiment were YOKOGAWA models DL2024, 700924, and 701932, respectively.



(a)



(b)

Fig. 19. Measured of υ_{S1} (500 V/div) and i_{S1} (10 A/div): (a) near the peak of utility-line input voltage. (b) near the zero crossing of utility-line input voltage, with bottom two waveforms as zoomed-in views of top two waveforms

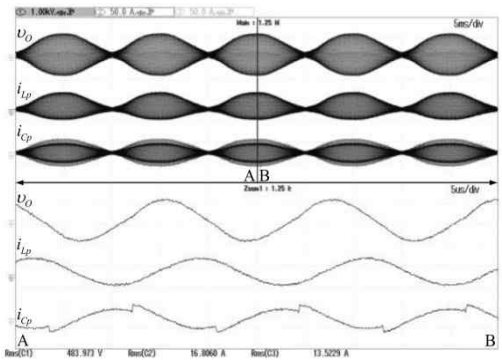


Fig. 20. Experimental waveforms of υ_O (1,000 V/div), i_{Lp} (50 A/div), and i_{Cp} (50 A/div), with lower three waveforms as zoomed-in views of top three waveforms

The experimental waveforms of the switch voltage υ_{S1} and the switch current i_{S1} of the unidirectional switch comprises the IGBT Q_1 in series with the diode D_{Q1} near the peak and the zero-crossing of the utility-line input voltage at full load condition are shown in Fig. 19(a) and (b), respectively. Fig. 20 depicts the measured waveforms of the output voltage υ_O, the planar coil-vessel current i_{Lp}, and the parallel capacitor current i_{Cp}. It can be seen that

these waveforms roughly match the key waveforms shown in Fig. 5. The experimental waveforms of the utility-line input voltage υ_{in} , the utility-line input current i_{in}, the utility-line input power p_{in}, the output voltage υ_O , the planar coil-vessel current i_{Lp}, and the output power of the Class-D inverter p_{out} are shown in Fig. 21. The utility-line input power P_{in} is 2,599.13 W and the output power of the resonant inverter P_{out} is 2,501.93 W. The efficiency of the proposed induction cooker was $\eta_I = (2{,}501.93/2{,}599.13) \times 100\% = 96.26\%$.

Table 3 shows a comparison of circuit parameters calculated from 2,500-W excitation test-bench and LCR meter. It can be seen that the difference of these parameters are quite large. Therefore, the induction load parameters from low-signal excitation with LCR meter is not suitable for this application. A comparison of theoretical parameters calculated from 2,500-W excitation test-bench and experimental results is given in Table 4. The difference between the theoretical and the experimental values are almost all under 3%, indicating a good agreement. Finally, Table 5 shows keys performance comparison among the Class-D current-source parallel resonant inverter for the induction heating application. It can be noticed that the proposed Class-D current-source resonant inverter using a parallel load network under large-signal excitation has features of more accurate results and the proposed scheme provides a more systematic, simple, and feasible solution than the conventional Class-D current-source resonant inverter using series-parallel *R-L* and *C* load network load network under low-signal excitation. Moreover, the devices stress and power loss analysis are described.

Table 4. Comparison between theoretical (calculated from 2,500-W test-bench) and experimental circuit parameters

Parameter	Theoretical	Experimental	Difference
P_{in}	2,673.78 W	2,599.13 W	-2.79%
P_{out}	2,566.83 W	2,501.93 W	-2.53%
f_r	60 kHz	60.63 kHz	1.05%
R_p	96.56 Ω	93.62 Ω	-3.04%
L_p	90.35 μH	86.64μH	-4.11%
C_p	77.93 nF	75 nF	-3.76%
$\upsilon_{O,\mathrm{rms}}$	497.85 V	483.97 V	-2.79%
$i_{S,\mathrm{avg}}$	5.47 A	5.47 A	0%
$\upsilon_{S,\mathrm{max}}$	995.7 V	1,016 V	2.04%
$i_{S,\mathrm{max}}$	17.19 A	17.4 A	1.22%

5. Conclusion

This paper has presented the step-by-step design procedure explained with design example based on the principle of the Class-D current-source resonant inverter with the simplified load network model that is the parallel resonant equivalent circuit under large-signal excitation for the zero-ripple line current domestic induction cooker which has the following characteristics:

1. It is ensures more accurate results and the proposed scheme provides a more systematic, simple, and feasible solution than the conventional resonant inverter using series-parallel *R-L* and *C* load network under low-signal excitation.
2. The inherent ripple cancellation technique with the Class-D current-source resonant inverter, the line current of the proposed topology is ripple free. As a result, the differential mode EMI filter is not needed and high power quality in utility-line can be obtained.
3. The standard-recovery diodes for the bridge-rectifier can be employed.
4. The devices stress and power loss analysis of induction cooker with a parallel load network under large-signal excitation are described.

A prototype designed for a 2,500-W domestic induction cooker was built and tested to verify the theoretical analysis. The experimental results show that the zero-ripple line current Class-D current-source resonant inverter for use in domestic induction cooker with the parallel resonant equivalent circuit had a PF close to 1, a 4.7% THD_i, and an efficiency of 96.26% in full-power condition. Finally, the difference between the theoretical and the experimental values are almost all under 3%, indicating a good agreement.

Acknowledgements

This work was supported in part by the Thailand

Table 5. Comparison among current-source resonant inverter for the induction heating applications

Item	[16]	[17]	[18]	[19]	[28]	[29]	[30]	Proposed
Standard line voltage	No	No	Yes	No	No	No	No	Yes
Induction-load characterization	Series- parallel *R-L* and *C*	Series-parallel *R-L* and *C*	Series-parallel *R-L* and *C*	Series-parallel *R-L* and *C*	Series-parallel *R-L* and *C*	Series-parallel *R-L* and *C*	Series-parallel *R-L* and *C*	Parallel *RLC*
Low/large-signal excitation	Low	Low	Low	Low	Low	Low	Low	Large
Design example	No	No	No	No	No	No	No	Yes
Device stress design	No	No	No	No	No	No	No	Yes
Power loss analysis	No	No	Yes	No	No	No	No	Yes

Research Fund, the Commission on Higher Education, and King Mongkut's University of Technology North Bangkok under Grant No. TRG5880088.

References

[1] E. J. Davies, and P. Simpson, "Induction Heating Handbook," *McGraw-Hill*, UK, 1979.

[2] S. Zinn and S. L. Semiatin "Elements of Induction Heating," *ASM International*, Metals Park, Ohio, U.S.A, 1991.

[3] D. Y. Lee and D. S. Hyun, "A New Hybrid Control Scheme using Active-Clamped Class-E Inverter with Induction Heating Jar for High Power Applications," *Journal of Power Electronics*, vol. 2, no. 2, pp. 104-111, Apr. 2002.

[4] H. Sarnago, O. Lucia, A. Mediano, and J. M. Bu rdio, "A Class-E Direct AC-AC Converter with Multicycle Modulation for Induction Heating Syst ems," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 5, pp. 2521-2530, May 2014.

[5] P. Charoenwiangnuea, C. Ekkaravarodome, I. Boonyaroonate, P. Thounthong, and Kamon Jirasereeamornkul, "Design of Domestic Induction Cooker Based on Optimal Operation Class-E Inverter with Parallel Load Network Under Large-Signal Excitation," *Journal of Power Electronics*, vol. 17, no. 4, pp. 892-904, Jul. 2017.

[6] I. Millan, J. M. Burdio, J. Acero, O. Lucia, and S. Llorente, "Series Resonant Inverter with Selective Harmonic Operation Applied to All-Metal Domestic Induction Heating," *IET Power Electronics*, vol. 4, no. 5, pp. 587-592, May 2011.

[7] H. Sarnago, O Lucia, A. Mediano, and J. M. Burdio, "Class-D/DE Dual-Mode-Operation Resonant Converter for Improved-Efficiency Domestic Induction Heating System," *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1274-1285, Mar. 2013.

[8] H. Sarnago, O Lucia, A. Mediano, and J. M. Burdio, "Direct AC-AC Resonant Boost Converter for Efficient Domestic Induction Heating Applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1128-1139, Mar. 2014.

[9] O. Jimenez, O Lucia, I. Urriza, L. A. Barragan, and D.Navarro, "Analysis and Implementation of FPGA-Based Online Parametric Identification Algorithms for Resonant Power Converters," *IEEE Transactions on Industrial Informatics*, vol. 10, no. 2, pp. 1144-1153, May 2014.

[10] B. Nagarajan, R. R. Sathi, and P. Vishnuram, "Power Tracking Control of Domestic Induction Heating System using Pulse Density Modulation Scheme with the Fuzzy Logic Controller," *Journal of Electrical Engineering & Technology*, vol. 9, no. 6, pp. 1978-1987, Nov. 2014.

[11] H. Sarnago, O. Lucia, A. Mediano, and J. M. Burdio, "Analytical Model of the Half-Bridge Series Resonant Inverter for Improved Power Conversion Efficiency and Performance," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4128-4143, Aug. 2015.

[12] P. K. Sharath, N. Vishwanathan, and M. K. Bhagwan, "Buck-Boost Interleaved Inverter Configuration for Multiple-Load Induction Cooking Application," *Journal of Electrical Engineering & Technology*, vol. 10, no. 1, pp. 271-279, Jan. 2015.

[13] T. Mishima, Y. Nakagawa, and M. Nakaoka, "A Bridgeless BHB ZVS-PWM AC-AC Converter for High-Frequency Induction Heating Applications," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3304-3315, Jul./Aug. 2015.

[14] H. Sarnago, O Lucia, D. Navarro, and J. M. Burdio, "Operating Conditions Monitoring for High Power Density and Cost-Effective Resonant Power Converters," *IEEE Transactions on Power Electronics*, vol. 51, no. 4, pp. 488-496, Jun. 2016.

[15] A. Dominguez, L. Angel Barragan, J. I. Artigas, A. Otin, I. Urriza, and D. Navarro, "Reduced-Order Models of Series Resonant Inverters in Induction Heating Applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2300-2311, Mar. 2017.

[16] A. Namadmalan, J. S. Moghani, and J. Milimonfared, "A Current-Fed Parallel Resonant Push-Pull Inverter with a New Cascaded Coil Flux Control for Induction Heating Applications," *Journal of Power Electronics*, vol. 11, no. 5, pp. 632-638, Sep. 2011.

[17] A. Namadmalan and J. S. Moghani, "Self-Oscillating Switching Technique for Current Source Parallel Resonant Induction Heating Systems," *Journal of Power Electronics*, vol. 12, no. 6, pp. 851-858, Nov. 2012.

[18] H. Sarnago, O. Lucia, A. Mediano, and J. M. Burdio, "High-Efficiency Parallel Quasi-Resonant Current Source Inverter Featuring SiC Metal-oxide Semiconductor Field-Effect Transistors for Induction Heating Systems with Coupled Inductors," *IET Power Electronics*, vol. 6, no. 1, pp. 183-191, Jan. 2013.

[19] T. Mishima, K. Konishi, and M. Nakaoka, "Current-Source ZCS High-Frequency Resonant Inverter Based on Time-Sharing Frequency Doubler Principle and Induction Heating Applications," *International Conference on Power Electronics and Drive Systems*, pp. 598-603, 9-12 Jun. 2015.

[20] J. Acero, C. Carretero, I. Millan, O. Lucia, R. Alonso, and J. M. Burdio, "Analysis and Modeling of Planar Concentric Windings Forming Adaptable-Diameter Burners for Induction Heating Appliances," *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1546-1558, May 2011.

[21] S. Chudjuarjeen, A. Sangswang, and Chayant Koompai,

"An Improved *LLC* Resonant Inverter for Induction-Heating Applications with Asymmetrical Control," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2915-2925, Jul. 2011.
[22] T. Mishima, C. Takami, and M. Nakaoka, "A New Current Phasor-Controlled ZVS Twin Half- Bridge High-Frequency Resonant Inverter for Induction Heating," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 5, pp. 2531-2545, May 2014.
[23] V. Esteve, J. Jordán, E. S. Kilders, E. J. Dede, E. Maset, J. B. Ejea, and A. Ferreres, "Enhanced Pulse-Density-Modulated Power Control for High-Frequency Induction Heating Inverters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 6905-6914, Nov. 2015.
[24] H. Sarnago, O. Lucia, M. P. Tarragona, and J. M. Burdío, "Dual-Output Boost Resonant Full-Bridge Topology and its Modulation Strategies for High-Performance Induction Heating Applications," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 6, pp. 3554-3561, Jun. 2016.
[25] B. Chuang, L. Hua, J. Kelin, H. Jingang, and L. Hui, "A Novel Multiple-Frequency Resonant Inverter for Induction Heating Applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8162-8171, Dec. 2016.
[26] H. Sarnago, O. Lucia, and J. M. Burdío, "Interleaved Resonant Boost Inverter Featuring SiC module for High-Performance Induction Heating," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1018-1029, Feb. 2017.
[27] T. Mishima, S. Sakamoto, and C. Ide, "ZVS Phase-Shift PWM-Controlled Single-Stage Boost Full-Bridge AC-AC Converter for High-Frequency Induction Heating Applications," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 2054-2061, Mar. 2017.
[28] A. Polsripim, S. Chudjuarjeen, A. Sangswang, P. N. N. Ayudhya, and C. Koompai, "A Soft Switching Class D Current Source Inverter for Induction Heating with Ferromagnetic Load," *International Conference on Power Electronics and Drive Systems*, pp. 877-881, 2-5 Nov. 2009.
[29] J. Jittakort, A. Sangswang, S. Naetiladdanon, C. Koompai, and S. Chudjuarjeen, "A Soft Switching Class D Current Source Inverter for Induction Heating With Non-Ferromagnetic Load," *European Conference on Power Electronics and Applications*, pp. 1-10, 30 Aug.-1 Sept. 2011.
[30] A. Namadmalan and J. S. Moghani, "Tunable Self-Oscillating Switching Technique for Current Source Induction Heating Systems," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 5, pp. 2556-2563, May 2014.
[31] W. Hurley and J. Kassakian, "Induction Heating of Circular Ferromagnetic Plates," *IEEE Transactions on Magnetics*, vol. 15, no. 4, pp. 1174-1181, Jul. 1979.
[32] T. Tanaka, "A New Induction Cooking Range for Heating Any Kind of Metal Vessels," *IEEE Transactions on Consumer Electronics*, vol. 35, no. 3, pp. 635-641, Aug. 1989.
[33] M. Humza and B. Kim, "Analysis and Optimal Design of Induction Heating Cookers," *Journal of Electrical Engineering & Technology*, vol. 11, no. 5, pp. 1282-1288, Sep. 2016.
[34] M. K. Kazimierczuk and D. Czarkowski, "Resonant Power Converters," 2nd ed., *Wiley*: New York, 1995.
[35] M. K. Kazimierczuk and A. Abdulkarim, "Current-Source Parallel Resonant DC/DC Converter," *IEEE Transactions on Industrial Electronics*, vol. 42, no. 2, pp. 199-208, Apr. 1995.
[36] H. W. E. Koertzen, V. J. D. Wyk, and J. A. Ferreira, "An Investigation of the Analytical Computation of Inductance and AC Resistance of the Heat-Coil for Induction Cookers," *International Conference on Industry Applications Society Annual Meeting*, vol. 1, pp. 1113-1119, Oct. 1992.

Chainarin Ekkaravarodome He received the B.Ind.Tech. degree in industrial electrical technology from King Mongkut's Institute of Technology North Bangkok, Bangkok, Thailand, in 2003, and the M.E. and Ph.D. degrees in electrical engineering and energy technology from King Mongkut's University of Technology Thonburi, Bangkok, Thailand, in 2005 and 2009, respectively. He is currently an Assistant Professor with the Department of Instrumentation and Electronics Engineering, Faculty of Engineering, King Mongkut's University of Technology North Bangkok. His current research interests include electronic ballasts, induction heating, LED drivers, power-factor-correction circuits, resonant rectifiers, and soft-switching power converters.

Phatiphat Thounthong He received the B.S. and M.E. degrees in electrical engineering from King Mongkut's Institute of Technology North Bangkok, Bangkok, Thailand, in 1996 and 2001, respectively, and the Ph.D. degree in electrical engineering from Institut National Polytechnique de Lorraine (INPL)-Université de Lorraine, Nancy-Lorraine, France, in 2005. Since 2012, he has been a Full Professor in Department of Teacher Training in Electrical Engineering, King Mongkut's University of Technology North Bangkok. He is the author of 85 scientific papers (including 17

papers in IEEE Transactions/Magazines) published in Scopus with citations = 1,829 times (without self-citations) and h-index=20(without self-citations). His current research interests include power electronics, electric drives, electric vehicles, electrical devices (fuel cells, photovoltaic, wind turbine, batteries, and supercapacitors), nonlinear controls, and observers. Dr. Thounthong received the First Prize Paper Award from the IEEE Industry Applications Society-Industrial Automation and Control Committee in 2009 (TX, USA), the Third Prize Outstanding Paper Award from the IEEE International Telecommunications Energy Conference in 2015 (Osaka, Japan), the Best Poster Presentation Award from the IEEE International Conference on Electrical Machines in 2010 (Rome, Italy), 2012 TRF-CHE-Scopus Young Researcher Awards (Engineering & Multidisciplinary Technology), and 2017 TRF-CHE-Scopus Researcher Awards (Engineering & Multidisciplinary Technology).

Kamon Jirasereeamornkul He received the B.E. and M.E. degrees in electrical engineering, and the Ph.D. degree in electrical and computer engineering from King Mongkut's University of Technology Thonburi, Bangkok, Thailand, in 1997, 2001, and 2006, respectively. He is currently an Assistant Professor with the Department of Electronic and Telecommunication Engineering, Faculty of Engineering, King Mongkut's University of Technology Thonburi. His current research interests include electronic ballasts, induction heating, LED drivers, power-factor-correction circuits, resonant rectifiers, and soft-switching power converters.