J Electr Eng Technol.2018; 13(3): 1212-1222
http://doi.org/10.5370/JEET.2018.13.3.1212

ISSN(Print) 1975-0102
ISSN(Online) 2093-7423

Common-mode Voltage Reduction for Inverters Connected in Parallel Using an MPC Method with Subdivided Voltage Vectors

Joon Young Park*, Jiook Sin, Yeongsu Bak*, Sung-Min Park*** and Kyo-Beum Lee†**

Abstract – This paper presents a model predictive control (MPC) method to reduce the common-mode voltage (CMV) for inverters connected in parallel, which increase the capacity of energy storage systems (ESSs). The proposed method is based on subdivided voltage vectors, and the resulting algorithm can be applied to control the inverters. Furthermore, we use more voltage vectors than the conventional MPC algorithm; consequently, the quality of grid currents is improved. Several methods were proposed in order to reduce the CMV appearing during operation and its adverse effects. However, those methods have shown to increase the total harmonic distortion of the grid currents. Our method, however, aims to both avoid this drawback and effectively reduce the CMV. By employing phase difference in the carrier signals to control each inverter, we successfully reduced the CMV for inverters connected in parallel, thus outperforming similar methods. In fact, the validity of the proposed method was verified by simulations and experimental results.

Keywords: Parallel-connected inverters, Grid-connected inverters, Common-mode voltage, Model predictive control, Phase-shifted carrier.

1. Introduction

Recently, the demand for the use of renewable energy sources, such as solar, wind, and biomasses, has rapidly increased given the depletion of existing fossil fuel deposits and environmental pollution. However, these sources might be unpredictable and unreliable due to changing environmental conditions. In this regard, energy storage systems (ESSs) are used for storing the power generated by these sources in battery systems. In addition, ESSs connected to the grid are used for storing the additional power when its cost is low, such as at night.

Furthermore, ESSs connected to the grid can improve the energy quality and maximize its efficiency by supplying the stored power whenever required. The ESS is usually composed of two-level inverters for power conversion, given their many advantages including reduction of production costs and varied applicability. Various studies on grid-connected ESSs using two-level inverters were performed for various applications. For instance, grid-connected high-capacity ESSs to store extra power are required in industrial applications [1-5]. To extend the capacity of ESSs sharing a common grid, methods for connecting the inverters in parallel can be used [6-10]. For this application, the three-phase output of the connected inverters results in grid currents that are the sum of the currents of all inverters and should be accurately controlled.

In general, grid currents of ESSs are regulated using a proportional-integral (PI) controller [11]. However, this type of controller uses the pulsation of input/output currents, which generates high noise levels at the ESS output [12]. This problem can be solved by decreasing the system response time and increasing efficiency. For instance, model predictive control (MPC) is more reliable and accurate than other methods such as PI control. However, the conventional MPC algorithm increases the total harmonic distortion (THD) of grid currents in the inverter, because it generates one state change per sampling period [13-21]. According to the IEEE standard on the subject, the THD of the grid currents should not exceed 5%.

To reduce the THD of the grid currents in the system using the conventional MPC, an algorithm with subdivided voltage vectors was proposed [22, 23]. For this MPC algorithm, the optimum voltage vector is obtained from the subdivided voltage vectors. The reference voltage vectors have a more sinusoidal shape than those in the conventional MPC algorithm; thus, the THD decreases.

However, a common-mode voltage (CMV) is generated at the ESS inverters. The CMV can cause multiple problems such as leakage currents, a faulty activation of the current detection circuit, and radiation of electromagnetic interference noise in the system [24]. Many filtering methods for the inverter output were studied to reduce the CMV. However, these methods present some disadvantages including the increased volume, weight, and cost of the

† Corresponding Author: Dept. of Electrical and Computer Engineering, Ajou University, Korea. (kyl@ajou.ac.kr)
* Dept. of Electrical and Computer Engineering, Ajou University, Korea. (park@patguide.com, wov2@ajou.ac.kr)
** LS mecapion, Daegu, Korea. (sinjo527@naver.com)
*** Dept. of Electronic and Electrical Engineering, Hongik University, Korea. (smpark@hongik.ac.kr)
Received: June 17, 2017; Accepted: December 18, 2017

system because of the additional LC filters. In addition, several PWM methods to decrease the CMV were studied [25-29]. Most of them focus on removing the zero-voltage vector from the PWM switching, thus reducing the CMV. However, the complexity of the control system is highly increased. Moreover, the THD of the grid currents also increases given the active-voltage vectors used to substitute the zero-voltage vectors.

In this paper, we propose a reduction method for the CMV in parallel-connected inverters using an MPC algorithm with subdivided voltage vectors. This method aims to effectively reduce both the CMV and the THD of the grid currents. The validity of the proposed method is verified through simulations and experimental results.

2. Topology and Control Method for Two-Level Inverters in Parallel

2.1 Topology

Fig. 1 illustrates a grid-connected ESS composed of two inverters in parallel. The inverters share a common DC bus and are connected in parallel to extend the ESS capacity for high-power applications. Each inverter has filtering inductors for connection to the grid. In addition, the DC bus is divided to deliver positive and negative voltages and has a neutral point (O). A controller area network (CAN) is used for communication between the inverters.

2.2 Conventional MPC algorithm

In ESSs as that shown in Fig. 1, the PI controller is generally used to control the grid currents, but it presents disadvantages such as pulsation. On the other hand, an MPC can overcome the drawbacks of the PI controller. In addition, MPC allows to operate in real-time reference tracking and produce minimum error. The MPC algorithm is useful to predict the next state of the system based on a model. In particular, the system model for a three-phase two-level inverter is defined as

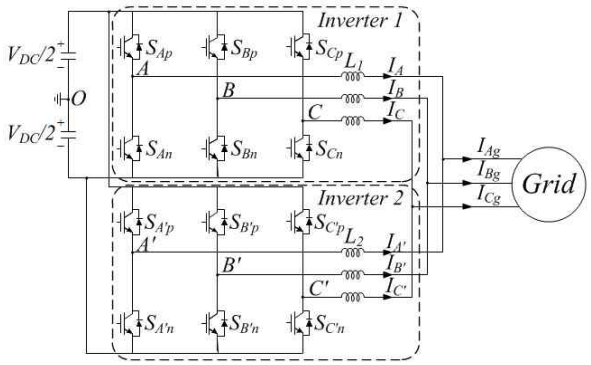

Fig. 1. Parallel-connected two-level inverters

$$v = Ri + L\frac{di}{dt} + e\,, \tag{1}$$

where v, i, and e represent the inverter voltage, grid current, and grid voltage vectors, respectively; R and L are the filter resistance and inductance, respectively. In order to express (1) in discrete time, the forward Euler method is used, and the corresponding equation for the system current is defined as

$$i(k+1) = i(k) + \frac{T_s}{L}\left(v(k) - Ri(k) - e(k)\right), \tag{2}$$

where T_s and k represent the sampling period and switching step, respectively. Considering all the possible combinations of switching, eight voltage vectors can be obtained as shown in Fig. 2(a). Therefore, the eight current vectors are predicted from (2). To determine the optimum voltage vector in the possible voltage vectors, a cost function can be given by

$$g = \left|i_d^{ref}(k+1) - i_d(k+1)\right| + \left|i_q^{ref}(k+1) - i_q(k+1)\right|, \tag{3}$$

where $i_d^{ref}(k+1)$ and $i_q^{ref}(k+1)$ are d-q axis reference currents. Additionally, $i_d(k+1)$ and $i_q(k+1)$ are d-q axis predictive currents depending on the possible voltage vectors in the d-q stationary reference frame. As a result, the optimum voltage vector minimizing the cost function can be obtained [31-33] and it is applied to the inverter during the T_s.

In the conventional MPC algorithm, the grid current and grid voltage are measured after the switching state is applied. Additionally, the predictive currents for all the possible switching combinations are obtained. Through the calculation of the cost function, the optimum voltage vector is determined and the switching state depending on the optimum voltage vector is stored.

2.3 MPC algorithm with subdivided voltage vectors

The conventional MPC algorithm provides low-quality grid currents because only eight voltage vectors can be

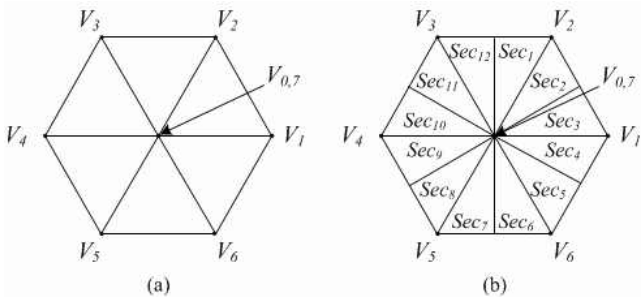

Fig. 2. Space vector diagram of (a) conventional MPC algorithm and (b) proposed MPC algorithm with subdivided voltage vectors

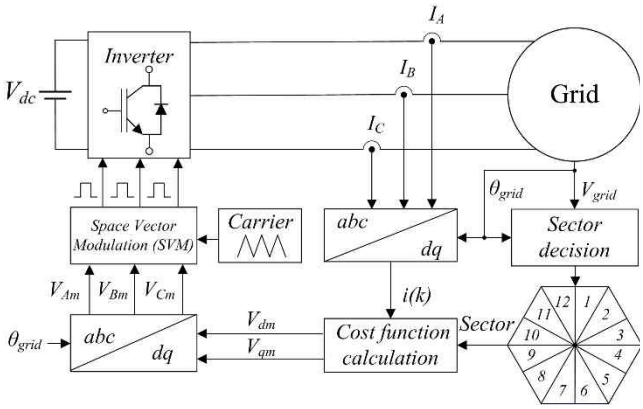

Fig. 3. Block diagram of the proposed MPC algorithm with subdivided voltage vectors in a grid-connected inverter

obtained from the switching states of the inverter, as shown in Fig. 2(a). Consequently, only one switching state can be active in a control period. On the other hand, we propose an MPC algorithm with subdivided voltage vectors to control the inverters. The cost function for the proposed MPC algorithm with subdivided voltage vectors is equal to that of the convectional MPC algorithm as in (3). By using these vectors, the cost function can determine more reference voltage vectors than the conventional MPC algorithm.

The research on the MPC using the subdivided voltage vectors have been extensively studied [34]. In [34], the space vector diagram is divided into 54 sectors as equilateral triangle. However, in case the voltage vectors are excessively divided, it causes the computation load for determination of the optimal voltage vector using the cost function in the MPC algorithm. Contrary to the other research, in this paper, the space vector diagram for the proposed MPC algorithm is divided into 12 sectors as shown in Fig. 2(b). In this case, each sector is formed to a right-angled triangle and the trigonometrical function can be used to calculate the voltage vectors. Therefore, the calculation of the voltage vectors is simple. It will be described later.

Fig. 3 shows the block diagram of the proposed MPC algorithm with subdivided voltage vectors in a grid-connected inverter. These vectors provide several intermediate voltages, as shown in Fig. 2(b). Moreover, the vectors can be used to find the optimized voltage vector in the proposed MPC algorithm. The reference voltage is determined from the cost function, as shown in Fig. 3. The subdivided voltage vectors have a relation of symmetry among them, and can be obtained by using subdivided voltage vectors of Sec_1, Sec_2, and Sec_3.

Fig. 4 shows the voltage vectors of Sec_1, Sec_2, and Sec_3 divided N times. Through the subdivided voltage vector of Sec_1, it is possible to obtain those of Sec_1, Sec_2, and Sec_3 by using symmetrical relationships. The values of the subdivided voltage vectors are defined by (4), (5), and (6)

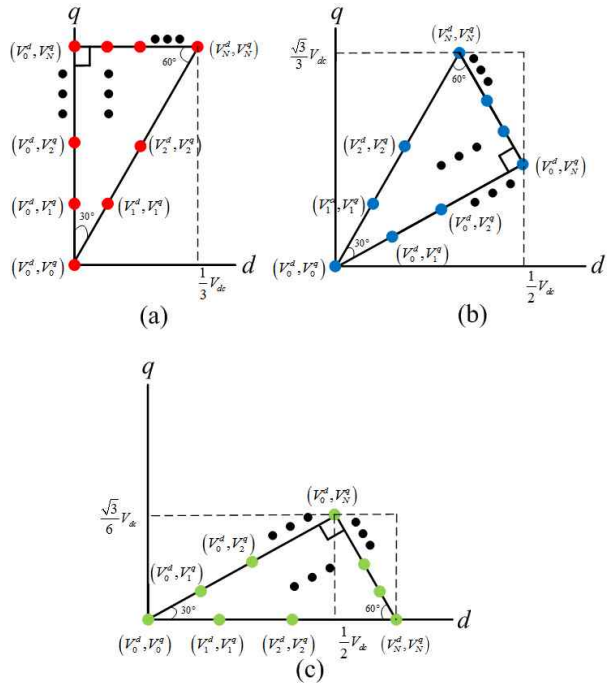

Fig. 4. Subdivided voltage vectors of (a) Sec_1, (b) Sec_2, and (c) Sec_3

for each sector in the d–q axes [22, 23].

$$\left(V_{x_i}^{d_1}, V_{y_j}^{q_1}\right) = \left(\frac{x_i}{N}\frac{1}{3}V_{DC}, \frac{y_i}{N}\frac{\sqrt{3}}{3}V_{DC}\right), \tag{4}$$

$$\left(V_{x_i}^{d_2}, V_{y_j}^{q_2}\right) = \left(\frac{-x_i+3y_j}{N}\frac{1}{6}V_{DC}, \frac{x_i+y_i}{N}\frac{\sqrt{3}}{6}V_{DC}\right), \tag{5}$$

$$\left(V_{x_i}^{d_2}, V_{y_j}^{q_2}\right) = \left(\frac{x_i+3y_j}{N}\frac{1}{6}V_{DC}, \frac{x_i-y_i}{N}\frac{\sqrt{3}}{6}V_{DC}\right), \tag{6}$$

where x_i and y_j are the coordinate values of each sector, N is the number of subdivided voltage vectors, and V_{DC} is the DC-link voltage. Among the subdivided voltage vectors, the optimum voltage vector is obtained and applied to the inverter switching by using space vector modulation (SVM). The different voltage vectors allow an increase in the control switching. Consequently, the quality of the grid currents is higher than that obtained from the conventional MPC algorithm. In addition, the THD of the grid currents is reduced by using the MPC algorithm with subdivided voltage vectors [22, 23].

3. CMV in Two-Level Inverters

The CMV usually appears in ESSs using inverters. The CMV of a two-level inverter is the potential between the star point of the load, such as the grid or a motor, and the neutral point O of the DC bus. Given that the inverter does

Table 1. CMV magnitude according to the switching state

Switching state	Inverter pole voltage			V_{CM}
	V_{AO}	V_{BO}	V_{CO}	
V_0	$-V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}/2$
V_1	$V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}/6$
V_2	$V_{DC}/2$	$V_{DC}/2$	$-V_{DC}/2$	$V_{DC}/6$
V_3	$-V_{DC}/2$	$V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}/6$
V_4	$-V_{DC}/2$	$V_{DC}/2$	$V_{DC}/2$	$V_{DC}/6$
V_5	$-V_{DC}/2$	$-V_{DC}/2$	$V_{DC}/2$	$-V_{DC}/6$
V_6	$V_{DC}/2$	$-V_{DC}/2$	$V_{DC}/2$	$V_{DC}/6$
V_7	$V_{DC}/2$	$V_{DC}/2$	$V_{DC}/2$	$V_{DC}/2$

not produce a sinusoidal supply to the load, it always generates CMV variations with peak amplitudes that reach up to $\pm V_{DC}/2$. The CMV in a two-level inverter is the average value of the three output voltages generated by the inverter, defined as

$$V_{CM} = \frac{1}{3}\left(V_{AO} + V_{BO} + V_{CO}\right), \tag{7}$$

where V_{AO}, V_{BO}, and V_{CO} are the output voltages of the inverter to the neutral point O of the DC bus.

Table 1 lists the CMV magnitude at various switching states of the inverter. It corresponds to $\pm V_{DC}/6$ in the active-voltage vectors and $\pm V_{DC}/2$ in the zero-voltage vectors. Therefore, in order to reduce the CMV, the zero-voltage vectors need to be suppressed.

However, the CMV for two-level inverters connected in parallel is different from that of a single inverter. In fact, this CMV is the average value of the six output voltages, provided that two inverters are connected in parallel (see Fig. 1):

$$V_{CM} = \frac{1}{6}\left(V_{AO} + V_{BO} + V_{CO} + V_{A'O} + V_{B'O} + V_{C'O}\right), \tag{8}$$

where $V_{A'O}$, $V_{B'O}$, and $V_{C'O}$ are the output voltages of Inverter 2 to the neutral point O of the DC bus, as shown in Fig. 1. Given that the voltage terms for the CMV in (8) can be either positive or negative, V_{CM} can be zero. This is the basis for CMV reduction methods. These methods have been applied [25-29], but at the expense of a decrease in the quality of the grid currents given the elimination of the zero-voltage vectors. On the other hand, this paper proposes a CMV reduction method for inverters connected in parallel that aims to maintain a good quality of these currents, as presented in the following.

4. Proposed CMV Reduction Method

As mentioned above, the conventional CMV reduction methods generally focus on eliminating the zero-voltage vectors. Hence, these methods require additional active-voltage vectors to eliminate and replace the zero-voltage

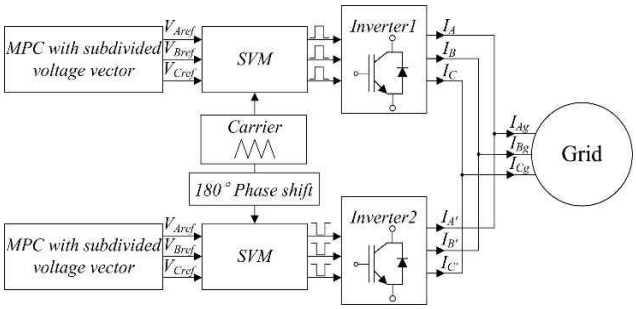

Fig. 5. Block diagram of the proposed CMV reduction method

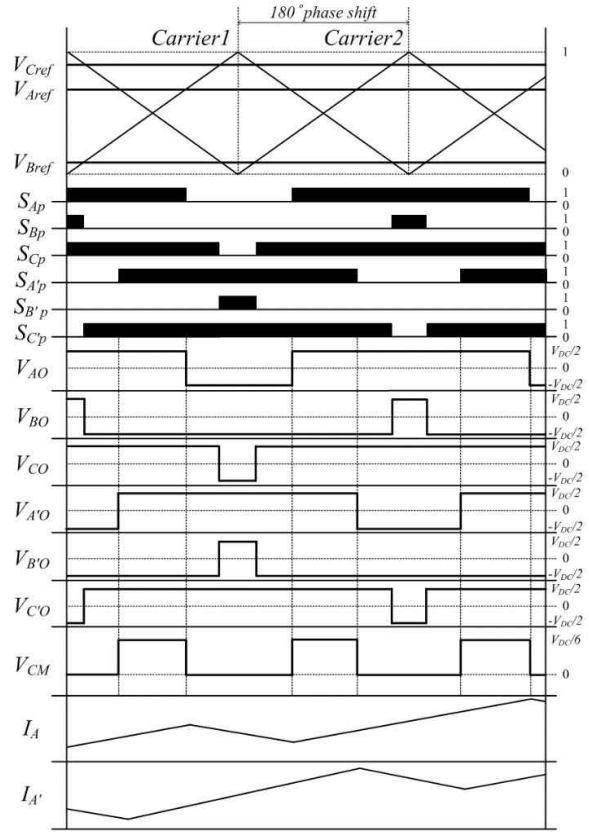

Fig. 6. Comparison of switching signals depending on Carrier 1 and Carrier 2

vectors. Consequently, they increase both the control system complexity and the THD of the grid currents. On the other hand, the proposed CMV reduction method is easy to apply, and it effectively solves the problem of the increased THD if compared to conventional reduction methods based on MPC algorithms.

The conventional MPC algorithm generates one switching state per sampling period. Hence, the carrier wave is not used for inverter switching. The proposed MPC algorithm with subdivided voltage vectors generates a stationary reference frame of d–q axes voltages through the corresponding cost function as shown in Fig. 5.

As mentioned above, the reference voltages of each inverter are obtained by the MPC algorithm with subdivided

voltage vectors, which are compared with the carrier wave of each inverter through a coordinate transformation. Each inverter connected in parallel, which is considered in the proposed MPC algorithm, has individual carrier signals.

Fig. 6 shows the comparison of the switching signals of each inverter. The carriers (i.e., Carrier 1 and Carrier 2) are shifted by 180°, in order to operate with phase difference. The reference voltage vectors (i.e., V_{Aref}, V_{Bref}, and V_{Cref}) are compared to the carriers. Therefore, the switching signals (i.e., $S_{A'p}$, $S_{B'p}$, and $S_{C'p}$) of Carrier 2 are generated with the corresponding phase difference to those (i.e., S_{Ap}, S_{Bp}, and S_{Cp}) of Carrier 1.

The pole voltages (i.e., V_{AO}–$V_{A'O}$, V_{BO}–$V_{B'O}$, and V_{CO}–$V_{C'O}$) of each phase are also generated with a difference of 180° for each inverter. As a result, the CMV (V_{CM}) average value of the pole voltages is reduced by the proposed method. In addition, the grid currents of the inverters have a connected in parallel, the grid currents are the sum of the output currents of each inverter. The switching ripple at the grid side has two times the switching ripple of the output currents in each inverter.

On the other hand, in the proposed reduction method, the switching ripple of Carrier 2 also occurs in a shifted position. Hence, the switching ripple of the grid currents decreases when the currents from the inverters are combined before entering to the grid side. Consequently, our method shows lower switching ripple in the grid currents than conventional CMV reduction methods based on MPC such as the active zero-state PWM (AZSPWM) algorithm [35-37] or methods considering the CMV factor in the cost function [38-40]. However, the proposed method cannot be applied to the conventional MPC algorithm because it performs one switching per sampling period without considering the carrier wave. To overcome this, Fig. 5 shows a block diagram for the implementation of the proposed method, where each inverter is controlled using the MPC algorithm with subdivided voltage vectors, and the carrier waves of the inverters have a phase shift of 180° to reduce the total CMV in the system.

5. Simulation Results

In order to demonstrate the operation of the proposed CMV reduction method in a system composed of two parallel-connected two-level inverters, we performed a simulation using the PSIM software. The simulation parameters are listed in Table 2. We compared the proposed method with two other methods, namely, the convectional MPC algorithm with the CMV factor in the cost function and the AZSPWM algorithm.

Table 2. Simulation parameters

Parameter	Value
DC-link voltage	300 V
Grid phase voltage	90 V_{rms}
Control period	100 μs
Switching frequency	10 kHz
Fundamental frequency	60 Hz
Filter resistance R	0.1 Ω
Filter inductance L	10 mH

Fig. 7 shows the simulation results for the conventional MPC algorithm using the CMV factor in the cost function. Fig. 7(a) and Fig. 7(b) show the grid currents (i.e., I_{Ag}, I_{Bg}, and I_{Cg}) and CMV of the total system. The reference q-axis currents of each inverter are controlled to a peak of 10 A.

The output-phase currents of each inverter are combined prior to their injection into the grid side. V_{CM} is reduced by adding the CMV factor in the cost function of the algorithm after 0.3 s. In this case, V_{CM} is reduced from $2V_{DC}/3$ to $V_{DC}/3$. However, the THD of the grid currents increases from 8.7% to 12.1%, as seen in Fig. 7(a), because active-voltage vectors are used with exception of the zero-voltage vectors, given the CMV factor in the cost function.

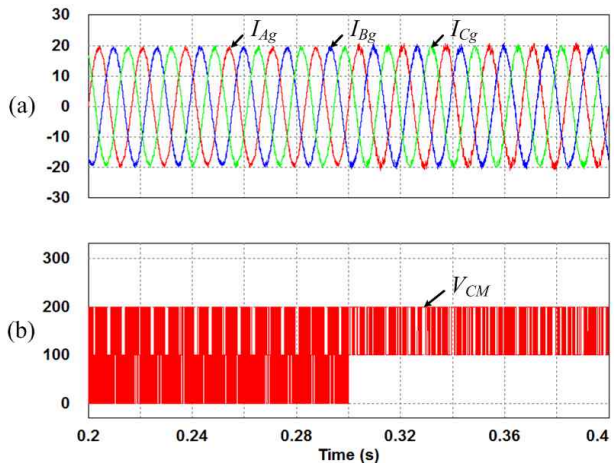

Fig. 7. Simulation results of CMV reduction using MPC with CMV factor in the cost function: (a) grid currents and (b) CMV

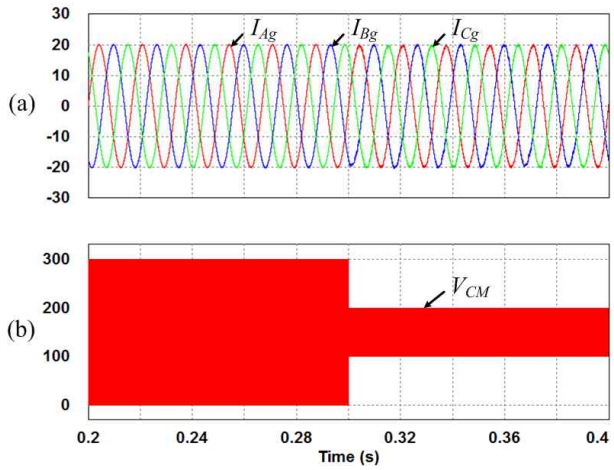

Fig. 8. Simulation results of CMV reduction using AZSPWM for MPC with subdivided voltage vectors: (a) grid currents and (b) CMV

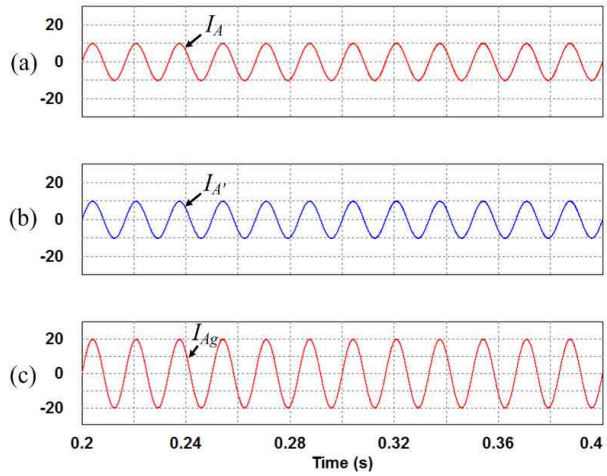

Fig. 9. Simulation results of the proposed CMV reduction method using MPC with subdivided voltage vectors: (a) output current of Inverter 1, (b) output current of Inverter 2, and (c) grid current

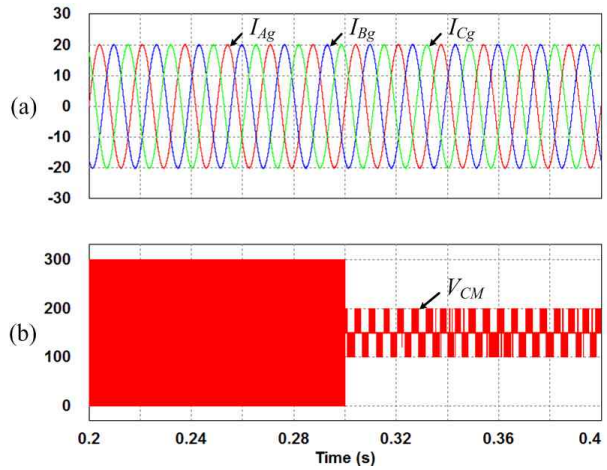

Fig. 10. Simulation results of the proposed CMV reduction method using MPC with subdivided voltage vectors: (a) grid currents and (b) CMV

Fig. 8 shows the simulation results of the CMV reduction using the MPC algorithm with subdivided voltage vectors. After 0.3 s, the AZSPWM algorithm is applied. In this case, an algorithm to improve the THD is used, and the magnitude of V_{CM} is reduced from V_{DC} to $V_{DC}/3$. However, the THD of the grid currents increases from 4.4% to 5.9% because the active-voltage vectors are used instead of the zero-voltage vectors.

Fig. 9 and Fig. 10 show the simulation results of the proposed CMV reduction method for the two inverters connected in parallel. The MPC algorithm with subdivided voltage vectors was used for control. The reference q-axis currents of both of inverters are controlled to a peak of 10 A, as shown in Fig. 9(a) and Fig. 9(b), and the resulting grid currents reach a peak of 20 A, as shown in Fig. 9(c). Carrier 2 has a 180° phase difference with respect to

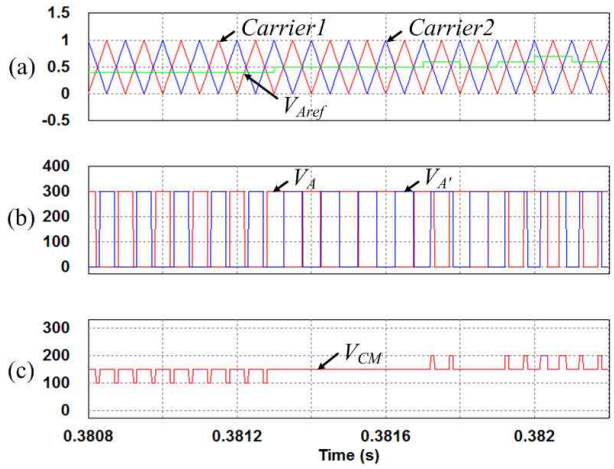

Fig. 11. Simulation results to analyze the proposed method: (a) comparison of carriers and reference voltage, (b) pole voltages of phases A and A', and (c) CMV

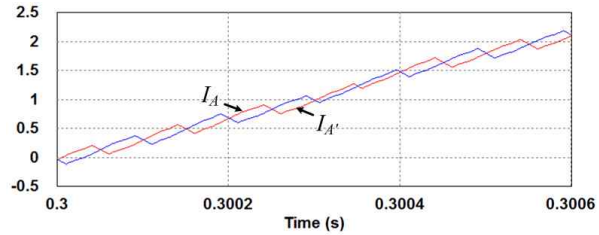

Fig. 12. Simulation results of the output currents for each inverter

Carrier 1 after 0.3 s. V_{AO}–$V_{A'O}$, V_{BO}–$V_{B'O}$, and V_{CO}–$V_{C'O}$ corresponding to each phase are generated with a 180° difference among them as well. This results in a V_{CM} reduction from V_{DC} to $V_{DC}/3$, as shown in Fig. 10(b). In addition, the grid currents show lower switching ripples than those obtained with the other methods. The THD of the grid currents decreases from 4.4% to 3.1%.

Fig. 11 shows simulation results to analyze the proposed CMV reduction method. Fig. 11(a) shows the two carriers (i.e., Carrier 1 and Carrier 2) corresponding to each inverter and the reference voltage of phase A (V_{Aref}). Fig. 11(b) shows the pole voltages of phases A and A' (i.e., V_A and $V_{A'}$) according to Carrier 1 and Carrier 2. Fig. 11(c) shows the V_{CM} of the system with the 180° phase difference. Both V_A and $V_{A'}$, respectively related to Carrier 2 and Carrier 1, operate with a phase difference of 180° between them.

Fig. 12 shows the output currents of each inverter after 0.3 s. Through the proposed reduction method, the switching ripples are also generated with a 180° phase difference. Therefore, the grid currents that correspond to the sum of the output currents of each inverter show lower switching ripples than the cases where our method is not applied.

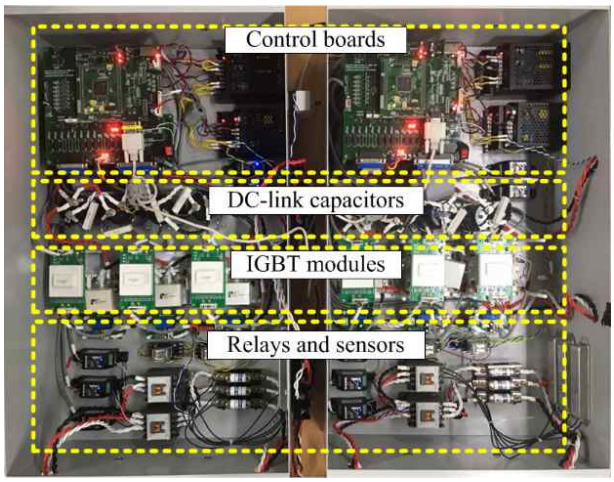

Fig. 13. Experimental setup

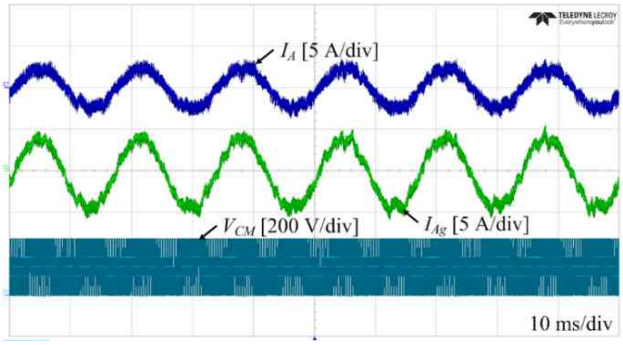

Fig. 14. Experimental results for the parallel inverters operation without using the proposed method

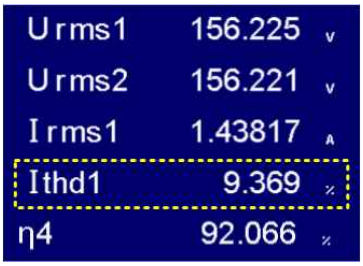

Fig. 15. THD analysis of the grid currents and the efficiency for the inverters connected in parallel without using the proposed method

6. Experimental Results

Besides simulations, we also conducted experiments to verify the proposed CMV reduction method. Fig. 13 shows the circuit used in the experiments to connect two inverters in parallel.

The circuit is composed of two control boards, DC-link capacitors, and two-level IGBT modules. The control boards

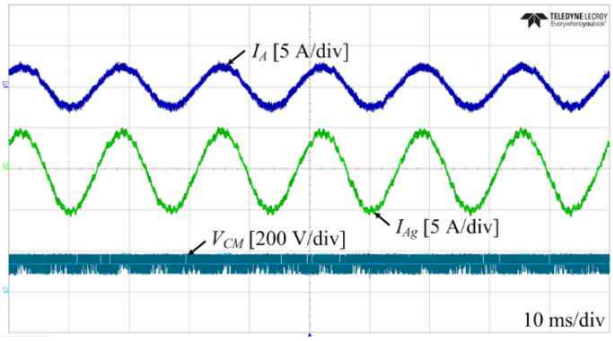

Fig. 16. Experimental results for the parallel inverters operation using the proposed method

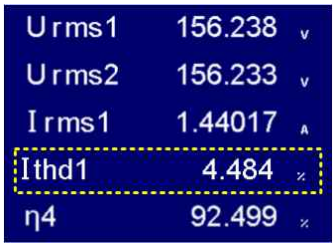

Fig. 17. THD analysis of the grid current and the efficiency for the inverters connected in parallel using the proposed method

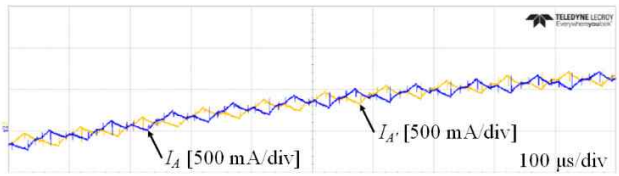

Fig. 18. Experimental results of the output currents for each inverter

are based on DSP controllers (TMS320F28335) from Texas Instruments. The experimental setup parameters are also those used for the simulation and listed in Table 2. A CAN is used for communication between Inverter 1 and Inverter 2.

Fig. 14 shows the experimental results for the parallel inverters operation without using the proposed method. The MPC algorithm with subdivided voltage vectors is used as control algorithm. The phase current (I_A) of Inverter 1 was controlled to a peak of 2 A; hence, the grid current (I_{Ag}) reached a peak of 4 A. The V_{CM} variation ranged from 0 V to 300 V.

Fig. 15 shows the THD analysis of the grid currents and the efficiency for the inverters connected in parallel. The THD in the grid current of phase A (I_{thd1}) reached 9.369% without using the proposed CMV reduction method. Additionally, the efficiency (η_4) of the inverters connected in parallel is 92.066%.

Fig. 16 shows the experimental results for the parallel

inverters operation using the proposed CMV reduction method and MPC with subdivided voltage vectors as the control algorithm. The reference q-axis currents of both inverters were controlled to a peak of 2 A, and the corresponding IAg reached a peak of 4 A. The phase difference between carrier signals resulted in a decrease of V_{CM} variation from V_{DC} to $V_{DC}/3$, with values ranging from 100 V to 200 V.

Fig. 17 shows the THD analysis of the grid currents and the efficiency for the inverters connected in parallel when applying our proposed CMV reduction method. The THD in the grid current of phase A (I_{thd1}) reached 4.484%. Additionally, the efficiency (η_4) of the inverters connected in parallel is 92.499%. Consequently, these grid currents showed lower switching ripples than those without using the proposed method, and the THD decreased from 9.369% to 4.484%.

Finally, Fig. 18 shows the experimental results of the output currents for each inverter. As shown in Fig. 12, the switching ripples are generated with a 180° phase difference by the proposed reduction method.

7. Conclusion

In this paper, the reduction method for the CMV in parallel-connected inverters using the MPC algorithm with subdivided voltage vectors is proposed. In the ESS, the MPC algorithm can be used to control the grid currents instead of the PI controller. The conventional MPC algorithm increases the THD of the grid currents because it generates one switching state per sampling period. Therefore, in this paper, the MPC algorithm with the subdivided voltage vectors is used for the quality improvement and the THD reduction of the grid currents. However, in the proposed MPC algorithm with subdivided voltage vectors, the CMV is increased due to the zero-voltage vectors. Therefore, we proposed a CMV reduction method using the phase difference among carrier signals. The proposed method not only reduces the CMV but also the THD of the grid currents. In other words, in order to achieve the technical results such as the reduction of both the CMV and the THD of the grid currents in the parallel-connected inverters, the phase difference among the carrier signals is most important compared with the MPC and subdivided voltage vectors. Additionally, the subdivided voltage vectors are required to reduce the THD of the grid currents. In this paper, the phase difference among carrier signals and the subdivided voltage vectors should be integrated to achieve the CMV reduction additionally as well as the THD reduction of the grid currents in the parallel-connected inverters. In the tested system with two inverters, the phase difference was 180° between the carriers for state switching. The proposed method successfully reduced the CMV variation from V_{DC} to $V_{DC}/3$. In addition, the switching ripples of the grid currents were reduced along with the corresponding THD of the grid currents. Moreover, this method can improve the system durability and we verified its ease of implementation. The validity of the proposed method was verified by both simulation and experimental results, outperforming similar methods.

Acknowledgements

This work was supported by the Korea Institute of Energy Technology Evaluation and Planning (KETEP) and the Ministry of Trade, Industry & Energy (MOTIE) of the Republic of Korea (No. 20171210201100) and the grant (No.20172020108970) from the Korea Institute of Energy Technology Evaluation and Planning (KETEP) that was funded by the Ministry of Trade, Industry and Energy (MOTIE).

References

[1] J.-S. Lee and K.-B. Lee, "New Modulation Techniques for a Leakage Current Reduction and a Neutral-Point Voltage Balance in Transformerless Photovoltaic Systems Using a Three-Level Inverter," *IEEE Trans. Power Electron*., vol. 29, no. 4, pp. 1720-1732, Apr. 2014.

[2] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Trans. Ind. Electron*., vol. 53, no. 5, pp. 1398-1409, Oct. 2006.

[3] S.-W. Hyun, S.-J. Hong, J.-H. Lee, C.-B. Lee, and C.-Y. Won, "A Method to Compensate the Distorted Space Vectors in the Unbalanced Neutral Point Voltage of 3-level NPC PWM Inverters," *Journal of Power Electronics*, vol. 16, no. 2, pp. 455-463, Mar. 2016.

[4] U.-M. Choi and K.-B. Lee, "Neutral-Point Voltage Balancing Method for Three-Level Inverter Systems with a Time-Offset Estimation Scheme," *Journal of Power Electronics*, vol. 13, no. 2, pp. 243-249, Mar. 2013.

[5] J.-S. Lee and K.-B. Lee, "Tolerance Control for the Inner Open-Switch Faults of a T-Type Three-Level Rectifier," *Journal of Power Electronics*, vol. 14, no. 6, pp. 1157-1165, Nov. 2014.

[6] J.-S. Park and F.-S. Kang, "Five-Level PWM Inverter Using Series and Parallel Alternative Connection of Batteries," *Journal of Electrical Engineering & Technology*, vol. 12, no. 2, pp. 701-710, Mar. 2017.

[7] S.-C. Shin, H.-J. Lee, Y.-H. Kim, J.-H. Lee, T. K. Lee, and C.-Y. Won, "Power Control Method for Reducing Circulating Current in Parallel Operation of DC Distribution System," *Journal of Electrical*

Engineering & Technology, vol. 8, no. 5, pp. 1212-1220, Sep. 2013.

[8] Z. Guowei, W. Tongzhen, H. Shengli, and K. Lingzhi, "The Control for Grid Connected Inverter of Distributed Generation under Unbalanced Grid Voltage," *in Proc. SUPERGEN Conf*., pp. 1-5, 2009.

[9] J.-S. Lee and K.-B. Lee, "Time-Offset Injection Method for Neutral-Point AC Ripple Voltage Reduction in a Three-Level Inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1931-1941, Mar. 2016.

[10] M.-G. Jeong, H. U. Shin, J.-W. Baek, and K.-B. Lee, "An Interleaving Scheme for DC-link Current Ripple Reduction in Parallel-Connected Generator Systems," *Journal of Power Electronics*, vol. 17, no. 4, pp. 1004-1013, Jul. 2017.

[11] J.-K. Kim, J.-H. Lee, H.-G. Jeong, and K.-B. Lee, "Improvement of Grid-Connected Inverter Systems with PR Controllers under the Unbalanced and Distorted Grid Voltage," *in Proc. IPEMC Conf.*, pp. 1183-1187, 2012.

[12] Y. Zhang, J. Liu, and C. Zhang, "Comparison of Traditional Two-Stage Buck-Boost Voltage Source Inverter and Diode-Assisted Buck-Boost Voltage Source Inverter," *in Proc. APEC Conf.*, pp. 141-148, 2012.

[13] W. J. Choi, E. Lee, and K.-B. Lee, "A Novel MPC-SVM Strategy for Direct Torque Flux Control of an Induction Motor Drive System Using a Matrix Converter," *in Proc. ICIT Conf.*, pp, 181-186. 2014.

[14] J.-C. Park, C.-B. Park, J.-H. Baek, and S.-S. Kwak, "Optimal Zero Vector Selecting Method to Reduce Switching Loss on Model Predictive Control of VSI," *The Trans. Korean Institute of Power Electron.*, vol. 20, no. 3, pp. 273-279, Jun. 2015.

[15] R. Sultana and S. K. Sahoo, "Finite Control Set Model Predictive Current Control for a Cascaded Multilevel Inverter," *Journal of Electrical Engineering & Technology,* vol. 11, no. 6, pp. 1674-1683, Nov. 2016.

[16] I.-G. Kim and S.-S. Kwak, "An Algorithm for Even Distribution of Loss, Switching Frequency, Power of Model Predictive Control Based Cascaded H-bridge Multilevel Converter," *The Trans. Korean Institute of Power Electron.*, vol. 20, no. 5, pp. 448-455, Oct. 2015.

[17] Y. Cho and K.-B. Lee, "Virtual-Flux-Based Predictive Direct Power Control of Three-Phase PWM Rectifiers With Fast Dynamic Response," *IEEE Trans. Power Electron*., vol. 31, no. 4, pp. 3348-3359, Apr. 2016.

[18] J.-S. Lee and K.-B. Lee, "Predictive Control of Vienna Rectifiers for PMSG Systems," *IEEE Trans. Ind. Electron*., vol. 64, no. 4, pp. 2580-2591, Apr. 2017.

[19] A. A. Ahmed, B. K. Koh, H. S. Park, K.-B. Lee, and Y. I. Lee, "Finite-Control Set Model Predictive Control Method for Torque Control of Induction Motors Using a State Tracking Cost Index," *IEEE Trans. Ind. Electron*., vol. 64, no. 3, pp. 1916-1928, Mar. 2017.

[20] Z. Gong, P. Dai, X. Wu, F. Deng, D. Liu, and Z. Chen, "A Hierarchical Model Predictive Voltage Control for NPC/H-Bridge Converters with a Reduced Computational Burden," *Journal of Power Electronics*, vol. 17, no. 1, pp. 136-148, Jan. 2017.

[21] B. Feng and H. Lin, "Finite Control Set Model Predictive Control of AC/DC Matrix Converter for Grid-Connected Battery Energy Storage Application," *Journal of Power Electronics*, vol. 15, no. 4, pp. 1006-1017, Jul. 2015.

[22] H.-C. Moon, J.-S. Lee, J.-H. Lee, and K.-B. Lee, "Space Vector Modulation based on Model Predictive Control to Reduce Current Ripples with Subdivided Space Voltage Vectors," *The Trans. Korean Institute of Power Electron.*, vol. 22, no. 1, pp. 18-26, Feb. 2017.

[23] H.-C. Moon, J.-S. Lee, J.-H. Lee, and K.-B. Lee, "Model Predictive Control of a Grid-Connected Inverter to Reduce Current Ripples and Computation Loads," *in Proc. APEC Conf.*, pp. 1097-1102, 2017.

[24] Y.-M. Yang, H.-M. Peng, and Q.-D. Wang, "Common Model EMI Prediction in Motor Drive System for Electric Vehicle Application," *Journal of Electrical Engineering & Technology,* vol. 10, no. 1, pp. 205-215, Jan. 2015.

[25] K.-S. Ahn, N.-S. Choi, E.-C. Lee, and H.-J. Kim, "A Study on a Carrier Based PWM having Constant Common Mode Voltage and Minimized Switching Frequency in Three-Level Inverter," *Journal of Electrical Engineering & Technology*, vol. 11, no. 2, pp. 393-404, Mar. 2016.

[26] S. Kahng, J. Lee, K.-T. Kim, and H.-S. Kim, "Metamaterial CRLH Structure-based Balun for Common-Mode Current Indicator," *Journal of Electrical Engineering & Technology*, vol. 9, no. 1, pp. 301-306, Jan. 2014.

[27] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich, "Impact of Interleaving on AC Passive Components of Paralleled Three-Phase Voltage-Source Converters," *IEEE Trans. Ind. Appl*., vol. 46, no. 3, pp. 1042-1054, May/Jun. 2010.

[28] Y.-S. Lai, P.-S. Chen, H.-K. Lee, and J. Chou, "Optimal Common-Mode Voltage Reduction PWM Technique for Inverter Control With Consideration of the Dead-Time Effects — Part II: Applications to IM Drives With Diode Front End," *IEEE Trans. Ind. Appl*., vol. 40, no. 6, pp. 1613-1620, Nov./Dec. 2004.

[29] J.-W. Shin, H. Shin, G.-S. Seo, J.-I. Ha, and B.-H. Cho, "Low-Common Mode Voltage H-Bridge Converter with Additional Switch Legs," *IEEE Trans. Power Electron*., vol. 28, no. 4, pp. 1773-1782, Apr. 2013.

[30] M. M. Renge and H. M. Suryawanshi, "Multilevel Inverter to Reduce Common Mode Voltage in AC

Motor Drives Using SPWM Technique," *Journal of Power Electronics*, vol. 11, no. 1, pp. 21-27, Jan. 2011.
[31] J. Rodriquez, J. Pontt, C. A. Silva, P. Correa, P. Lezana, P. Cortes, and U. Ammann, "Predictive Current Control of a Voltage Source Inverter," *IEEE Trans. Ind. Electron*., vol. 54, no. 1, pp. 495-503, Feb. 2007.
[32] G. Du, Z. Liu, F. Du, and J. Li, "Performance Improvement of Model Predictive Control Using Control Error Compensation for Power Electronic Converters Based on the Lyapunov Function," *Journal of Power Electronics*, vol. 17, no. 4, pp. 983-990, Jul. 2017.
[33] A. Bakeer, M. A. Ismeil, and M. Orabi, "Modified Finite Control Set-Model Predictive Controller (MFCS-MPC) for quasi Z-Source Inverters based on a Current Observer," *Journal of Power Electronics*, vol. 17, no. 3, pp. 610-620, May 2017.
[34] Y. Wang, X. Wang, W. Xie, F. Wang, M. Dou, R. M. Kennel, R. D. Lorenz, and D. Gerling, "Deadbeat Model-Predictive Torque Control With Discrete Space-Vector Modulation for PMSM Drives," *IEEE Trans. Ind. Electron*., vol. 64, no. 5, pp. 3537-3547, May 2017.
[35] S. M. Ali, V. V. Reddy, and M. S. Kalavathi, "Simplified Active Zero State PWM Algorithms for Vector Controlled Induction Motor Drives for Reduced Common Mode Voltage," *in Proc. ICRAIE Conf.*, pp. 1-7, 2014.
[36] Y.-S. Lai and F.-S. Shyu, "Optimal Common-Mode Voltage Reduction PWM Technique for Inverter Control With Consideration of the Dead-Time Effects — Part I: Basic Development," *IEEE Trans. Ind. Appl*., vol. 40, no. 6, pp. 1605-1612, Nov./Dec. 2004.
[37] R. M. Tallam, R. J. Kerkman, D. Leggate, and R. A. Lukaszewski, "Common-Mode Voltage Reduction PWM Algorithm for AC Drives," *IEEE Trans. Ind. Appl*., vol. 46, no. 5, pp. 1959-1969, Sep./Oct. 2010.
[38] M. J. Duran, J. A. Riveros, F. Barrero, H. Guzman, and J. Prieto, "Reduction of Common-Mode Voltage in Five-Phase Induction Motor Drives Using Predictive Control Techniques," *IEEE Trans. Ind. Appl*., vol. 48, no. 6, pp. 2059-2067, Nov./Dec. 2012.
[39] R. Vargas, U. Ammann, J. Rodriguez, and J. Pontt, "Predictive Strategy to Control Common-Mode Voltage in Loads Fed by Matrix Converters," *IEEE Trans. Ind. Electron*., vol. 55, no. 12, pp. 4372-4380, Dec. 2008.
[40] P. Cortes, S. Kouro, B. L. Rocca, R. Vargas, J. Rodriguez, J. I. Leon, S. Vazquez, and L. G. Franquelo, "Guidelines for Weighting Factors Design in Model Predictive Control of Power Converters and Drives," *in Proc. ICIT Conf.*, pp. 1-7, 2009.

Joon Young Park He received the B.S. degree in Manufacturing Engineering from Kyungpook National University, Daegu, Korea, in 1998. He received the M.S. degree in Mechanical Manufacturing Engineering from Korea Polytechnic University, Incheon, Korea, in 2014. He is currently working toward his Ph.D. degree in Electrical and Computer Engineering at Ajou University, Suwon, Korea. His research interests include power conversion and grid-connected systems.

Jiook Sin He received the B.S. degree in Electronic Engineering from Keimyung University, Daegu, Korea, in 2015. He received the M.S. degree in Electrical and Computer Engineering from Ajou University, Suwon, Korea, in 2017. Since 2017, he has been with the LS mecapion, Daegu, Korea. His research interests include grid-connected systems and motor drives.

Yeongsu Bak He received the B.S. and M.S. degrees in Electrical and Computer Engineering from Ajou University, Suwon, Korea, in 2014 and 2016, respectively. He is currently working toward his Ph.D. degree in Electrical and Computer Engineering at Ajou University, Suwon, Korea. His research interests include grid-connected systems and matrix converter.

Sung-Min Park He received the B.S. degree in Electronics Engineering and M.S. degree in Electrical Engineering from Korea University, Seoul, Korea, in 2001 and 2003, respectively. He received the Ph.D. degree from the University of Connecticut, Storrs, CT, USA, in 2015. From 2003 to 2008, he was a Senior Engineer with LG Electronics, Seoul. From 2008 to 2010, he was with Samsung Heavy Industries, Suwon. From 2014 to 2015, he was a Senior Research Engineer at the United Technologies Research Center (UTRC), East Hartford, CT, USA. Since 2015, he has been an Assistant Professor in the Department of Electronic and Electrical Engineering, Sejong, Hongik University. His research interests include power electronics applications for home appliances and renewable energy systems.

Kyo-Beum Lee He received the B.S. and M.S. degrees in Electrical and Electronic Engineering from Ajou University, Suwon, Korea, in 1997 and 1999, respectively. He received the Ph.D. degree in Electrical Engineering from Korea University, Seoul, Korea, in 2003. From 2003 to 2006, he was with the Institute of Energy Technology, Aalborg University, Aalborg, Denmark. From 2006 to 2007, he was with the Division of Electronics and Information Engineering, Chonbuk National University, Jeonju, Korea. In 2007, he joined the School of Electrical and Computer Engineering, Ajou University, Suwon, Korea. He is an Associate Editor of the IEEE Transactions on Power Electronics, the Journal & Technology. His current research interests include electric machine drives, renewable power generation, and electric vehicle applications.