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Analysis of Flat-Band-Voltage Dependent Breakdown Voltage for 10 nm Double Gate MOSFET

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Abstract

The existing modeling of avalanche dominated breakdown in double gate MOSFETs (DGMOSFETs) is not relevant for 10 nm gate lengths, because the avalanche mechanism does not occur when the channel length approaches the carrier scattering length. This paper focuses on the punch through mechanism to analyze the breakdown characteristics in 10 nm DGMOSFETs. The analysis is based on an analytical model for the thermionic-emission and tunneling currents, which is based on two-dimensional distributions of the electric potential, obtained from the Poisson equation, and the Wentzel-Kramers-Brillouin (WKB) approximation for the tunneling probability. The analysis shows that corresponding flat-band-voltage for fixed threshold voltage has a significant impact on the breakdown voltage. To investigate ambiguousness of number of dopants in channel, we compared breakdown voltages of high doping and undoped DGMOSFET and show undoped DGMOSFET is more realistic due to simple flat-band-voltage shift. Given that the flat-band-voltage is a process dependent parameter, the new model can be used to quantify the impact of process-parameter fluctuations on the breakdown voltage.

Index Terms: Breakdown voltage, DGMOSFET, Flat band voltage, Oxide thickness

I. INTRODUCTION

To reduce the short channel effects (SCEs) due to significant down scaling of MOSFETs, double gate MOSFETs (DGMOSFETs) are used in sub-10-nm CMOS technology [1]. Many models for various DGMOSFETs have been proposed and used to analyze the transport characteristics [2, 3]. As dimensions shrink into nanometer scales, the reduction of threshold voltage (V_{th}) introduces many problems, such as shrinking of the operation region and a decrease in breakdown voltage [4]. Mohammad et al. [5] have determined the breakdown voltage of DGMOSFET with the channel length of above 50 nm from Fulop's avalanche breakdown condition [6]. Lee et al. [7] analyzed the breakdown voltage due to impact ionization in multi-gate MOSFETs (MuGFETs) with channel lengths above 45 nm. The avalanche breakdown due to impact ionization is an important breakdown mechanism when the channel length is above 45 nm, but avalanche does not occur in the case of ballistic carrier transport in the fully depleted region of 10 nm devices. This is a consequence of the fact that the average scattering length is in the order of 10 nm [8]. Accordingly, the punch-through effect due to the lowering of source-to-drain barrier is the dominant breakdown mechanism in 10 nm DGMOSFETs. The variation of source-to-drain barrier in the channel causes changes in the contributions of thermionic-emission and tunneling currents, which determine the drain current in 10 nm devices. In particular, an abrupt increase of tunneling current due to a reduction of the barrier width can sufficiently increase the drain current to cause device breakdown. How-

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ever, the current increase with drain voltage does not provide an obvious definition for the breakdown voltage. Lee et al. [7] adopted a method to define the breakdown voltage from current–voltage characteristics that is similar to that used to define the threshold voltage. This method is suitable for devices with sufficiently long channels to ignore the tunneling current. However, this method cannot be used to obtain the breakdown voltage due to the punch-through effect. Thus, we define the breakdown voltage as the drain voltage for the drain current of 10^{-7} A in 10 nm DGMOSFETs with equal channel length and width at V_{th} = 0.3 V.

The flat-band-voltage is an important parameter to determine threshold voltage. Flat-band-voltage is constant at fixed threshold voltage even though the flat-band-voltage is a process dependent parameter, which varies due to unintended process fluctuations [9]. We focus on analysis of impact of flat-band-voltage to sustain breakdown voltage of 1.5 V above at threshold voltage of 0.3 V, including the dependence on the silicon thickness and the top/bottom oxide thickness.

There are few doping atoms in the channel in nanoscale DGMOSFET, even when the nominal doping concentration is high. A DGMOSFET with a length, width and silicon thickness of 10 nm only has one dopant to doping concentration of 10^{18}/cm^3. We compare the dependence of flat-band-voltage on breakdown voltages between high doping and undoped channel in this paper.

The model for the drain current of DGMOSFETs having the channel length of 10 nm includes the thermionic-emission and tunneling currents. The electric-potential model proposed by Ding et al. [10] for asymmetric DGMOSFET is used to obtain the thermionic-emission current, whereas Wentzel-Kramers-Brillouin (WKB) approximation is applied to obtain the tunneling current.

This paper is arranged as follows. The potential energy, the thermionic current, and the tunneling current are described in Section II. We present the effects of silicon thickness and flat-band-voltage on the breakdown voltage in Section III and discuss the results in Section IV.

II. THE MODEL SCHEME

Fig. 1 shows the cross-sectional diagram of a DGMOSFET. Because the considered channel length is 10 nm, the thermionic-emission and tunneling currents are considered as the only components of the drain current. The effective top and bottom gate voltages are $V_{gt} - V_{fbt}$ and $V_{gb} - V_{fbb}$, respectively, where V_{fbt} is the top flat-band-voltage and V_{fbb} is the bottom flat-band-voltage. The breakdown voltage is analyzed for $V_{gt} = V_{gb} = 0$ V and $V_{fbt} = V_{fbb}$.

The analysis presented in this paper is based on analytical modeling because the conventional simulation tools average

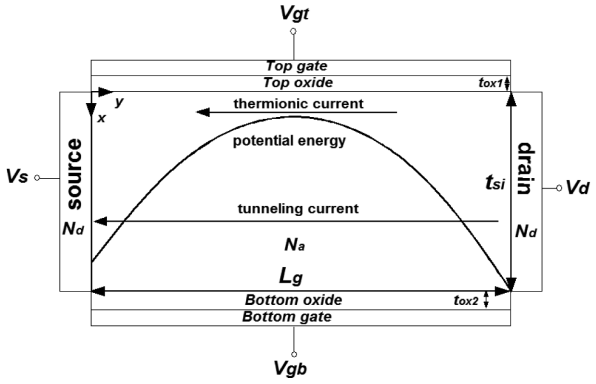

Fig. 1. Schematic diagram of a double gate MOSFET with potential energy and currents.

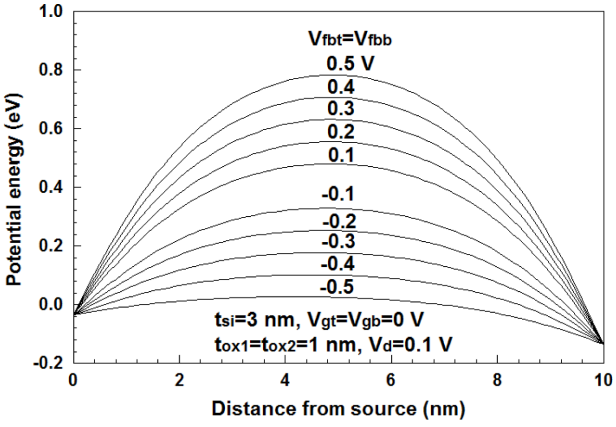

Fig. 2. Potential energy distribution along the y-axis for the increasing flat-band-voltage in an undoped DGMOSFET with L_g = 10 nm.

the effects of carrier concentration to levels that, in the case of channel dimensions used in this paper, can correspond to charge that is much smaller than the unit charge of a single carrier. To obtain the potential-energy distribution, the solution of Poisson's equation presented in [11] is applied to the DGMOSFET.

Fig. 2 shows the potential-energy distributions along y-axis through the conduction path [12] in the undoped channel. Based on the potential-energy distribution, the tunneling current (I_{tunn}) and thermionic-emission current (I_{ther}) can be calculated from the analytical models presented in [11] and [13]. Total drain current (I_{total}) is obtained as the sum of the thermionic-emission and tunneling currents.

It can be seen from Fig. 2 that the flat-band voltages determine the potential energy and, therefore, the drain-to-source current for set values of the gate-oxide and silicon thicknesses. The fact that the flat-band voltages can control the source-to-drain barrier in intrinsic-body DGMOSFET enables proper threshold-voltage design without the need for P-type doping of the silicon body between the source and the drain.

For the analysis presented in this paper, the flat-band voltages $V_{fbt} = V_{fbb}$, the gate-oxide thicknesses $t_{ox1} = t_{ox2}$, and the silicon thickness t_{Si} were always set at values that correspond to the threshold voltage of V_{th} = 0.3 V. The threshold voltage was defined as the intercept between the gate-voltage axis and the extrapolated linear region of the transfer characteristic [14].

III. RESULTS AND DISCUSSIONS

Fig. 3(a) shows the current–voltage characteristics of an intrinsic-body DGMOSFET with $L_g = W$ = 10 nm and $t_{ox1} = t_{ox2}$ = 1 nm. As mentioned in the previous section, the flat-band-voltage value $V_{fbt} = V_{fbb}$ was set so that the threshold voltage is V_{th} = 0.3 V. It can be seen that the current increase with drain voltage does not provide an obvious definition for the breakdown voltage. The method that is used to define the breakdown voltage in devices with long channels [7] cannot be used because of the dominance of the tunneling current. Thus, we define the breakdown voltage as the drain voltage for the drain current of 10^{-7} A in 10 nm DGMOSFETs with equal channel length and width at V_{th} = 0.3 V as shown by the dotted line and circles in Fig. 3(a). The definition is reasonable because the drain current of 10^{-7} A for the channel width of 10 nm corresponds to 10 μA/μm, which is much smaller than the current in saturation. As can be seen, the breakdown voltage decreases with an increase in silicon thickness, dropping below 1 V for silicon thicknesses above 4 nm. The contributions of tunneling currents to the total drain current are shown in Fig. 3(b), with silicon thickness as the parameter. The tunneling current is dominant when the drain voltage increases toward the breakdown voltage and the silicon thickness is below 3 nm. The circles denote the tunneling-current contribution at the breakdown condition. We can see that the tunneling current dominates for the acceptable breakdown voltages above 1.5 V and the corresponding silicon thicknesses below 3 nm.

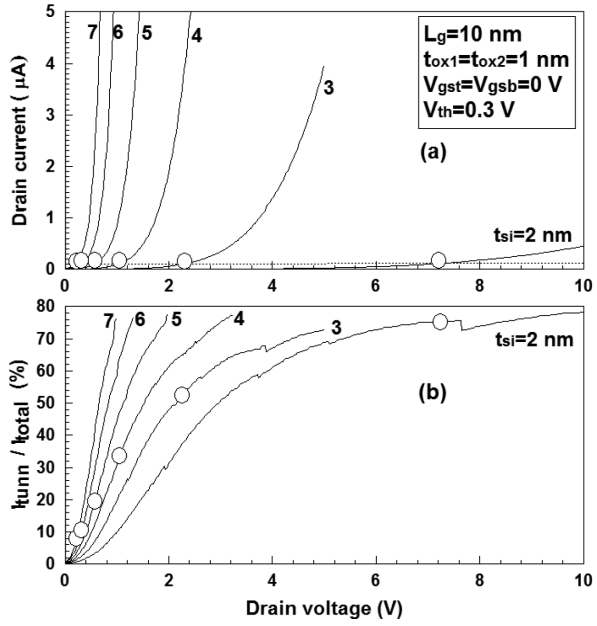

Fig. 3. (a) Drain current–voltage characteristics and (b) contributions of tunneling currents for different silicon thickness of a undoped DGMOSFET with $L_g = W$ = 10 nm, and $t_{ox1} = t_{ox2}$ = 1 nm. Circles show points to denote breakdown.

Fig. 4 shows the breakdown voltage dependence on the flat-band voltage for different silicon thicknesses with $L_g = W$ = 10 nm, and $t_{ox1} = t_{ox2}$ = 1 nm. In Fig. 4, we compare the breakdown voltages for the intrinsic-body DGMOSFETs with the breakdown voltages that could be achieved by the theoretical DGMOSFETs with P-type bodies and uniformly distributed acceptor concentration of 10^{18}/cm^3. The table inside this figure shows the corresponding numbers of acceptor ions. It is obvious from these numbers that the DGMOSFETs with the P-type bodies are practically not possible because the assumed doping concentration at these dimensions corresponds to fewer than 1 doping atom in the P-type body. Fig. 4 also shows that the P-type doping is not necessary, because its effect can be achieved by an increase in the flat-band-voltage in the case of the intrinsic-body DGMOSFETs.

Fig. 5 shows breakdown voltages for different silicon thicknesses and oxide thicknesses of undoped DGMOSFETs with $L_g = W$ =10 nm when threshold voltage is 0.3 V in the case of equal top and bottom oxide thickness. Breakdown voltages decrease with increase of oxide thicknesses under same conditions as shown in Fig. 5.

Breakdown voltages are below 1.5 V except t_{si} = 3 nm in the case of top and bottom oxide thickness of 2 nm as shown in Fig. 5(d), while breakdown voltages is nearly 1.5 V at silicon thickness of 6 nm in the case of top and bottom oxide

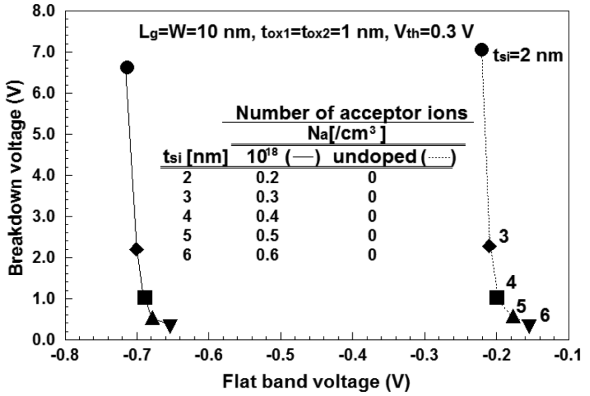

Fig. 4. Breakdown voltages for the intrinsic-body and doped-body DGMOSFETs with $L_g = W$ = 10 nm, $t_{ox1} = t_{ox2}$ = 1 nm and t_{Si} set at values that correspond to V_{th} = 0.3 V.

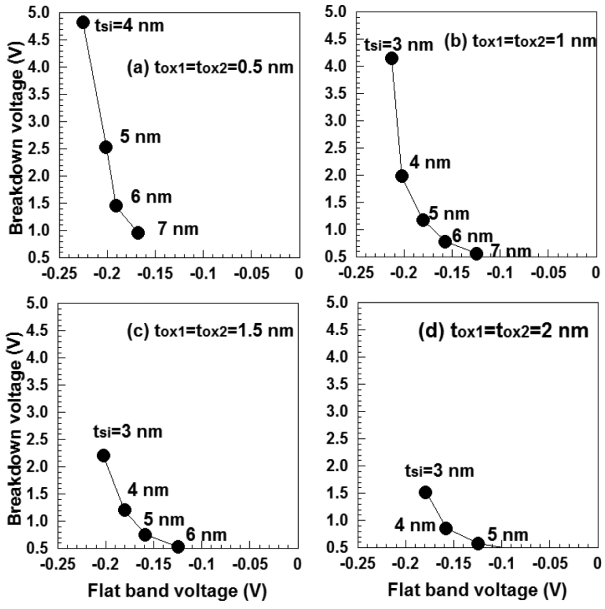

Fig. 5. Breakdown voltages for different silicon thicknesses of undoped DGMOSFETs with L_g = W = 10 nm, and (a) t_{ox1} = t_{ox2} = 0.5 nm, (b) t_{ox1} = t_{ox2} = 1 nm, (c) t_{ox1} = t_{ox2} = 1.5 nm, and (d) t_{ox1} = t_{ox2} = 2 nm when threshold voltage is 0.3 V.

Table 1. Possible silicon thickness to oxide thickness for breakdown voltage above 1.5 V

$t_{ox1} = t_{ox2}$ (nm)	t_{si} (nm)
0.5	<6.0
1.0	<5.5
1.5	<4.5
2.0	<3.0

thickness of 0.5 nm as shown in Fig. 5(a). To sustain breakdown voltage of 1.5 V above, flat-band-voltage has to be below -0.2 V regardless of top and bottom oxide thicknesses. We know that the thinner oxide thickness is, the thicker possible silicon thickness can become, to make a DGMOSFET having breakdown voltage of 1.5 V above at V_{th} = 0.3 V as shown in Table 1.

IV. CONCLUSION

The breakdown voltage in 10-nm DGMOSFETs has been analyzed without the inadequate assumptions of avalanche-dominated breakdown and uniform P-type doping. Based on models for the thermionic-emission and tunneling currents in intrinsic-body DGMOSFETs, it is found that the contribution of the tunneling current is dominant when the breakdown voltage is above 1.5 V. The breakdown voltage is strongly dependent on the silicon and oxide thicknesses. To design a DGMOSFET with acceptable breakdown voltage, thinner oxide thicknesses enable the use of thicker silicon thickness. The quantitative results can be used during the design of 10 nm DGMOSFETs with acceptable breakdown voltages.

This approach of breakdown voltage control by suitable adjustments of the flat-band-voltage can be used, in principle, for DGMOSFETs with channel lengths smaller than 10 nm having reasonable oxide and silicon thickness.

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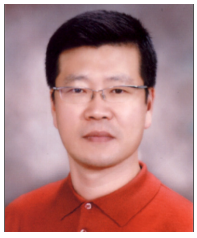

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