JPE 18-2-28

https://doi.org/10.6113/JPE.2018.18.2.640
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Design of a TRIAC Dimmable LED Driver Chip with a Wide Tuning Range and Two-Stage Uniform Dimming

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Abstract

A TRIAC dimmable LED driver with a wide tuning range and a two-stage uniform dimming scheme is proposed in this paper. To solve the restricted dimming range problem caused by the limited conduction ratio of TRIAC dimmers, a conduction ratio compensation technique is introduced, which can increase the output current up to the rated output current when the TRIAC dimmer turns to the maximum conduction ratio. For further optimization, a two-stage uniform dimming diagram with a rapid dimming curve and a slow dimming curve is designed to make the LED driver regulated visually uniform in the whole adjustable range of the TRIAC dimmer. The proposed control chip is fabricated in a TSMC 0.35μm 5V/650V CMOS/LDMOS process, and verified on a 21V/500mA circuit prototype. The test results show that, in the 90V/60Hz~132V/60Hz ac input range, the voltage linear regulation is 2.6%, the power factor is 99.5% and the efficiency is 83%. Moreover, in the dimming mode, the dimming rate is less than 1% when the maximum dimming current is 516mA and the minimum dimming current is only about 5mA.

Key words: Constant output current, LED driver, Wide tuning range, TRIAC dimmer, Two-stage uniform dimming

I. INTRODUCTION

High brightness (HB) LEDs have become increasingly popular in the lighting market since they have higher luminous efficiency, less energy consumption and longer life expectancy than traditional incandescent lamp bulbs [1]-[3]. However, there are various aspects that require attention when it comes to applying LEDs for general lighting. One such aspect is related to the dimming control of HB LEDs, especially the LEDs drivers' compatibility with a TRIAC dimmer, which means the driver should be specially designed to avoid potential issues such as flicker, audible noise, improper dimming function, limited dimming scope etc. [4], [5].

However, the present situation of the technology that allows LED drivers to perform wide range dimming is still imperfect [6]. In [7], an extra dummy load is parallel connected to a TRIAC dimmer, to make the LED match the dimmer. The conduction angle of the TRIAC dimmer ranges from 30° to 150°, and the dimming ratio is about 10%. However, this method is only suitable for the half-bridge topology and the extra dummy load decreases the system efficiency. In [8], an additional CFL ballast circuit is added, so that the current flowing through the LED can be regulated by the conduction angle of the TRIAC dimmer. However, the use of an additional CFL ballast circuit increases the power consumption of the circuit and reduces the system efficiency. In [9], power factor correction was introduced to make the input current track the input voltage. Therefore, the LED drivers can exhibit behavior that is similar to incandescent lamps and be compatible with the TRIAC dimmers. However, since the conduction angle of the TRIAC dimmer is limited, the dimming range of the output current is also limited without any offset. In [10], by introducing a LC input filter and a changing switched capacitor, the power of the LED is controlled by the Triac dimmer and the system has a high linear adjustment rate. However, in the dimming process, the minimum power of the LED load is only about 20~30% of the maximum power, and the dimming range is narrow. Therefore, it is necessary to research the compatibility of the

Manuscript received Feb. 15, 2017; accepted Jul. 15, 2017
Recommended for publication by Associate Editor Chun-An Cheng.
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dimming controller and the TRIAC dimmer to expand the scope of the dimming.

On the other hand, it has been extensively studied on how to achieve satisfactory light since the quality and correlated color temperature (CCT) of light has an impact on human comfort and productivity. In [11], a control method based on an estimator of the luminous flux emitted by a LED is proposed to obtain the enhanced full linear dimming control of the device. In [12], a scheme for controlling the luminosity and CCT of a bi-color LED lamp by utilizing closed-loop control with feedback from a color sensor is presented. The study in [13] is primarily targeted at achieving accurate dimming and CCT control of bi-color variable CCT LED lamps, through the use of a nonlinear empirical LED model that accounts for the thermal interdependence of the two color sources and the actual imperfections of LEDs. All of these studies aim at improving the comfort of human eyes when exposed to light.

There is a difference between actual brightness and observed brightness. This difference leads to the fact that the sensitivity of an eye to changes in brightness is affected by the initial brightness value. For example, in the process of changing from dark to bright, if the actual brightness increases linearly, the observed brightness increases quickly at first, but very slowly later. Based on the above characteristics of the human eye, uniform dimming is another important performance characteristic for a high quality light source.

Up to now, no published work claims to achieve a wide dimming ratio and uniform dimming at the same time. A novel dimming control circuit is proposed in this paper. By introducing conduction compensation technology, the dimming current rises to the rated current when the conduction angle reaches the maximum and declines nearly to zero when the conduction angle reaches the minimum. Consequently, the output current is no longer restricted by the limited conduction angle, and the dimming range can be greatly enlarged. Meanwhile, since eyes are insensitive to large current LED lighting and sensitive to small current LED lighting, the two-stage uniform dimming design is proposed based on a previous design. Namely, a two-stage dimming curve consisting of rapid and slow dimming curves is designed to make the LED brightness vary fairly uniformly with the conduction angle. The detailed operation principle for the proposed dimming circuit is illustrated in Section II. Then, design considerations of the key circuits are presented in Section III. Section IV shows some experimental results, while Section V concludes the paper.

II. Operation Principle

A. System Overview

A system diagram of the proposed wide tuning range and two-stage uniform dimming AC-DC LED driver is shown in Fig. 1. It consists of a bridge rectifier BD, TRIAC dimmer, primary-side sense resistor R_{CS}, RCD snubber circuit, freewheel diode D_o, output capacitor C_o, power MOSFET M_1 and the control IC. The control IC is mainly composed of an I_{out} estimation circuit, constant current (CC) module, power factor correction (PFC) module and the proposed dimming control circuit. A conduction ratio detection circuit (CRDC), conduction ratio compensation circuit (CRCC) and pull-down current control circuit (PCCC) form the proposed dimming control circuit, which can guarantee an output current constant with a wide tuning range. With two-stage dimming optimization, the proposed dimming control circuit is developed and the output current shows two-stage uniform dimming characteristics.

In the control IC, as shown in Fig. 1, the I_{out} estimation circuit samples the voltage of the primary-side sense resistor and exports V_{CAL}, which indicates output current value. Meanwhile, V_{CAL} is processed in the CC to make the output current constant. I_{pull} is achieved from the proposed dimming control circuit. V_{COMP} is obtained from the CC, which disposes of the pull-down current. The PFC module manages V_{COMP} and FB from the auxiliary winding. The driving signal DRV, and the signal T_{ON} and T_{OFF} can be acquired in the normal condition. In order to regulate the output current by the TRIAC, the proposed dimming control circuit generates a pull-down current controlled by the TRIAC dimmer to the CC. As a result, the output current can be regulated by the TRIAC dimmer. The detail principle of the constant current and the dimming are explained below.

B. Principle of Constant Current

The proposed controller operates in the boundary conduction mode (BCM) and the output current is estimated by the I_{out} estimation block. Steady state waveforms of the sensed primary-side signals for the output current estimation are shown in Fig. 2. According to Fig. 1, DRV is the driving voltage of the power MOSFET M_1. When the DRV is a high voltage, the power MOSFET is switch-ON and this period is called T_{ON}. Similarly, T_{OFF} is the switch-OFF period during a switching cycle. I_P is the primary-side instantaneous current. I_S is the secondary-side instantaneous current.

When the system works in the stable state, the output current can be expressed as Eq (1).

$$I_{OUT} = \frac{1}{2} \cdot \frac{I_{SP} \cdot T_{OFF}}{T_{ON} + T_{OFF}} \tag{1}$$

In Eq (1), I_{OUT} is the output current, and I_{SP} is the peak current of the secondary-side instantaneous current in a switching cycle. T_{ON} and T_{OFF} are the turn-on time and turn-off time, respectively.

V_{CS} is the sensing voltage of the primary-side sense resistor. V_{CAL} is the output of the I_{OUT} estimation module, which calculates V_{CS} with T_{ON} and T_{OFF}. Therefore, V_{CAL} can be

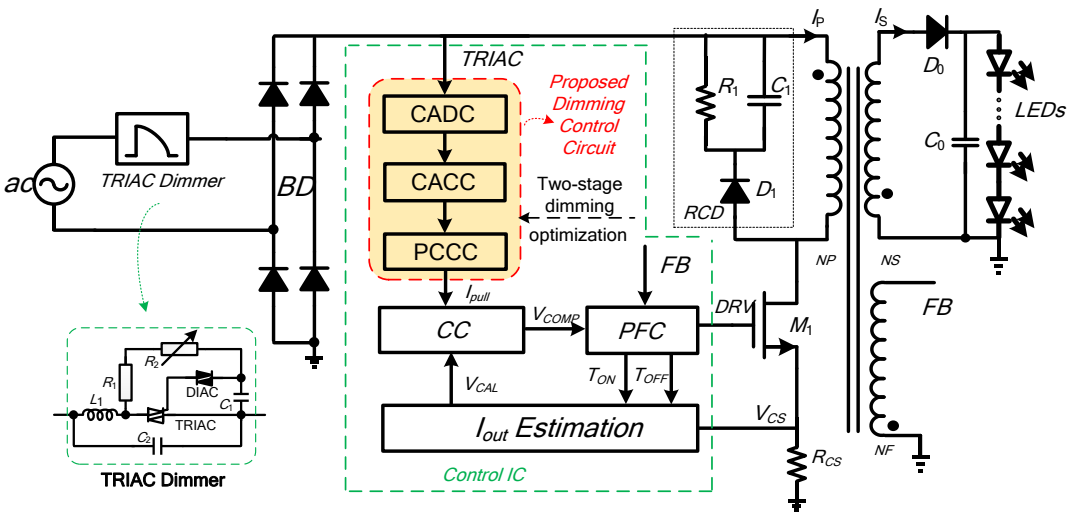


Fig. 1. System diagram of the proposed circuit.

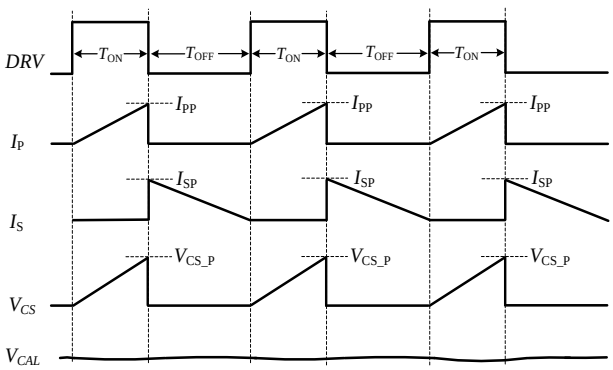


Fig. 2. Key operation principle waveforms of the proposed circuit.

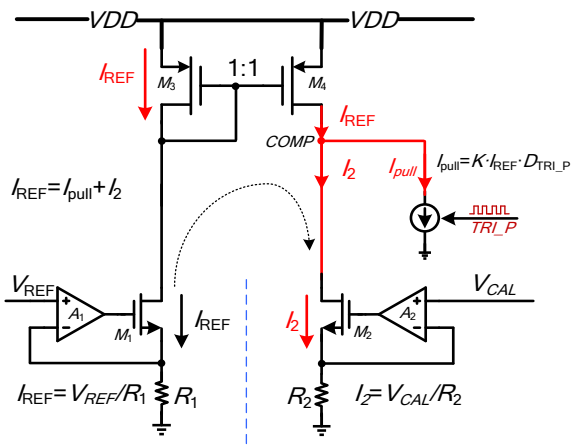


Fig. 3. Constant current control circuit.

obtained by Eq (2).

$$V_{CAL}=\frac{V_{CS\_P}\cdot T_{OFF}}{T_{ON}+T_{OFF}} \tag{2}$$

According to the relationship of the transformer ampere-turns, there is:

$$I_{SP}=\frac{N_P}{N_S}\cdot I_{PP}=\frac{N_P}{N_S}\cdot\frac{V_{CS\_P}}{R_{CS}} \tag{3}$$

Where, N_P and N_S are the turns of the primary-side winding and secondary-side winding, respectively. I_{PP} and V_{CS_P} denote the peak value of I_P and V_{CS}. R_{CS} is the value of the primary-side sense resistor. The average output current I_{OUT} can be given as:

$$I_{OUT}=\frac{1}{2}\cdot\frac{N_P}{N_S}\cdot\frac{V_{CAL}}{R_{CS}} \tag{4}$$

In Eq (4), the output current I_{OUT} is determined by N_P, N_S, R_{CS} and V_{CAL}.

Fig. 3 shows the constant current control circuit. The amplifier, NMOS and resistor comprise the voltage-to-current converter. Therefore, the current I_{REF} and I_2 are converted by the reference voltage V_{REF} and the estimated output current signal V_{CAL}, respectively. COMP is connected to the external compensation capacitance, and the current I_2, I_{REF} and I_{pull} meet Kirchhoff's current law.

$$I_{REF}=I_2+I_{pull}=\frac{V_{CAL}}{R_2}+I_{pull} \tag{5}$$

In Eq (5), I_{REF} is the reference current, I_2 is converted by V_{CAL}, and V_{CAL} comes from the I_{OUT} estimation circuit. R_2 is the converted resistor, and I_{pull} is the pull-down current from the proposed dimming control circuit.

In according to Eq (4) and (5), the output current I_{OUT} can be derived as:

$$I_{OUT}=\frac{1}{2}\cdot\frac{N_S}{N_P}\cdot\frac{R_2}{R_{CS}}\cdot(I_{REF}-I_{pull}) \tag{6}$$

In Eq (6), R_{CS} is the primary-side sense resistor. Eq (6) shows that I_{OUT} varies with I_{pull}, which is controlled by the conduction angle of the TRIAC dimmer. Therefore, I_{OUT} can be regulated by the conduction angle. In addition, I_{OUT} is kept constant when the conduction angle is fixed. The rated output current I_{RC} is an output current without a TRIAC dimmer and

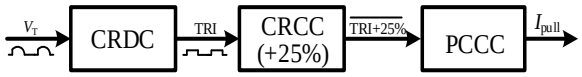


Fig. 4. Dimming control circuits with a wide tuning range.

can be expressed as:

$$I_{RC} = \frac{1}{2} \cdot \frac{N_S}{N_P} \cdot \frac{R_2}{R_{CS}} \cdot I_{REF} \tag{7}$$

In Eq (7), I_{REF} is the reference current, R_2 is the converted resistor of the CC, and N_S and N_P are the turns of the primary-side winding and secondary-side winding, respectively. The core dimming scheme is controlled by the proposed dimming control circuit, and the detailed dimming principle is emphatically explained.

C. Wide Tuning Range Dimming Principle

The proposed dimming control circuit of a wide tuning range is presented in Fig. 4, including the conduction ratio detection circuit (CRDC), the conduction ratio compensation (CRCC) and the pull-down current control circuit (PCCC). The conduction ratio D is the ratio of the conduction angle with 180°. Generally, the maximum and minimum D are set as 75% and 20%, respectively, since the conduction angle of the TRIAC dimmer is limited.

During normal operation, the ac input voltage is chopped by the TRIAC and the sensed voltage waveforms are V_T. The V_T signal is compared to a small threshold voltage 0.2V in the CRDC and the output signal TRI is a pulse signal with its duty cycle proportional to the conduction angle D. The CRCC adds an extra 25% duty cycle to the TRI and inverts it to an output signal $\overline{\text{TRI+25\%}}$. As a result, when D is less than 75%, the duty cycle of $\overline{\text{TRI+25\%}}$ is 1-(D+25%). Similarly, when D is larger than 75%, $\overline{\text{TRI+25\%}}$ is always kept at a low voltage and its duty cycle is zero.

The PCCC generates the pull-down current I_{pull} by two manipulated variables K and $D_{\overline{\text{TRI+25\%}}}$. As a result, I_{pull} can be expressed as:

$$I_{pull} = K \cdot I_{REF} \cdot D_{\overline{\text{TRI+25\%}}} \tag{8}$$

In Eq (8), I_{pull} is the pull-down current from the proposed dimming control circuit, I_{REF} is the reference current, K is the pull coefficient of the PCCC, which is controlled by the reference voltage and resistor, and $D_{\overline{\text{TRI+25\%}}}$ is the duty cycle of $\overline{\text{TRI+25\%}}$ coming from the CRCC. In order to make the output current go down to zero when D comes to its minimum value 20%, according to Eq (6) and (8), the pull coefficient K of the PCCC can be determined by Eq (9).

$$I_{REF} = K \cdot I_{REF} \cdot (1-(20\%+25\%)) \tag{9}$$

In Eq (9), I_{REF} is the reference current, and K must be set as 1.78.

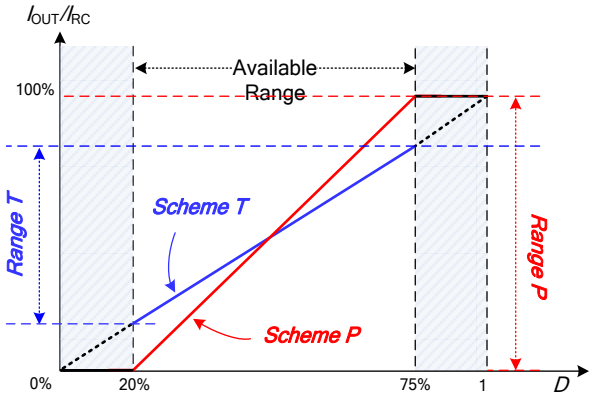


Fig. 5. Theoretical dimmer outline of a wide tuning range design.

Combining Eq (6), (7) and (8) with K=1.78, the output current can be rewritten as:

$$I_{OUT} = 1.78 \cdot D \cdot I_{RC} - 0.33 \cdot I_{RC} \tag{10}$$

Eq (10) shows that the output current I_{OUT} is linear to the conduction ratio D, and I_{RC} is the rated output current.

When the conduction ratio D varies from 20% to 75%, the output current I_{OUT} can be regulated from zero to I_{RC}.

The theoretical dimmer outline of the traditional dimming control circuit and the proposed dimming control circuit is shown in Fig. 5. Traditionally, the output current is directly controlled by the conduction ratio D without any conduction ratio compensation or optimization of the pull coefficient K. Therefore, the output current range is always restricted by the limited conduction ratio D, as shown by Scheme T in Fig. 5. The proposed dimming control circuit can manage the maximum output current up to I_{RC} when D is above 75%, and the minimum output current down to zero when D is less than 20%. Therefore, the proposed control circuit can manage the wide tuning range.

D. Two-Stage Uniform Dimming Principle

The proposed wide tuning range and two-stage uniform dimming control circuit is developed from a previous design and its diagram is given in Fig. 6. With the rapid dimming curve l_1 and the slow dimming curve l_2, the output current can be regulated relatively uniform in the whole adjustable range, since eyes are sensitive to small current LED lighting but not to large current LED lighting. In addition, the dimming curves l_1 and l_2 are selected by the switch circuit. Compared with TRI_REF whose duty cycle is 50%, rapid dimming l_1 is chosen when D is larger than 50%, and slow dimming l_2 is selected when D is smaller than 50%.

The rapid dimming curve l_1 consists of the CRDC, CRCC and PCCC, and its pull coefficient K_1 is 2.5. Similar to the wide tuning range design, the CRDC detects the conduction angle D. The CRCC adds an extra 25% duty cycle to the TRI and then inverts it to the output signal $\overline{\text{TRI+25\%}}$. The pull-down current I_{pull1} of l_1 is generated from PCCC(K_1=2.5)

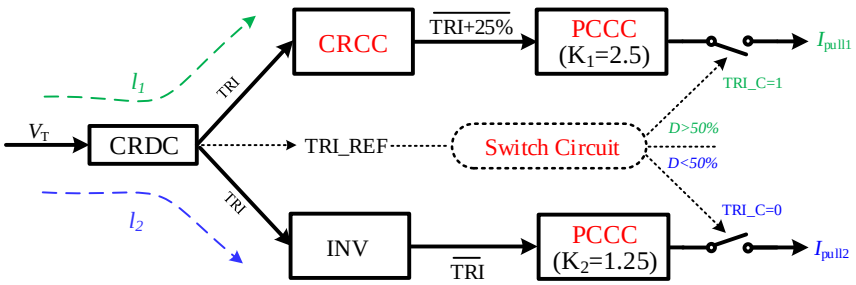


Fig. 6. Wide tuning range and a two-stage uniform dimming control circuit.

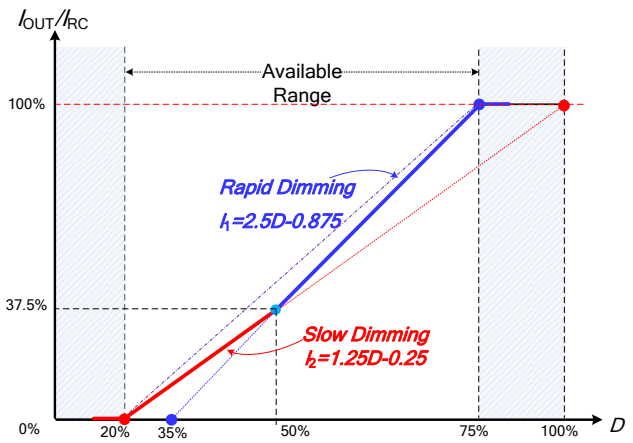


Fig. 7. Theoretical output outline of the wide tuning range and two-stage uniform dimming design.

and meets Eq (11).

$$I_{\text{pull1}} = D_{\overline{\text{TRI+25\%}}} \cdot K_1 \cdot I_{\text{REF}} = 2.5 \cdot (1 - D - 25\%) \cdot I_{\text{REF}} \quad (11)$$

In Eq (11), $D_{\overline{\text{TRI+25\%}}}$ is the duty cycle of $\overline{\text{TRI+25\%}}$ from the CRCC, and K_1 is the pull coefficient of the PCCC in l_1. D is the conduction ratio.

The slow dimming curve l_2 is composed of the CRDC, INV and PCCC with the pull coefficient K_2=1.25. The INV is an inverter to reverse the TRI to obtain $\overline{\text{TRI}}$. The pull-down current I_{pull2} is generated from the PCCC (K_2=1.25) and satisfies:

$$I_{\text{pull2}} = D_{\overline{\text{TRI}}} \cdot K_2 \cdot I_{\text{REF}} = 1.25 \cdot (1 - D) \cdot I_{\text{REF}} \quad (12)$$

In Eq (12), $D_{\overline{\text{TRI}}}$ is the duty cycle of $\overline{\text{TRI}}$ coming from the INV, and K_2 is the pull coefficient of the PCCC in l_2. D is the conduction ratio.

Through the switch circuit, the pull-down current I_{pull} can be switched between I_{pull1} and I_{pull2} according to the conduction ratio D, and I_{pull} can be expressed as:

$$I_{\text{pull}} = \begin{cases} 2.5 \cdot [1 - (D + 0.25)] \cdot I_{\text{REF}}; (0.5 < D < 0.75) \\ 1.25 \cdot (1 - D) \cdot I_{\text{REF}} \quad ; (0.2 < D < 0.5) \\ I_{REF} \quad ; (0 < D < 0.2) \\ 0 \quad ; (0.75 < D < 1) \end{cases} \quad (13)$$

In Eq (13), I_{pull} is the pull-down current of the proposed dimming control circuit, I_{REF} is reference current and D is conduction ratio of the TRIAC dimmer.

According to Eq (6), (7) and (13), the output current I_{OUT} can be rewritten as:

$$I_{\text{OUT}} = \begin{cases} 2.5 \cdot D \cdot I_{\text{RC}} - 0.875 \cdot I_{\text{RC}}; (0.5 < D < 0.75) \\ 1.25 \cdot D \cdot I_{\text{RC}} - 0.25 \cdot I_{\text{RC}}; (0.2 < D < 0.5) \\ I_{\text{RC}} \quad ; (0.75 < D < 1) \\ 0 \quad ; (0 < D < 0.2) \end{cases} \quad (14)$$

In Eq (14), I_{OUT} is the output current, I_{RC} is the rated output current, and D is the conduction ratio.

Based on Eq (14), a theoretical output diagram of the wide tuning range and the two-stage uniform dimming design is presented in Fig. 7.

In Fig. 7, when the adjustment of the TRIAC dimming conduction angle is between 20% and 75%, the current flowing through the LED can be adjusted between zero and the rated output current. When the conduction angle is greater than 50%, the LED output current with the conduction angle changes quickly into the fast dimming mode; when the conduction angle is less than 50%, the LED output current with the conduction angle changes slowly into the slow dimming mode. The output current can be adjusted from zero to the rated current value throughout the active range of the TRIAC dimmer, and the brightness of the LEDs observed by the human eye remains relatively uniform throughout the dimming interval. 50% is the result of multiple tests and brightness verifications, which is the experience value. When Selecting 50% as the critical point of the slow and fast current regulation, it is possible to realize the best characteristics of uniform dimming. Therefore, with two-stage dimming optimization, the proposed control circuit can manage a wide tuning range and two-stage uniform dimming.

III. Design Considerations of the Key Circuits

In order to achieve the proposed wide tuning range and two-stage uniform dimming characteristic, key circuits of the developed dimming control circuit are discussed in detail.

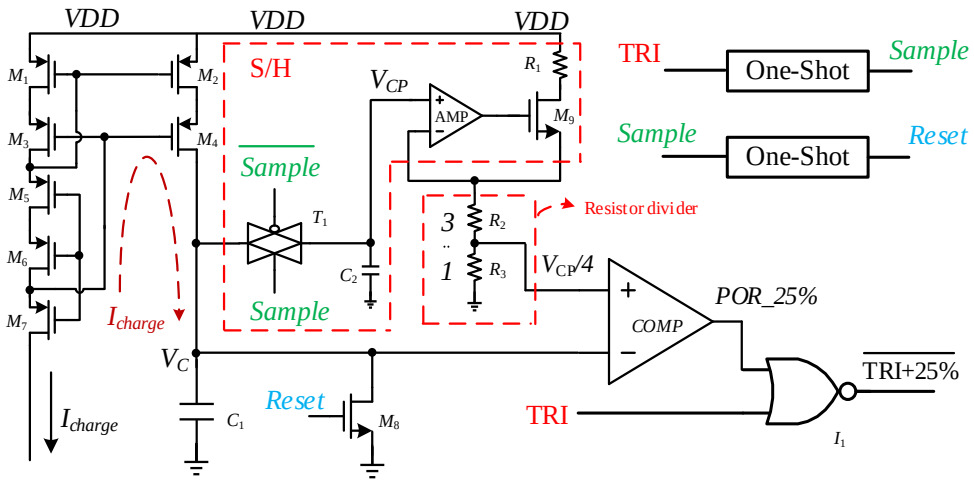


Fig. 8. Design implementation of the conduction ratio compensation circuit.

A. *Conduction Ratio Compensation Circuit (CRCC)*

The CRCC is the core circuit to improve the dimming range of the output current. By imposing an extra compensation to the detected conducted ratio, the weakness where the maximum conduction ratio cannot reach 100% can be avoided, and the maximum output current can reach rated output current.

In order to achieve an extra 25% compensation for D, a conduction ratio compensation circuit is designed in Fig. 8, which contains a sample and hold (S/H) module, resistor divider, comparator, one-shot and charging/discharging circuit composed of M_1~M_7, C_1 and M_8. The one-shot is a monostable trigger, outputting a narrow pulse signal at the falling edge of the input signal during each cycle. A high precision cascade current mirror consists of M_1~M_7 to charge the capacitance C_1, and M_8 discharges C_1 rapidly when the reset signal is high. The S/H is composed of the transmission gate T_1, holding capacitance C_2, amplifier, M_9 and R_1. R_2 is three times R_3 in value, and resistor divider is formed.

Fig. 9 shows key operation waveforms of the conduction ratio compensation circuit. The TRI is the detected conduction ratio signal coming from the CRDC. In addition, a narrow pulse signal sample and reset can be achieved by the TRI and sample, respectively. The current I_{charge} charges the capacitance C_1, and V_C increases linearly in every cycle. When the signal reset is active, V_C must be dropped to zero. Before the signal reset, the peak voltage V_{CP} of V_C is sampled and held by a signal sample in the S/H. Processed by the resistor divider, $V_{CP}/4$ can be achieved and compared with V_C. As a result, a 25% extra compensation signal POR_25% is achieved. With a logical gate, the signal TRI+25% after compensation can be obtained, as can the signal $\overline{\text{TRI+25\%}}$ as shown in Fig. 9.

B. *Switch Circuit*

The switch circuit is designed to identify whether D is larger

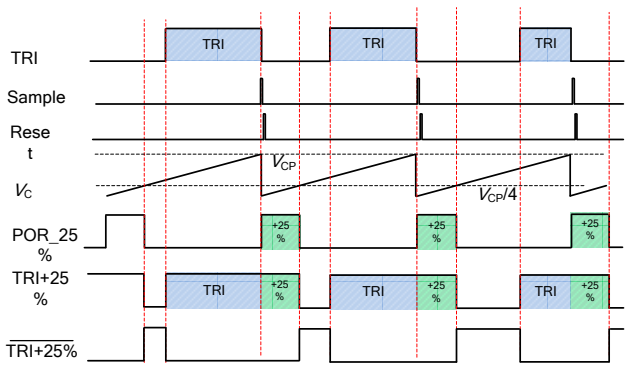


Fig. 9. Key operation waveforms of the conduction ratio compensation circuit.

than 50%. Therefore, a switch reference signal TRI_REF with a 50% duty ratio and the same period as the TRI must be introduced. The circuit to generate the switch reference signal TRI_REF is similar to the conduction ratio compensation circuit. With the resistor ratio of the resistor divider in the CRCC replacing 3/1 with 1/1, $V_{CP}/2$ is compared with V_C and switch reference signal TRI_REF, the duty ratio of which is 50%.

The switch circuit is shown in Fig. 10. The TRI is the detected conduction ratio signal. TRI_REF is the switch reference signal and $\overline{\text{TRI+25\%}}$ is the output of the CRCC. D_1 is triggered by the falling edge of the clock, and the switch circuit outputs TRI_C and TRI_P. When D is larger than 50%, TRI_C=1, and the rapid dimming curve is selected. Namely, the PCCC, the pull coefficient K_1 of which is 2.5, is selected and TRI_P is $\overline{\text{TRI+25\%}}$. Otherwise, when D is less than 50%, TRI_C=0, and the slow dimming curve is chosen. Namely, the pull coefficient K_2 of the PCCC is 1.25 and TRI_P is the $\overline{\text{TRI}}$. As a result, the dimming curve can be switched between l_1 and l_2.

From Fig. 11, when D is larger than 50%, TRI_REF is in

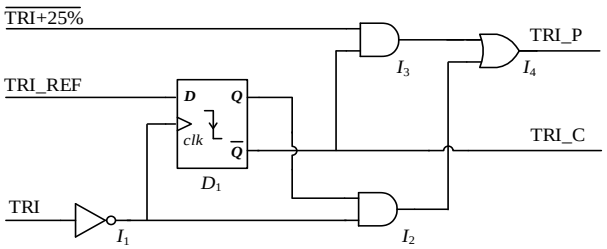


Fig. 10. Design implementation of the switch circuit.

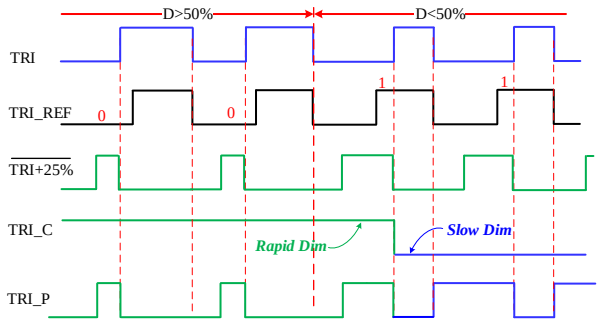


Fig. 11. Key operation waveforms of the switch circuit.

low voltage while the flip-flop D_1 is triggered at the rising edge of TRI. TRI_C is kept high, the output of I_2 is 0, and TRI_P follows $\overline{\text{TRI+25\%}}$. When D is less than 50%, the flip-flop D_1 is triggered at the rising edge of TRI and TRI_REF is in the high voltage. Meanwhile, TRI_C stays in low level, the output of I_3 is 0, and TRI_P follows $\overline{\text{TRI}}$. As a result, TRI_P can be switched from $\overline{\text{TRI+25\%}}$ to $\overline{\text{TRI}}$. At the same time, TRI_C can be changed from 1 to 0.

C. Pull-Down Current Control Circuit (PCCC)

In order to satisfy the different requirements of the rapid dimming curve and to slow the dimming curve, two pull-down current control circuits with different coefficient, namely PCCC(K_1=2.5) and PCCC(K_2=1.25) are designed as shown in Fig. 12. The detail circuit of each branch consists of an amplifier AMP, NMOS and pull resistor R_p. The average pull-down current is determined by the reference voltage V_{REF}, pull resistor R_p and the duty ratio of the pull-down current control signal TRI_P, as defined in Eq (15) and (16).

$$I_{pull1} = K_1 \cdot I_{REF} \cdot D_{TRI\_P} = 2.5 \cdot I_{REF} \cdot D_{TRI\_P} = \frac{V_{REF}}{R_{p1}} \cdot D_{TRI\_P} \quad (15)$$

$$I_{pull2} = K_2 \cdot I_{REF} \cdot D_{TRI\_P} = 1.25 \cdot I_{REF} \cdot D_{TRI\_P} = \frac{V_{REF}}{R_{p2}} \cdot D_{TRI\_P} \quad (16)$$

In Eq (15) and (16), I_{pull1} is the average pull-down current of the PCCC (K_1=2.5), and I_{pull2} is the average pull-down current of the PCCC (K_2=1.25). D_{TRI_P} is the duty ratio of TRI_P, and I_{REF} is the inner reference current. The pull resistors in the PCCC (K_1=2.5) and PCCC (K_2=1.25) are called R_{p1} and R_{p2}, respectively. Therefore, the coefficients K_1 and K_2 are determined by the pull resistors R_{p1} and R_{p2},

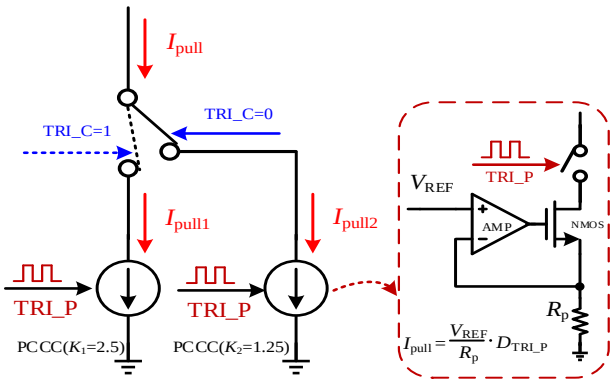


Fig. 12. Design implementation of the pull-down current control circuit.

respectively. By adjusting the value of the pull resistor, the pull coefficient of the PCCC can be regulated.

As shown in Fig. 12, TRI_C and TRI_P come from the switch circuit. When TRI_C=1, I_{pull1} generated from the PCCC (K_1=2.5) is selected, and I_{pull}=I_{pull1}. On the other hand, when TRI_C=0, I_{pull2} which comes from the PCCC (K_2=1.25) is obtained, and I_{pull}=I_{pull2}. As the result, the designed dimming outline can be achieved by the proposed system.

IV. Experimental Results

In order to verify the performance of the proposed scheme, a control IC for a TRIAC controlled AC-DC LED driver with a wide tuning range and two-stage uniform dimming has been implemented in a TSMC 0.35μm 5V/600V CMOS/LDMOS process. A micrograph is shown in Fig. 13 and the die size with PADs is 900μm *700μm. The chip includes a I_{out} estimation module, constant current module, PFC control module, voltage and current reference module, logical control circuit, conduction ratio compensation module, pull-down current control circuit, conduction ratio detection module, and UVLO & protection circuit.

A 10W circuit prototype with universal ac input (90-132Vac) and 21V/500mA dc output is built to drive 7 LEDs, as shown in Fig. 14. The key components and parameters of the proposed driver are listed in Table I.

Fig. 15 shows the measured output current versus the input voltage from 90V to 132V, without dimming conduction. From Fig. 15, the maximum output current is 510mA with a 110Vac input, and the minimum output current is 497mA witha 90Vac input. The voltage linear regulation is defined as the ratio of the difference between the maximum and minimum values to the theoretical value 500mA, about 2.6%, which shows that the output current variation is about 2.6% in the whole input range.

The input power factor versus the input voltage at no dimming conduction is shown in Fig. 16. The PF is well above 0.98 in the entire input range, which meets the related input current harmonics requirement. The maximum PF is up

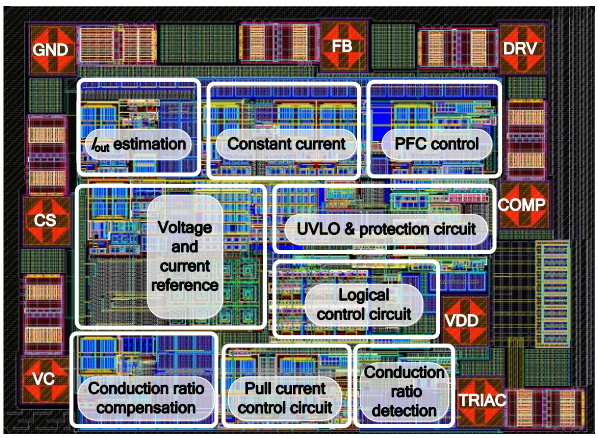


Fig. 13. Micrograph of the fabricated chip.

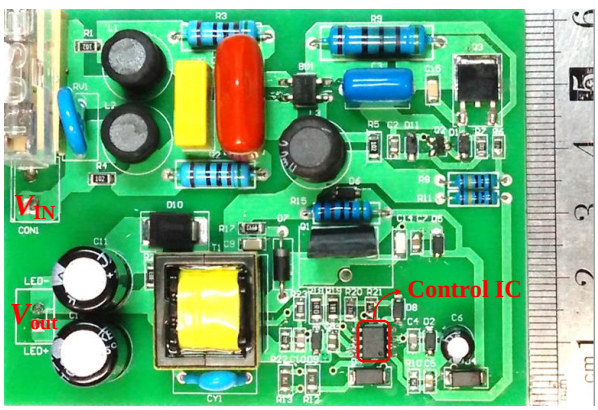


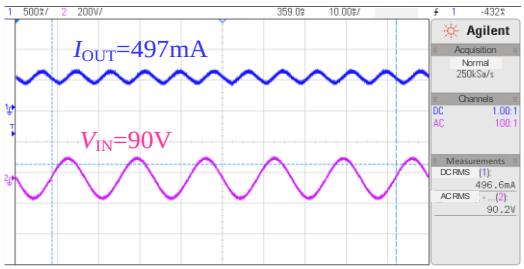
Fig. 14. Prototype of the proposed LED driver.

TABLE I
KEY COMPONENTS AND PARAMETERS

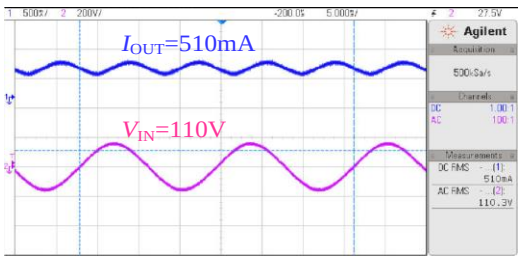
Parameters	Symbol	Value
AC input voltage	V_{IN}	90~132Vac（RMS）
Output current	I_{OUT}	500mA
Output voltage	V_{OUT}	21V
Bridge rectifier	BD1	MB6S
Primary-side inductance	L_P	1.15mH
Transformer core	T	EE6
Transformer Turns-ratio	$N_P : N_S : N_A$	157/31/37
Power MOSFET	Q_1	AP03N70
Output capacitor	C_o	470μF/35V
Primary-side current sense resistor	R_{CS}	2Ω

to 99.6% at 100Vac input. The measured efficiency of the prototype at no dimming conduction is shown in Fig. 17. The maximum efficiency is 83% at 132Vac input, and the minimum efficiency is above 75% in seven 3W-LEDs.

Fig. 18 shows the measured input current and rectified bus voltage V_T at different conduction ratios. The TRIAC dimmer



(a)



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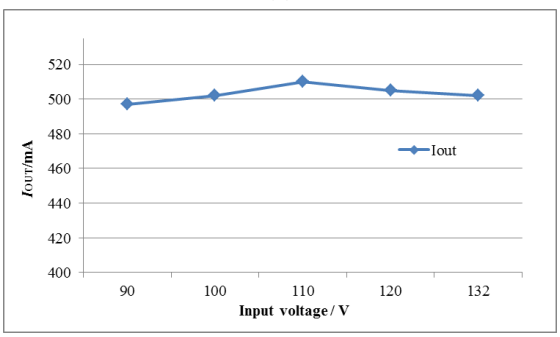
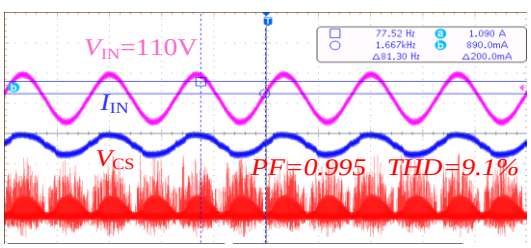
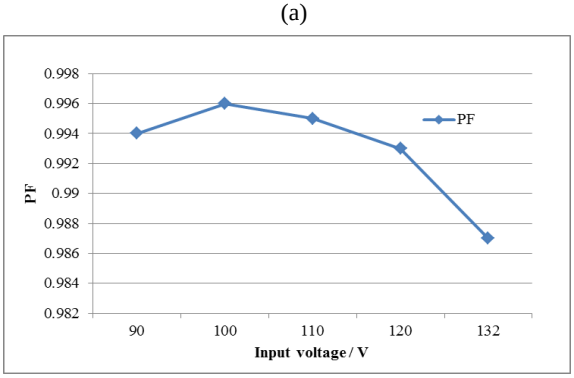


(c)

Fig. 15. Diagrams of: (a) measured steady-state waveforms under 90Vac; (b) measured steady-state waveforms under 110Vac; (c) measured output current IOUT versus the ac input voltage VIN.



(a)



(b)

Fig. 16. Diagrams of: (a) measured power factor under 110Vac and 60Hz-input; (b) measured PF versus the ac input voltage.

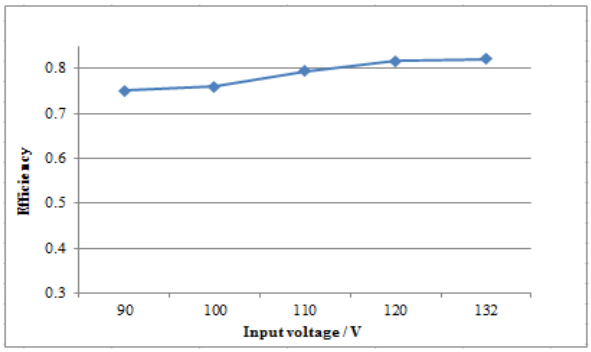
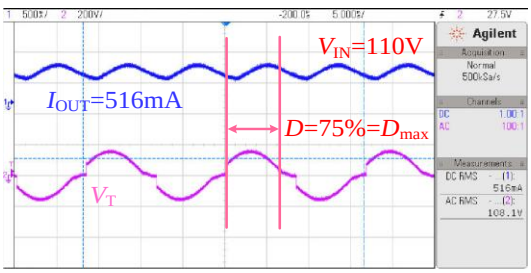
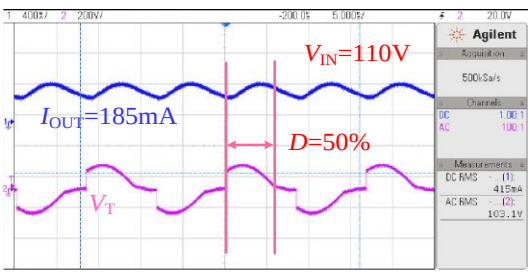


Fig. 17. Measured efficiency versus the ac input voltage.



(a)



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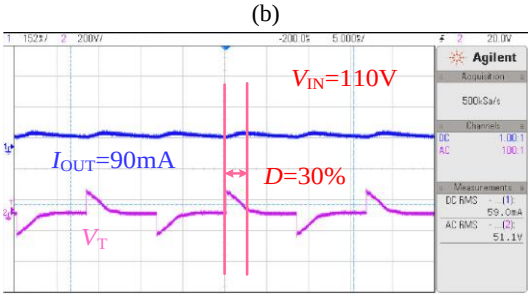
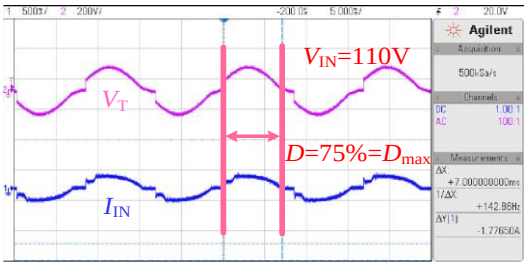
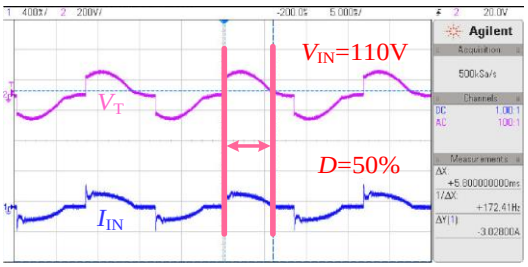


(c)

Fig. 18. Measured steady waveforms under 110Vac and 60Hz at: (a) D=75%; (b) 50%; (c) D=30%.



(a)



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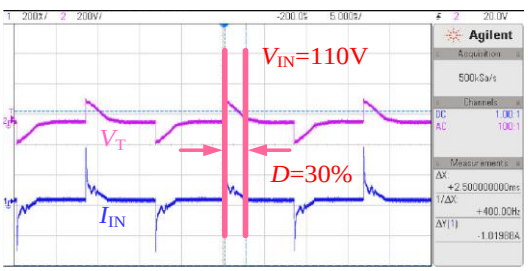

(c)

Fig. 19. Measured output current waveforms under 110Vac and 60Hz at: (a) D=75%; (b) D=50%; (c) D=30%.

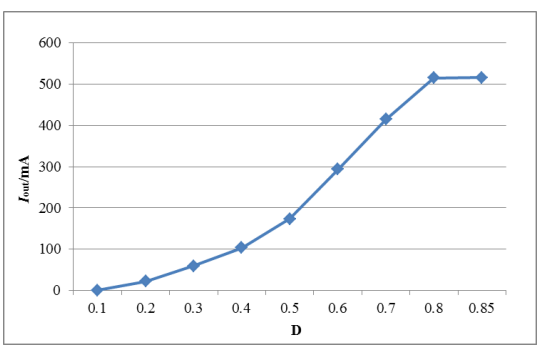

Fig. 20. Measured output current versus the conduction ratio.

used in the testing is a LEVITION 6633-P. It is clear that the input current follows the input voltage and that the input characteristic of the prototype is resistive.

Fig. 19 shows the measured output current and rectified bus voltage at different conduction ratios. The value of the output current is marked in the dimming mode D=75%, D=50%, and D=30%, respectively.

Fig. 20 shows the output current versus the conduction ratio at 110Vac input. From Fig. 20, the maximum output current is as large as the rated output current, and the minimum output current is nearly zero. In the whole dimming range, the dimming outline consists of a rapid dimming curve and a slow dimming curve. Therefore, the dimming outline exerts a wide tuning range and two-stage uniform dimming characteristics.

Finally, Table II shows a performance comparison with prior studies. From Table II, it is shown that the maximum output current I_{MAX} of the proposed TRIAC dimming driver is up to the rated output current I_{RC}, and that the current ratio which is the ratio of I_{MAX} and I_{RC}, is about 100%. In addition, its minimum dimming current I_{MIN} is only 5mA, and the dimming ratio which is the ratio of I_{MIN} and I_{MAX}, is less than 1%.

TABLE II
COMPARISON BETWEEN THE PROPOSED METHOD AND PRIOR STUDIES

	This work	**[15]**	**[16]**	**[14]**
Topology	FLYBACK-PSR	FLYBACK-PSR	FLYBACK-PSR	FLYBACK-PSR
Working mode	BCM	BCM	-	BCM
Rated load	21V/0.5A	27V/0.5A	24V/0.3A	28V/0.5A
Conduction ratio D	10%~85%	19%~78%	4%~92%	12%~89%
Efficiency η	83%	87.5%	80%	87%
Power factor PF	0.995	0.985	-	0.99
Rated current I_{RC}	510mA	475mA	300mA	-
Maximum dimming Current I_{MAX}	516mA	370mA	270mA	550mA
Minimum dimming Current I_{MIN}	5mA	50mA	13mA	50mA
Current ratio I_{MAX}/I_{RC}	≈100%	≈78%	≈90%	-
Dimming ratio I_{MIN}/I_{MAX}	1%	13%	4%	9%

V. CONCLUSIONS

This paper proposes a TRIAC controlled AC-DC LED driver chip with a wide tuning range and two-stage uniform dimming. When compared with prior designs, the dimming range is no longer restricted by the limited conduction ratio of TRIAC dimmers and the LED lights change more uniformly with the TRIAC dimmer. A theoretical analysis and key circuits are illustrated in this paper. The proposed control chip is fabricated in a TSMC 0.35μm 5V/650V CMOS/LDMOS process, and verified in a 21V/500mA circuit prototype. The test results show that, in 90V/60Hz~132V/60Hz ac input range, the voltage linear regulation is 2.6%, the power factor is 99.5%, and the efficiency is 83%. Moreover, in the dimming mode, the maximum dimming current is 516mA, with the corresponding rated current 510mA, the minimum dimming current is almost zero, and the dimming rate is less than 1%. Therefore, the proposed control chip has a promising application in TRIAC-dimmable LED drivers.

ACKNOWLEDGMENT

The authors would like to thank the National Natural Science Foundation of China (Grant No.61376029), the Fundamental Research Funds for the Central Universities, China, and the Research and Innovation Program for Graduate Students in Universities of Jiangsu Province (Grant No. SJLX16 0081) for supporting this research.

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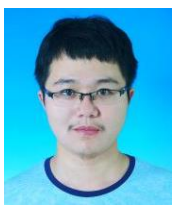

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