A Generalized Space Vector Modulation Scheme Based on a Switch Matrix for Cascaded H-Bridge Multilevel Inverters

Pratheesh K. J.[*], Jagadanand G.[*], and Rijil Ramchand[†]

[†,*]Department of Electrical Engineering, National Institute of Technology, Calicut, India

Abstract

The cascaded H Bridge (CHB) multilevel inverter (MLI) is popular among the classical MLI topologies due to its modularity and reliability. Although space vector modulation (SVM) is the most suitable modulation scheme for MLIs, it has not been used widely in industry due to the higher complexity involved in its implementation. In this paper, a simple and novel generalized SVM algorithm is proposed, which has both reduced time and space complexity. The proposed SVM involves the generalization of both the duty cycle calculation and switching sequence generation for any n-level inverter. In order to generate the gate pulses for an inverter, a generalized switch matrix (SM) for the CHB inverter is also introduced, which further simplifies the algorithm. The algorithm is tested and verified for three-phase, three-level and five-level CHB inverters in simulations and hardware implementation. A comparison of the proposed method with existing SVM schemes shows the superiority of the proposed scheme.

Key words: Cascaded H bridge (CHB) inverter, Five-level inverter, Multilevel inverters (MLI), Space vector modulation (SVM), Three-level inverter

I. INTRODUCTION

The introduction of the first multilevel inverter in the 1970s, classified as a three-level diode clamped inverter [1], substituted conventional high power two-level inverters for high power, medium voltage applications in the industry [2]. The aforementioned diode clamped topology, along with the flying capacitor (FC) and cascaded H bridge multilevel inverter topologies [3], have been established as classical multilevel topologies since then [4]. The industry has benefited from these multilevel inverter topologies due to their operation with low dv/dt, low harmonics and reduced device voltage stress when compared to two-level inverters [5]. The modular structure of the CHB multilevel inverter, a worthwhile advantage when compared to other classical MLI topologies, makes it ideal for systems such as photovoltaic arrays, fuel cells, batteries, etc. [6].

Popular modulation techniques [7] for multilevel inverters are carrier based pulse width modulation (PWM) [8], space vector modulation (SVM) [9] and nearest level modulation (NLM) [10]. The harmonics around the modulation frequency, the higher switching frequency and the difficulty in implementation as the number of levels increases, are some of the major drawbacks of carrier-based PWM [11]. Carrier-based PWM is a phase voltage modulation scheme that compares a triangular carrier wave and a reference sine wave to generate the PWM [12]. The conventional SVM deals with line-to-line voltages, which in turn act on all of the phases simultaneously, as opposed to the carrier-based PWM schemes. It is capable of utilizing the flexibility presented by the multilevel inverters such as the use of redundant space vectors [13], adjustable duty ratios and multiple switching sequences [14]. SVM algorithms include generalized 2D algorithms and 3D algorithms for any n-level inverter. Typically, these algorithms involve the following steps: determining the nearest three vectors of the reference vector (by finding the sector and triangle in which the reference vector is located) [15], computing the duty cycles (using complex equations) and selecting an appropriate switching

sequence [16]. These practices make the whole SVM algorithm complex and difficult to implement using a 2D algorithm, not to mention 3D SVM algorithms [17], which are a lot more cumbersome to implement. A brief review of the popular multilevel modulation techniques based on 2D algorithms [18]-[25] is presented in the following paragraph.

The phase disposition PWM [18] does not offer reduced complexity or flexible selection of the common mode voltages and carrier waves; while the carrier based SVPWM schemes use lookup tables for the generation of modulation waveforms [19]. The fast SVPWM scheme based on coordinate transformation [20] uses complex equations for the duty cycle computations and the generation of the switching states in this scheme lacks efficiency. The generalized SVM based on a two-level inverter [21] also employs a lookup table to store the switching states offline. Even though the generalized SVM in [22] does not make use of lookup tables, the increase in the number of levels of the inverter results in an increase in the computational complexity. Although the well-organized SVM schemes in [23] and [24] do not use lookup tables, these methods also suffers from increased computational complexity especially for the determination of the nearest vectors. The generalized method based on the *l*-factor approach in [25] provides a simple and real-time operation compatible algorithm. However, it involves too many steps when compared to the previous methods. Another major disadvantage of this approach is the presence of errors due to the approximations of the switching pulse durations.

An alternative method for SVM is the much simpler NLM method. Like the carrier based PWM, NLM also deals with the phase voltages. Here, the procedure is to calculate the nearest two voltage levels of the reference voltage vector and their duty ratios [26]. Although NLM is easier to implement than SVM, the selection of the redundant switching states and the adjustment of the duty ratios are not possible [27]. NLM also has a higher switching frequency resulting in higher switching losses when compared to SVM. However, the simplicity of NLM is helpful for reducing the complexity of the SVM.In this paper, such an SVM scheme is proposed, where time and space complexity reductions are achieved.

The proposed algorithm in this paper mainly focuses on simplicity and has the following notable features.

1. It is a simple and generalized method suitable for digital implementation with real-time computations.
2. The new approach to calculate the duty ratio does not involve any sector or triangle identification, which is a significant improvement when compared to the existing SVM methods.
3. There is no need to store all of the space vectors or switching states in a lookup table sincethe proposed method uses a generalized method for switching sequence generation. This saves memory especially for a higher number of levels.

Fig. 1. Space vector diagram of a three-level inverter.

4. The introduction of a generalized switch matrix whereit is possible to obtain the gate pulses for any n-level CHB inverter by varying a single parameter (the number of levels -n).
5. The time and space complexity remain almost the same, regardless of the number of levels. Meanwhile, in the conventional and existing SVMs, when the number of levels increases, they increase as a function of the number of levels.
6. The proposed SVM is suitable for the online variations of the modulation index, due to the simplicity and speed of the execution of the algorithm. This, in turn, helps to implement the proposed method even with a low-end microprocessor.

The proposed algorithm is explained with respect to a three-level CHB inverter (CHBI). Simulation and experimental results for a three-level CHBI and a five-level CHBI are also analyzed to support the proposed method.

II. PRINCIPLES OF SPACE VECTOR MODULATION AND NEAREST LEVEL MODULATION

A. Space Vector Modulation

Space vector modulation concurrently deals with all of the phases of a three-phase inverter. Hence, the reference vector V_{ref} accounts for the individual reference vectors for each of the three phases. If V_a^*, V_b^* and V_c^* are the reference phase voltages of phases *A*, *B* and *C*, the SVM reference vector for any *n* level inverter can be calculated in (1).

$$V_{ref} = (n-1) \times (V_a^* + V_b^* . e^{j2\pi/3} + V_c^* . e^{j4\pi/3}) \quad (1)$$

For the linear modulation range, this reference vector follows a circular trajectory, enclosed inside a regular hexagon, which is made of space vectors. From the space vector diagram in Fig. 1, it can be determined that the reference vector may be located in any one of the small triangles and that it is possible to synthesize one using its nearest three vectors (NTV). If V_0, V_1 and V_2 are the nearest three vectors of the reference voltage vector V^*, then it can be synthesized in (2).
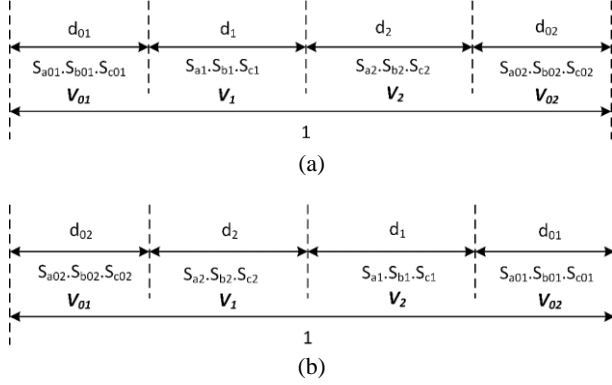
Fig. 2. Switching sequence in space vector modulation:(a) ascending; (b) descending.
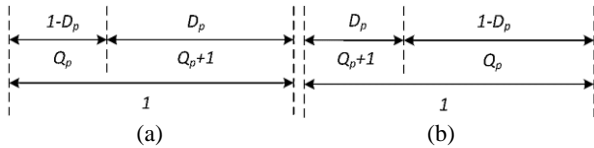

Fig. 3. Switching sequence in nearest level modulation: (a) ascending; (b) descending.

$$V^* . T_s = T_0 . V_0 + T_1 . V_1 + T_2 . V_2 \qquad (2)$$

$$T_0 + T_1 + T_2 = T_s \qquad (3)$$

where T_0, T_1 and T_2 are the times for which the nearest vectors V_0, V_1 and V_2 are switched during a sampling period with a of duration T_s. In order to generate a switching sequence from the selected nearest three vectors, which also consist of redundant switching states, (2) can be written as (4).

$$V^* = V_{01} . d_{01} + V_1 . d_1 + V_2 . d_2 + V_{02} . d_{02} \qquad (4)$$

$$d_{01} + d_1 + d_2 + d_{02} = 1 \qquad (5)$$

Thus, a switching sequence has four switching vectors V_{01}, V_1, V_2 and V_{02} and corresponding duty cycles namely, d_{01}, d_1, d_2, and d_{02} as shown in Fig. 2. The switching states corresponding to these four vectors can be represented as $(S_{a01}\ S_{b01}\ S_{c01})$, $(S_{a1}\ S_{b1}\ S_{c1})$, $(S_{a2}\ S_{b2}\ S_{c2})$ and $(S_{a02}\ S_{b02}\ S_{c02})$. The first two switching states are the redundant switching states and their corresponding duty cycles (d_{01} and d_{02}) are freely adjustable. The switching sequence may be arranged in two ways: ascending the switching sequence so that $S_{a01} < S_{a02}$ as shown in Fig. 2(a), and descending the switching sequence so that $S_{a01} > S_{a02}$ as shown in Fig. 2(b).

B. Nearest Level Modulation

Unlike space vector modulation with a rotating reference vector, nearest level modulation deals with the individual phase voltage reference, which in this case is the phase voltage of the inverter calculated in (6).

$$V_p^* = [Q_p . (1 - D_p) + (Q_p + 1) . D_p] . V_{dc}/(n-1)$$
$$= (Q_p + D_p) . V_{dc}/(n-1) \qquad (6)$$
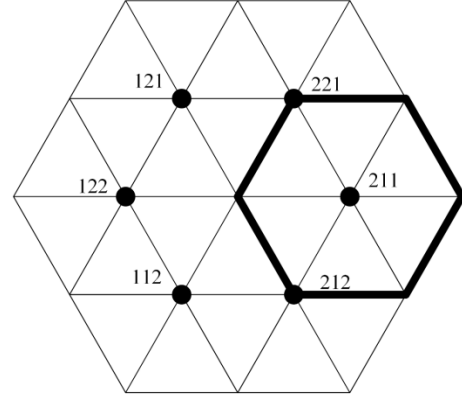
Fig. 4. Sub-hexagon centres in a space vector diagram of a three level inverter.

where D_p is the duty ratio of the phase p ($p = A$, B or C) and Q_p is the value of the switching state S_p of the inverter. In NLM, during one sampling period, each phase is switched between two adjacent switching states. Here, the switching can be done in ascending mode where the switching sequence varies as shown in Fig. 3(a) or in descending mode where the switching sequence varies as shown in Fig. 3(b). Since individual phase voltages are accounted for in NLM, it is easier to employ this method for multiphase multilevel inverters. To obtain the duty cycles of each phase in NLM, from (6), the level shifted voltage components for each of the phases (A, B and C) are calculated in (7).

$$U_p^* = m_i \times (n-1) \times V_p^* \qquad (7a)$$

$$U_p = U_p^* + ((n-1)/2) \qquad (7b)$$

where, $p = A$, B or C. The largest integer value of these level-shifted voltage components are then determined using the *ceiling* function in (8).

$$U_{ip} = ceil(U_p) \qquad (8)$$

Now, the duty ratios for each phases can be calculated in (9).

$$D_p = (U_{ip} - U_p) \qquad (9a)$$

$$\text{Such that, } 0 \le D_p \le 1 \qquad (9b)$$

III. PROPOSED SPACE VECTOR MODULATION

A. Generalized Method for SVM Duty Cycle Calculation

Conventional SVM methods generally follow a systematic procedure that involves locating the triangle and sector where the reference vector lies and then finding the nearest three vectors or switching states corresponding to this particular location, making the whole activity complex and difficult to implement in a processor in terms of both execution time and memory. The proposed method directly provides the nearest three vectors corresponding to the reference vector location using a simple, single step calculation using (8). They are in

TABLE I
DUTY RATIO CLASSIFICATION

Sequence Selector k	Duty ratio classification
1	$D_a \geq D_b \geq D_c$
2	$D_a \geq D_c \geq D_b$
3	$D_b \geq D_a \geq D_c$
4	$D_b \geq D_c \geq D_a$
5	$D_c \geq D_a \geq D_b$
6	$D_c \geq D_b \geq D_a$

Fig. 5. D_{max}, D_{mid} and D_{min} variation.
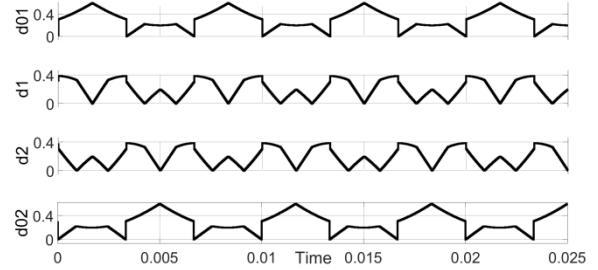
Fig. 6. SVM duty cycles using the proposed method.

fact, the sub-hexagon centers in a space vector diagram of the particular inverter as shown in Fig. 4. For example, if the reference vector is located in the second sector of the highlighted sub-hexagon in Fig. 4, first the proposed algorithm calculates the center of this sub-hexagon, which is 211. Then, the algorithm can use the switching state 211 to generate the nearest three vectors, which are 211, 221 and 321 or the switching sequence 211-221-321-322 as per the requirement. The algorithm can also calculate, in a similar manner, all of the other switching states including the redundant switching states in this particular sub-hexagon from the switching state 211. Thus, there is no need to store all of the switching states of the space vector diagram in the memory, the size of which really matters when the number of inverter levels increases.

Now, to derive the duty cycle expressions for the proposed space vector modulation, consider (4) for the phases A, B and C of the inverter.

$$V_a^* = (S_{a01}.d_{01} + S_{a1}.d_1 + S_{a2}.d_2 + S_{a02}.d_{02}).\frac{V_{dc}}{(n-1)} \quad (10a)$$

$$V_b^* = (S_{b01}.d_{01} + S_{b1}.d_1 + S_{b2}.d_2 + S_{b02}.d_{02}).\frac{V_{dc}}{(n-1)} \quad (10b)$$

$$V_c^* = (S_{c01}.d_{01} + S_{c1}.d_1 + S_{c2}.d_2 + S_{c02}.d_{02}).\frac{V_{dc}}{(n-1)} \quad (10c)$$

Now, the RHS of (1) becomes as (11) below.

$$(n-1).\left(V_a^* + V_b^*.e^{\frac{j2\pi}{3}} + V_c^*.e^{\frac{j4\pi}{3}}\right) =$$

$$V_{dc}.\left\{ \ d_{01}.\left(S_{a01} + S_{b01}.e^{\frac{j2\pi}{3}} + S_{c01}.e^{\frac{j4\pi}{3}}\right) \right.$$

$$+d_1.\left(S_{a1} + S_{b1}.e^{\frac{j2\pi}{3}} + S_{c1}.e^{\frac{j4\pi}{3}}\right)$$

$$+d_2.\left(S_{a2} + S_{b2}.e^{\frac{j2\pi}{3}} + S_{c2}.e^{\frac{j4\pi}{3}}\right)$$

$$\left. +d_{02}.\left(S_{a02} + S_{b02}.e^{\frac{j2\pi}{3}} + S_{c02}.e^{\frac{j4\pi}{3}}\right) \ \right\} \quad (11)$$

From (10) and (11), it is clear that (10) gives a particular solution to (11). It can also be seen that NLM is also a particular solution to SVM. Thus, it is possible to find the SVM duty cycles (d_{01}, d_1, d_2 and d_{02}) from the NLM duty cycles (D_a, D_b and D_c). Comparing (6) and (10) yields this relation in (12).

$$(S_{a01}.d_{01} + S_{a1}.d_1 + S_{a2}.d_2 + S_{a02}.d_{02}) = Q_a + D_a \quad (12a)$$

$$(S_{b01}.d_{01} + S_{b1}.d_1 + S_{b2}.d_2 + S_{b02}.d_{02}) = Q_b + D_b \quad (12b)$$

$$(S_{c01}.d_{01} + S_{c1}.d_1 + S_{c2}.d_2 + S_{c02}.d_{02}) = Q_c + D_c \quad (12c)$$

This calculation of the SVM duty cycles depends on the magnitude of D_a, D_b and D_c. If D_{max}, D_{mid} and D_{min} are the maximum, intermediate and minimum values among D_a, D_b and D_c, there are six possible combinations of D_a, D_b and D_c as shown in Table I. If $D_a \geq D_b \geq D_c$, then the switching states of phase A during $1-D_a$ and D_a are Q_a and Q_a+1. Since the values of S_{a01}, S_{a1}, S_{a2} and S_{a02} are either Q_a or Q_a+1 in one switching sequence, the LHS of (12) becomes:

$$Q_a.(d_{01} + d_1 + d_2 + d_{02}) + (d_1 + d_2 + d_{02}) = Q_a + D_a \quad (13a)$$

$$Q_b.(d_{01} + d_1 + d_2 + d_{02}) + (d_2 + d_{02}) = Q_b + D_b \quad (13b)$$

$$Q_c.(d_{01} + d_1 + d_2 + d_{02}) + (d_{02}) = Q_c + D_c \quad (13c)$$

These equations are only valid for the condition $D_a \geq D_b \geq D_c$. In general, for $D_{max} \geq D_{mid} \geq D_{min}$ for any of the phases, (13) can be rewritten as:

$$d_{01} = 1 - D_{max} \quad (14a)$$

$$d_1 = D_{max} - D_{mid} \quad (14b)$$

$$d_2 = D_{mid} - D_{min} \quad (14c)$$

$$d_{02} = D_{min} \quad (14d)$$

Fig. 5 and Fig. 6 show the variations of D_{max}, D_{mid} and D_{min} for a three-level inverter and the corresponding SVM duty cycles obtained using the proposed method. Here, the first and the last switching states have unequal duty ratios and in order to obtain a symmetrical switching sequence, the duty ratios d_{01} and d_{02} can be made equal as shown in (15).

$$d_{01} = d_{02} = 1 - D_{max} - D_{min} = d_0 \quad (15)$$

TABLE II
SWITCHING SEQUENCE DESIGN USING A SEQUENCE SELECTOR

k	d_{01}	d_1	d_2	d_{02}
1	$Q_a.Q_b.Q_c$	$Q_a+1.Q_b.Q_c$	$Q_a+1.Q_b+1.Q_c$	$Q_a+1.Q_b+1.Q_c+1$
2	$Q_a.Q_b.Q_c$	$Q_a+1.Q_b.Q_c$	$Q_a+1.Q_b.Q_c+1$	$Q_a+1.Q_b+1.Q_c+1$
3	$Q_a.Q_b.Q_c$	$Q_a.Q_b+1.Q_c$	$Q_a+1.Q_b+1.Q_c$	$Q_a+1.Q_b+1.Q_c+1$
4	$Q_a.Q_b.Q_c$	$Q_a.Q_b+1.Q_c$	$Q_a.Q_b+1.Q_c+1$	$Q_a+1.Q_b+1.Q_c+1$
5	$Q_a.Q_b.Q_c$	$Q_a.Q_b.Q_c+1$	$Q_a+1.Q_b.Q_c+1$	$Q_a+1.Q_b+1.Q_c+1$
6	$Q_a.Q_b.Q_c$	$Q_a.Q_b.Q_c+1$	$Q_a.Q_b+1.Q_c+1$	$Q_a+1.Q_b+1.Q_c+1$

TABLE III
SWITCHING FUNCTION VALUES AND SWITCH CONDITIONS

S_X	3 level	5 level
	X=(A, B, C)	
1	S_{X2}, S_{X3} ON	$S_{X2}, S_{X3}, S_{X6}, S_{X7}$ ON
2	S_{X2}, S_{X4} ON	$S_{X2}, S_{X3}, S_{X6}, S_{X8}$ ON
3	S_{X1}, S_{X4} ON	$S_{X2}, S_{X3}, S_{X5}, S_{X8}$ ON
4	-	$S_{X2}, S_{X4}, S_{X5}, S_{X8}$ ON
5	-	$S_{X1}, S_{X4}, S_{X5}, S_{X8}$ ON

B. Generalized Method for Switching Sequence Generation Using the Sequence Matrix

The sequence matrix is a matrix, which uses each of its column elements to create a valid switching sequence. In order to create a seven segment switching sequence, the sequence matrix should have seven columns, each of which represents a switching state in the space vector diagram. In each of these columns, the first, second and third elements represent the switching states of the three phases A, B and C, respectively. Thus, the sequence matrix in the proposed method has a size of 3x7. The algorithm generates the elements of the sequence matrix as indicated in section A. Using (8), the algorithm determines the starting switching state. Subsequently, the other switching states can be generated. The sequence matrix is updated at the start of each switching period by calculating the required switching states and arranging them for the current switching period. Since the initial switching state determines the switching sequence, selecting the redundant switching state results in a different sequence matrix and an alternate switching sequence.

As indicated in section A, the switching sequence generation is simple to carry out after identifying the switching state corresponding to the sub-hexagon center in which the reference vector lies. The switching sequence consists of four switching states from which it is possible to generate a seven segment switching sequence. The first switching state of the switching sequence is the switching state obtained from (8) and the remaining switching states are calculated by using the values of k as per the information provided in Table II. In the earlier example, since k=3 and the switching state is 211, the switching sequence is 211-221-321-322. Table II shows the switching sequence generation depending on the value of k. The seven-segment sequence(211-221-321-322-321-221-211) corresponding to these four switching states is generated using a sequence matrix.

This method of switching sequence generation is very suitable for real-time applications involving online computations. The rows of the sequence matrix (**Z**) represent each phase of a three-phase inverter and the columns of the matrix represent the current switching state of the inverter. Thus, the column elements of each row of the matrix **Z** are
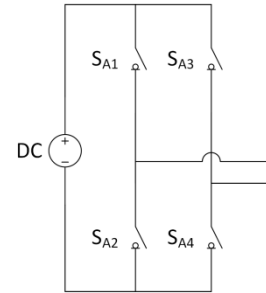

Fig. 7. Switch numbering followed for each H-bridge of the inverter. For additional H-bridges in the same phase (leg) the numbering is continuous.

essentially the switching function S_p of the inverter. If the switching functions S_a, S_b, and S_c are known, gate pulses can be generated using a switch matrix, as discussed in the next section. A sequence matrix **Z** for the sequence selector value k=3 in the earlier example for a modulation index of 0.8 is shown in (16).

$$\mathbf{Z} = \begin{bmatrix} 2 & 2 & 3 & 3 & 3 & 2 & 2 \\ 1 & 2 & 2 & 2 & 2 & 2 & 1 \\ 1 & 1 & 1 & 2 & 1 & 1 & 1 \end{bmatrix} \quad (16)$$

C. Generalized Switch Matrix for Gate Pulse Generation

In this paper, a matrix (**A**) is used to provide switching pulses to the gate driver circuit, which is a representation of the switching states of the individual switches of an inverter in a matrix form. The steps involved in the existing methods to provide pulses to the inverter are: (i) to determine the switching state, (ii) to decide which of the switches are to be turned *on* or *off*, and (iii) to provide corresponding logic pulses (0 or 1) to the switches. The introduction of a switch matrix helps to execute all these processes in a single step [28]. The dimensions of the switch matrix depend on the number of levels of the inverter. Since all of the classical multilevel inverter topologies use the same number of switches for a particular number of levels, only the elements of the switch matrix are different for different topologies.

The switch matrix generation for any *n*-level CHB inverter, having H bridges of equal dc link voltage, is discussed in this paper. In this case, the dimension of the switch matrix **A** are $(2*(n-1)) \times n$. This means that the number of rows of the switch matrix is equal to the number of switches

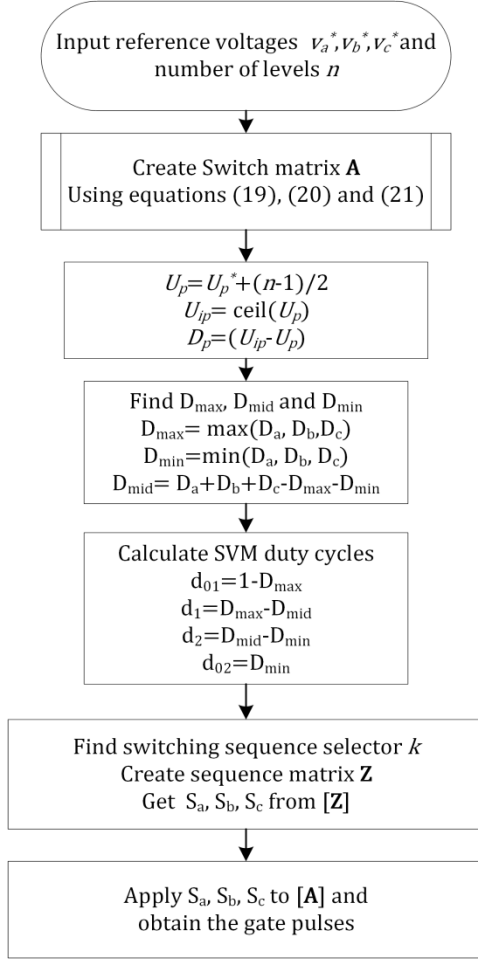Fig. 8. Complete flowchart for the proposed SVM scheme.

TABLE IV
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters	3 level	5 level
Bridge voltage, V_{dc}	50 V	50 V
Switching frequency, f_s	900 Hz	900 Hz
Modulation index, m_i	0.85	0.85
Balanced resistive load, R	50 Ω	50 Ω
Balanced inductive load, L	75 mH	75 mH

function value is *1*. The first element of each column represents the first switch of each inverter phase, and the last element of each column represents the last switch of each inverter phase. Thus, if the switching function value of the inverter phase is *3*, the algorithm selects the third column of the switch matrix and directly outputs the elements of that particular column to the gate driver circuit. The switching function values of a CHB inverter for three-level and five-level are given in Table III.

For the CHB topology, to generate a switch matrix, an intermediate switch matrix B is created. Then, it is extended to the actual switch matrix A. The intermediate switch matrix B is created in (19) and modified in (20). The variables i and j are varied from *1* to *(n-1)* and *1*to *n*, which represents the row and column numbers of the matrix.

$$B(i,j) = \begin{cases} 1\,; if\ j = 1\ \cap\ rem(i,2) = 0 \\ 0\,; if\ j = 1\ \cap rem(i,2) \neq 0 \\ 1\,; \qquad if\ j \neq 1\ \cap j = n \\ 0\,; \qquad if\ j \neq 1\ \cap j \neq n \\ B(i,j-1); if\ j \neq 1\ \cap i \neq 1 \end{cases} \quad (19)$$

$$B(i,j) =$$

$$\begin{cases} B(i,j-1) - 1\,; if\ (i+j) = (n+1)\ and\ i\ is\ even \\ B(i,j-1) + 1\,; if\ (i+j) = (n+1)and\ i\ is\ odd \end{cases} \quad (20)$$

Now, the actual switch matrix for any n-level CHB inverter is as shown in (21). Here, if l and m are the row and column numbers of the switch matrix, l varies from *1* to *2(n-1)* and m varies from *1* to *n*.

$$A(l,m) = \begin{cases} B((l+1)/2\,,m); if\ rem(l,2) \neq 0 \\ 1\,; if\ rem(l,2) = 0 \cap B(l/2,m) = 0 \\ 0\,; if\ rem(l,2) = 0 \cap B(l/2,m) \neq 0 \end{cases} \quad (21)$$

When the number of levels of an inverter (*n*) changes, equations (7) and (18) are affected and the algorithm outputs the corresponding pulses for the particular level number. Thus, the algorithm can be used without any modification or additional computational complexity for any number of inverter levels. In this case, the linear range of the modulation index is from 0 to 1. A flowchart for the complete algorithm is shown in Fig. 8.

present in each inverter leg (or phase) and that the number of columns of the switch matrix is equal to the number of levels, *n* (or the number of switching states) of the inverter. Three-level and five level CHB switch matrixes are shown in (17) and (18), respectively. The switches of the inverter H bridge module are numbered as shown in Fig. 7, and this is continued in the same order for additional H bridge modules as the number of levels increases.

$$A_{3L} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix} \quad (17)$$

$$A_{5L} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 \end{bmatrix} \quad (18)$$

In the above matrix (18), the first column represents the individual switch conditions when the inverter switching
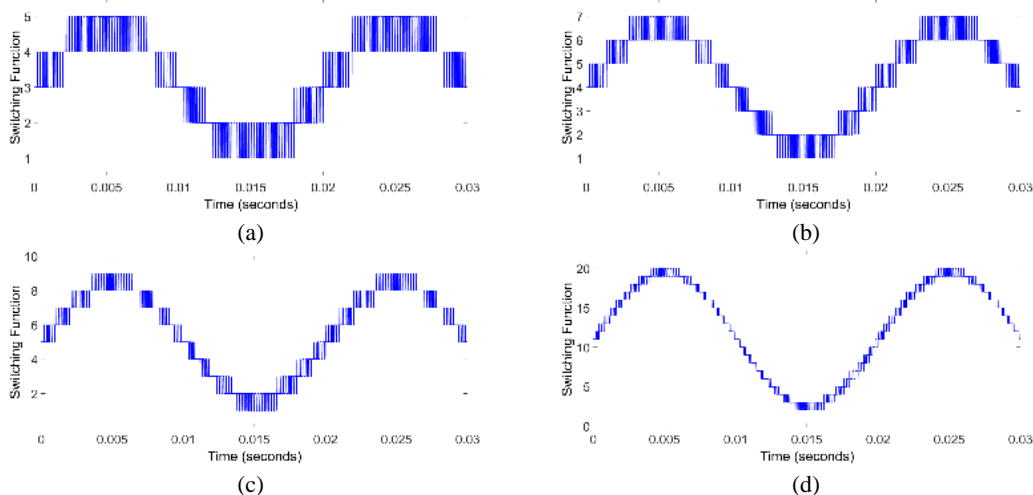
Fig. 9. Switching functions of: (a) five-level; (b) seven-level; (c) nine-level; (d) 21 level inverter.
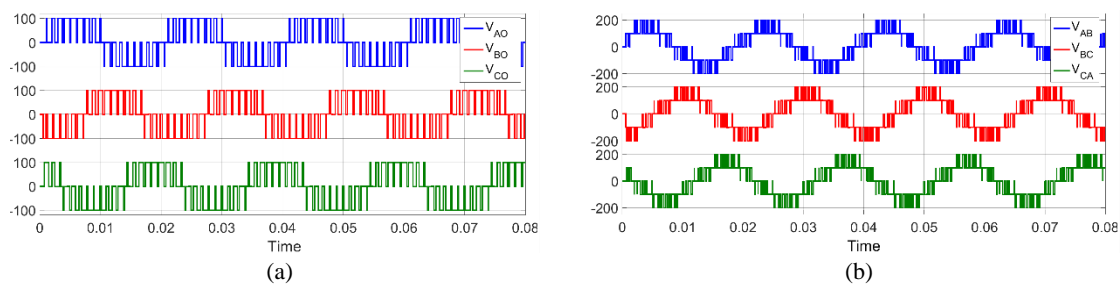

Fig. 10. Pole voltages of CHB inverters at a modulation index of 0.85: (a) three-level; (b) five-level.
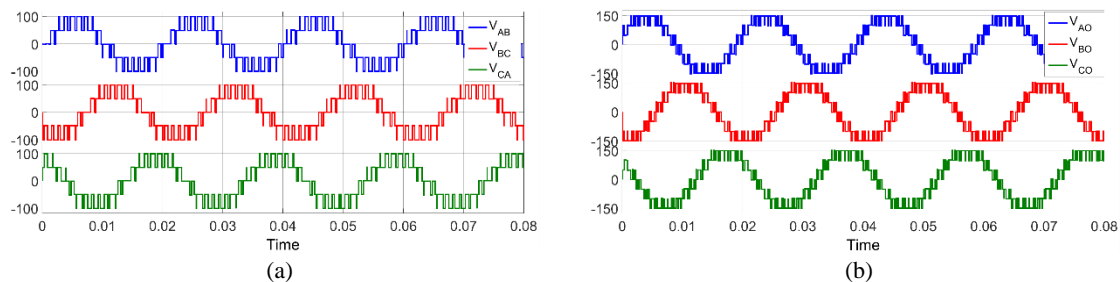

Fig. 11. Line voltages of CHB inverters, at a modulation index of 0.85: (a) three-level; (b) five-level.

IV. RESULTS AND DISCUSSIONS

A. Simulation Results

In order to show the effectiveness of the proposed algorithm for an n-level CHB inverter, the switching functions of five, seven, nine and 21 level inverters are shown in Fig. 9 (a), (b), (c) and (d). The switching function is an exact replica of the pole voltage of a multilevel inverter. Since a nine-level inverter pole voltage has nine levels, the switching function of the nine-level inverter also has nine levels from 1 to 9. Generally, an n-level inverter switching functions has 1 to n levels.

A three-phase CHBI for three-level and five level topologies is simulated with the parameters in Table IV. The simulated output pole voltages for the three and five level inverters are
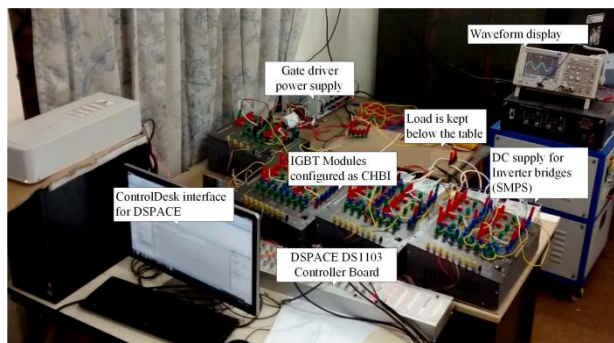
Fig. 12. Photograph of the experimental setup.

shown in Fig. 10 (a) and (b). The simulated output line voltages for the three and five level inverters are shown in Fig. 11 (a) and (b). The pole voltage is measured between the

(a)   (b)   (c)
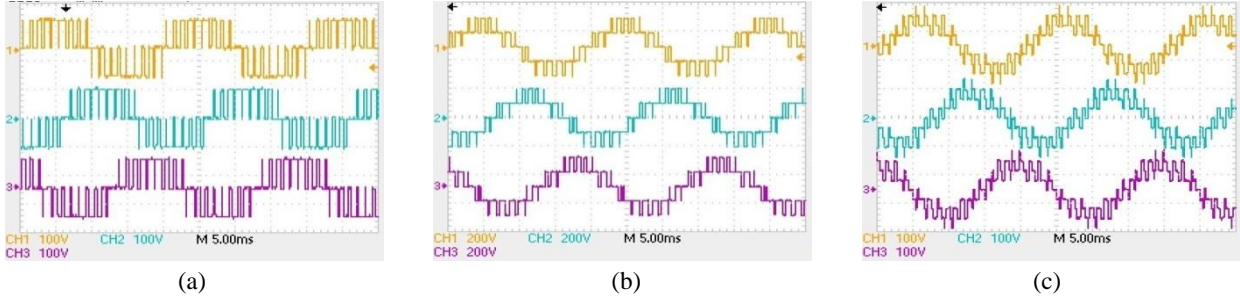
Fig. 13. Experimental results in a three-level CHBI for: (a) pole voltages; (b) line voltages; (c) phase voltages.

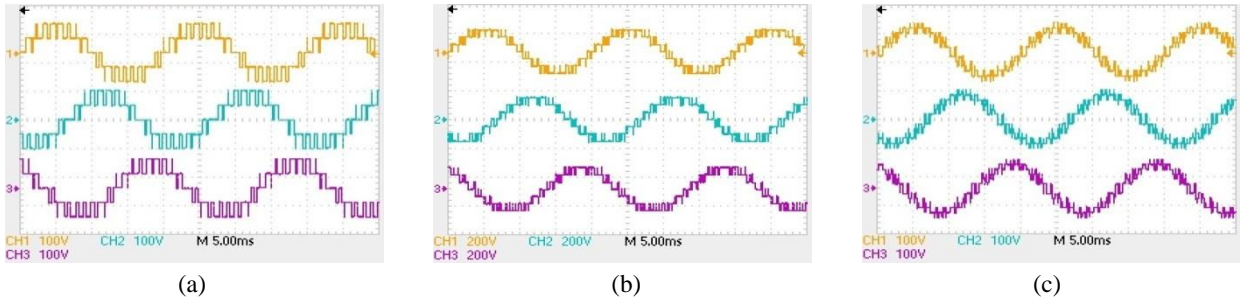(a)   (b)   (c)

Fig. 14. Experimental results in a five-level CHBI for: (a) pole voltages; (b) line voltages; (c) phase voltages.
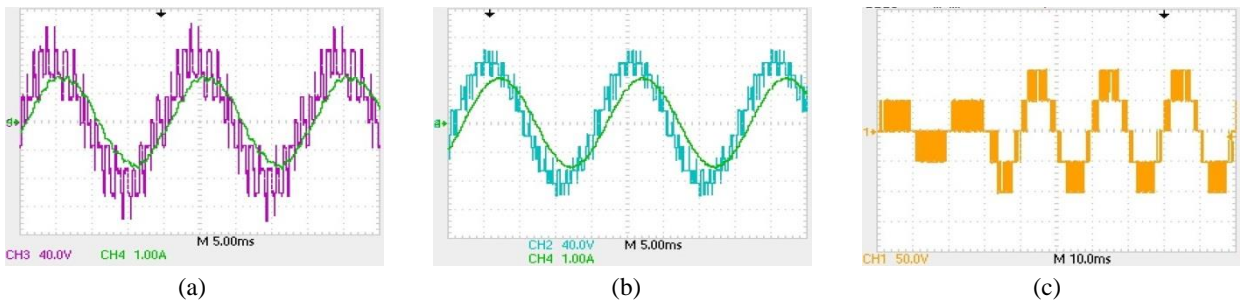

(a)   (b)   (c)

Fig. 15. Experimental results for phase voltage (CH1) and its corresponding phase current (CH2) for: (a) three-level CHBI; (b) five-level CHBI; and (c) variation inthe pole voltage of a five-level CHB inverter while the modulation index is varied from 0.2 to 0.9.

phase terminal and the common point (which connects all of the bottom H bridges in each phase).

B. Experimental Results

A laboratory prototype of a three-level, three phase CHB inverter with three individual H bridges (cells) is set up with the parameters shown in Table IV. Fig. 12 shows a photograph of the experimental setup. A dSPACE DS 1103 controller board is used to implement the algorithm and to generate the gate pulses. Fig. 13(a) shows experimental results pertaining to the pole voltages, Fig. 13(b) shows the line voltages, and Fig. 13(c) shows the phase voltages. The phase voltage is measured between the phase terminal and the neutral point of the star connected RL load. For the purpose of illustrating the generalized algorithm, a three-phase, five-level CHB inverter with six individual H bridges is set up with the parameters listed in Table IV. Experimental results, with the same RL load in the earlier case, for the pole voltages, line voltages and phase voltages are shown in Fig. 14(a), Fig. 14(b) and Fig. 14(c), respectively. Experimental results for the phase

voltage and the corresponding phase current for athree-level inverter and a five-level inverter are shown in Fig. 15(a) and Fig. 15(b), respectively.

The proposed algorithm is suitable for online variation of the modulation index. A five-level CHB inverter is subjected to an online variation of the modulation index while keeping the individual H bridge dc link voltage at 50V. In Fig. 15(c), the variation of the pole voltage of afive-level inverter is shown while the modulation index is varied from 0.2 to 0.9. The modulation index is varied from 0.1 to 0.995 in steps of 0.1, and the corresponding line voltage THD is plotted against the modulation index for both three-level and five-level inverters as shown in Fig. 16. In this case, the switching frequency is kept constant at 900 Hz.

C. Comparison with Existing Methods

The proposed algorithm is compared with existing SVM algorithms to demonstrate its improved time and space complexity. A generalized algorithm based on the two-level inverter (TI-SVM) in [21] and a generalized method based on

TABLE V
COMPARISON OF THE TIMER TASK TURNAROUND TIME

SVPWM scheme	Timer task turnaround time in μs	
	3 level	5 level
Proposed method	1.77	1.89
TI-SVM [21]	2.79	3.00
LF-SVM [25]	3.00	4.20

TABLE VI
COMPARISON OF THE MEMORY REQUIREMENT

SVPWM scheme	Total memory requirement in bytes		
	3 level	5 level	7 level
Proposed method	3864	4308	4806
TI-SVM [21]	11943	37845	50271
LF-SVM [25]	10341	12207	14112

TABLE VII
COMPARISON OF LINE VOLTAGE THD

SVPWM scheme	Line voltage THD in %	
	3 level	5 level
Proposed method	35.2	21.2
TI-SVM [21]	38.8	22.5
LF-SVM [25]	36	21.4

the *l-factor*(LF-SVM) approach in [25] are considered for comparison. All of the methods are implemented separately in the same controller board (dSPACE DS 1103) in the single timer task mode, and the turnaround time for the timer task is observed. The results in Table V show that the proposed method is superior when compared to the other methods in terms of execution time. In addition, the increase in the number of levels of the inverter does not really affect the proposed method. Fast processors are needed for algorithms with higher execution times. This increases the cost of the control circuit for the inverter. Hence, the proposed method with its shorter execution time is responsible for the cost saving aspect.

In order to find the memory requirements for the generated code in the processor, the three algorithms are implemented on a dSPIC 33EP512MU810 microprocessor using the MPLAB X IDE environment. The total memory usage for the code is observed for three-level, five-level and seven-level inverters. The results of this comparison are shown in Table VI. It is noted that the proposed algorithm takes up a lot less memory when compared to the other algorithms, even at a higher number of levels. This also improves the cost saving since a low-cost processor with less memory can be effectively used to implement the proposed scheme.

Another advantage of the proposed SVM is the suitability of the algorithm for real-time applications. This is largely due to its shorter execution time. The dynamic response of the system in Fig. 15(c) establishes this fact. A comparison of the load dynamic response in simulations of the proposed method
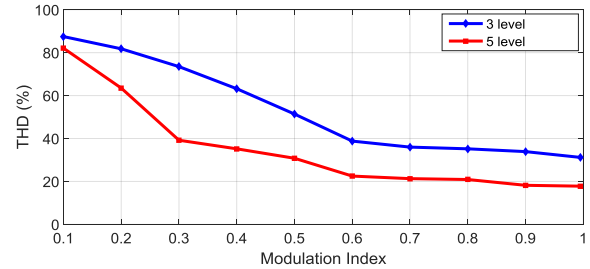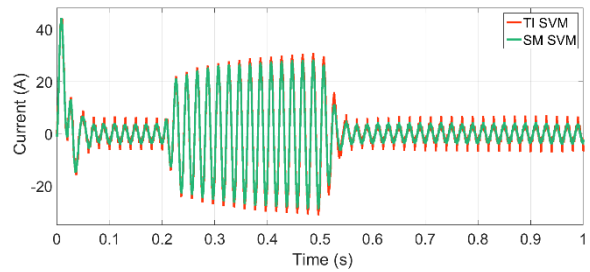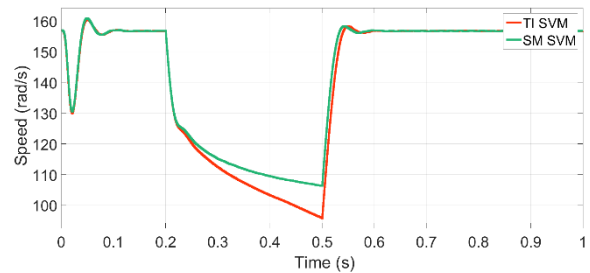

Fig. 16. Experimental results of line voltage THD vs. modulation index.

(a)

(b)

Fig. 17. Comparison of the dynamic load response of the proposed switch matrix based SVM (SM SVM) and the two-level inverter based SVM (TI SVM) in [21]: (a) Stator current comparison; (b) Speed comparison.

and the method in [25] reveals that the system response of the proposed method is comparable with that of the existing method. Here, a three-phase induction motor (4 kW, 400V, 50 Hz, 1430 rpm) is connected to the inverter as the load. The mechanical torque is varied from zero to 30 Nm at 0.2 s and then back to zero from 30 Nm at 0.5 s. The variation in the speed of the motor is observed (Fig. 16(a)) and it is found to be slightly better than the dynamic response of the two-level inverter based SVM method (Fig. 16 (b)) proposed in [21]. A comparison of THD measurements of the line voltage (with the parameters listed in Table IV) for a three-level inverter and a five-level inverter is shown in Table VII. It shows that the proposed SVM is comparable to the existing methods.

V. CONCLUSIONS

A generalized space vector modulation for a cascaded H bridge inverter using the concept of nearest level modulation is proposed in this paper. The algorithm depends on simple arithmetic and logic operations, which are easy to implement.

The algorithm presents a generalized method that is applicable to any n-level inverter for calculating the duty ratio and generating switching states without determining the sectors and triangles. Another advantage of the proposed scheme is the generation of a seven segment switching sequence with the use of a sequence matrix, which is also generalized for any n-level inverter. The gate pulses for a CHBI are generated with the help of a generalized switch matrix, which is not present in any of the existing SVPWM methods. Thus, depending on the value of *n* (the number of levels), the proposed algorithm calculates the duty cycles, generates the switching sequence and outputs gate pulses. Online variation of the modulation index is possible with the proposed method due to its reduced time and space complexity. The proposed scheme has been realized for three-level and five-level CHB inverter topologies with the only change being the value of *n* given as an input to the algorithm.

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Pratheesh K. J. received his B..Tech. degree in Electrical and Electronics Engineering from Kerala University, Kerala, India, in 2009;and his M..Tech. degree in Electrical Engineering from the National Institute of Technology Calicut, Calicut, India, in 2012, where he is presently working towards his Ph.D. degree in Electrical Engineering. His current research interests include power electronic circuits, pulse width modulation techniques and multilevel inverters.

Jagadanand G. received his B..Tech. degree in Electrical and Electronics Engineering from the University of Calicut, Calicut, India, in 1989; his M..Tech. degree in Electrical Engineering from the Regional Engineering College Calicut (CREC), Calicut, India, in 1991;and his Ph.D. in Electrical Engineering from National Institute of Technology Calicut, Calicut, India, in 2013. He is presently working as an Assistant Professor in the Department of Electrical Engineering, National Institute of Technology Calicut. His current research interests include power electronic circuits and control, multilevel inverters, SMPS, fault detection and diagnosis, and induction motor drives.

Rijil Ramchand received his B. Tech. degree in Electrical and Electronics Engineering from Calicut University, Calicut, India, in 1996; and his M..E. and Ph.D. degrees from the Indian Institute of Science, Bangalore, India, in 2002 and 2010, respectively. He is presently working as an Associate Professor in the Department of Electrical Engineering, National Institute of Technology Calicut, Calicut, India. His current research interests include power converters, pulse width modulation techniques, multilevel inverters and current controlled ac drives. He is a Senior Member of IEEE.