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Analyzing and Designing a Current Controller for Circulating Current Reduction in Parallel Three-Phase Voltage-Source Inverters

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Abstract

A circulating current is a major problem caused by directly connecting voltage-source inverters (VSIs) in parallel. This circulating current occurs as a zero-sequence current between the inverters by specific switch states. Several studies have presented alternatives using hardware and software methods. When coupled inductors (CIs) are employed for the high-frequency circulating current, a controller is required to prevent the low-frequency circulating current from saturating the CIs. In this study, the zero-sequence circulating current and its alternatives are investigated using hardware and mathematical description. A high-performance circulating current controller is proposed by applying a repetitive controller to the zero-sequence current control loop. The proposed controller can effectively minimize the low-frequency circulating current without any data sharing between the inverters in unfavorable conditions. It can also be applicable to the modular configuration of parallel three-phase VSIs. Experimental results verify the performance of the proposed controller.

Key words: Circulating current, Parallel operation, Voltage source inverter (VSI)

I. INTRODUCTION

Low-carbon energy technology was developed to solve the environmental pollution caused by the increase in energy consumption. To further this cause, distributed generation (DG), a system based on renewable energy resources such as wind turbine and photovoltaics, was developed [1]. As the power ratings of DG increase to support energy consumption, high-power voltage-source inverters (VSIs) are needed to deal with the full-scale power needed for grid connection. In high-current applications, a parallel connection of the VSIs is required because of certain limitations, such as the switching device and economic aspects [2].

Previous studies have been conducted on the circulating current for direct parallel three-phase VSIs [3]-[5]. In these papers, the circulating current is divided into two categories: zero-sequence circulating current (ZSCC) and non-zero-sequence circulating current (NZSCC) (i.e., cross current). Ogasawara et al. [4] introduced the cross and zero-sequence currents as circulating currents and the relationship between switching patterns and these currents. Both currents are differently controlled to maintain the average values at zero at all times. Yoshikawa et al. [5] suggested equivalent circuits for the motor, cross, and zero-sequence currents, which were separated by mathematical manipulation and controlled by independent controllers. Pan and Liao [3] proposed a definition and averaged model for the circulating current. The authors considered ZSCC and NZSCC and suggested a coordinate control method for positive-, negative-, and zero sequence currents. However, Pan and Liao [3] only cited the ZSCC with a different current sharing in the same hardware configuration (i.e., direct parallel three-phase VSIs). These studies [3]-[5] caused confusion about the components of a true circulating current. Other researchers [1], [6], [7] only considered the circulating current as the ZSCC, whereas the

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NZSCC was not mentioned. Moreover, these papers proposed methods for reducing the ZSCC with an open- or closed-loop control. Although the NZSCC (i.e., cross-current) was cited as the circulating current, considering the various cases of current sharing was not sensible [8], [9]. The NZSCC is represented by the difference in inverter currents [10]-[13]. The average value of the difference between inverter currents is controlled to zero in the case of equal current sharing. However, if current sharing is different, then the difference between the inverter currents is always present. Therefore, if the NZSCC is the circulating current, then it flows from one inverter to another. For instance, parallel inverters 1 and 2 are individually burdened with 30 and 10 A, respectively, for a total current of 40 A. This circulating current (i.e., 20 A) will affect the system's stability, current quality, and efficiency. However, results showed that it does not cause any problems by controlling the ZSCC for the circulating current. Consequently, the NZSCC is only a difference in the inverter currents, not the circulating current. The sequence of the inverter currents in the three-phase system for the circulating current likewise warrants a discussion. Generally, the components of the three-phase system can be classified as positive, negative, and zero sequence. On the one hand, the positive and negative components are balanced, and the sum of these components is zero. On the other hand, the zero-sequence components are in phase(i.e., zero-phase displacement), the sum of which has a certain value, not zero. Fundamentally, the states of the inverter switches are determined for the desired positive-sequence current of each inverter.

In other cases, positive- and negative-sequence currents could be desirable when the grid voltages are unbalanced. These cases call for balanced, instead of zero-sequence, currents. From this point of view, undesired and unintended circulating currents can be regarded as currents, except for balanced currents. Therefore, we conclude that the circulating current of direct parallel three-phase VSIs is zero sequence [20]. This means that ZSCC is only considered a circulating current.

In this study, ZSCC and its alternatives are investigated using hardware and mathematical description. A high-performance circulating current controller is proposed in which a repetitive controller (RC) is applied to the zero-sequence current control loop. The proposed controller can effectively minimize the low-frequency circulating current without any data sharing between inverters in unfavorable conditions.

The rest of the paper is organized as follows. Section II provides an analysis of the zero-sequence circulating current. Section III describes the design of the current controller with the ZSCC control algorithm. Section IV introduces the simulated and experimental results, which are based on the proposed controller with respect to conventional methods. Finally, Section V concludes.

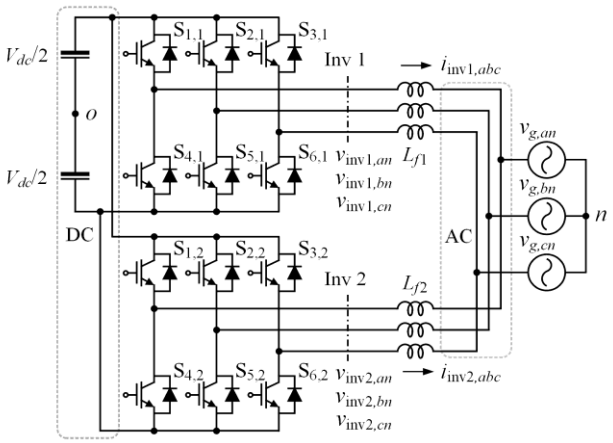

Fig. 1. Direct parallel three-phase VSIs.

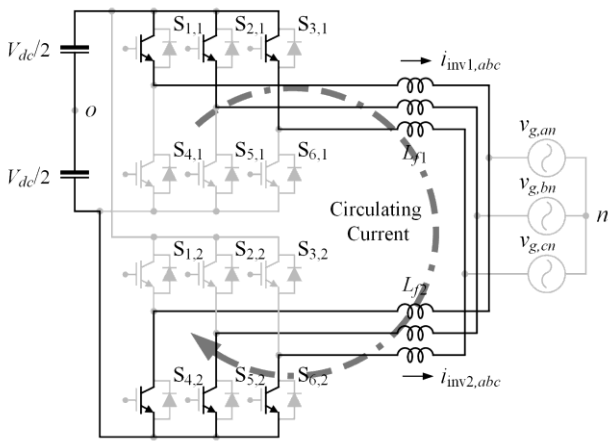

Fig. 2. Path of the circulating current via lower switches of inverter 1 and lower switches of inverter 2.

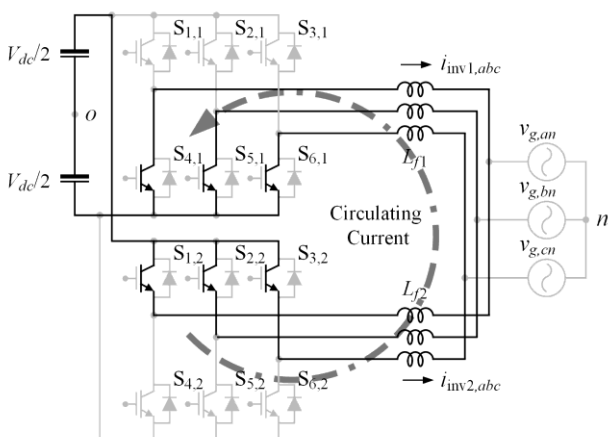

Fig. 3. Path of the circulating current via upper switches of inverter 1 and lower switches of inverter 2.

II. Analysis of Circulating Current

A. Zero-sequence Circulating Current

Fig. 1 shows a configuration of direct parallel three-phase VSIs for grid-connected application. The AC terminals of the

inverters are connected in parallel through filter inductors (i.e., L_{f1} and L_{f2} for inverters 1 and 2, respectively). The DC terminals are also connected in parallel. These connections develop a path for the circulating current between inverters. The pairs of switches that generate the circulating current in Fig. 1 are as follows:

$$\begin{aligned}&\text{Phase A: } [S_{1,1};S_{4,2}] \text{ or } [S_{4,1};S_{1,2}]\\ &\text{Phase B: } [S_{2,1};S_{5,2}] \text{ or } [S_{5,1};S_{2,2}].\\ &\text{Phase C: } [S_{3,1};S_{6,2}] \text{ or } [S_{6,1};S_{3,2}].\end{aligned} \tag{1}$$

Figs. 2 and 3 present the respective conditions and paths of the circulating current. These currents only occur in the one phase or simultaneously in the two and three phases. For the mathematical description, the voltage equations of the inverters connected to the grid in Fig. 1 are given as follows:

$$\begin{aligned}v_{inv1,an} &= L_{f1}\frac{di_{inv1,a}}{dt} + R_{f1}\cdot i_{inv1,a} + v_{g,an}\\ v_{inv1,bn} &= L_{f1}\frac{di_{inv1,b}}{dt} + R_{f1}\cdot i_{inv1,b} + v_{g,bn}\\ v_{inv1,cn} &= L_{f1}\frac{di_{inv1,c}}{dt} + R_{f1}\cdot i_{inv1,c} + v_{g,cn}\end{aligned} \tag{2}$$

$$\begin{aligned}v_{inv2,an} &= L_{f2}\frac{di_{inv2,a}}{dt} + R_{f2}\cdot i_{inv2,a} + v_{g,an}\\ v_{inv2,bn} &= L_{f2}\frac{di_{inv2,b}}{dt} + R_{f2}\cdot i_{inv2,b} + v_{g,bn}\\ v_{inv2,cn} &= L_{f2}\frac{di_{inv2,c}}{dt} + R_{f2}\cdot i_{inv2,c} + v_{g,cn}\end{aligned}, \tag{3}$$

where $v_{\text{inv1},an}$, $v_{\text{inv1},bn}$, and $v_{\text{inv1},cn}$ are the output voltages of inverter 1, while $v_{\text{inv2},an}$, $v_{\text{inv2},bn}$, and $v_{\text{inv2},cn}$ are the output voltages of inverter 2. L_{f1} and L_{f2} are the filter inductances of inverters 1 and 2, respectively. $i_{\text{inv1},a}$, $i_{\text{inv1},b}$, and $i_{\text{inv1},c}$ are the currents of inverter 1, while $i_{\text{inv2},a}$, $i_{\text{inv2},b}$, and $i_{\text{inv2},c}$ are the currents of inverter 2. $v_{g,an}$, $v_{g,bn}$, and $v_{g,cn}$ are grid voltages. The parasitic resistance of filter inductors R_{f1} and R_{f2} is neglected in Fig. 1 and will be omitted in further descriptions.

To further investigate the circulating current, inverter currents $i_{\text{inv1},x}$ and $i_{\text{inv2},x}$ are classified into those for power flow (i.e., balanced currents) and circulating current (i.e., unbalanced currents). The subscript "x" denotes phases a, b, and c. Therefore, the inverter currents are given as follows:

$$\begin{aligned}i_{inv1,x} &= i_{pow1,x} + i_{cir,x}\\ i_{inv2,x} &= i_{pow2,x} - i_{cir,x}\end{aligned}, \tag{4}$$

where $i_{pow1,x}$ and $i_{pow2,x}$ are the currents for the power flow, and $i_{cir,x}$ is the circulating current between inverters. These currents are depicted by the single-phase representation in Fig. 4. Given that the circulating current occurs as the difference in inverter voltages, this difference is obtained by the subtraction of Equations (2) and (3).

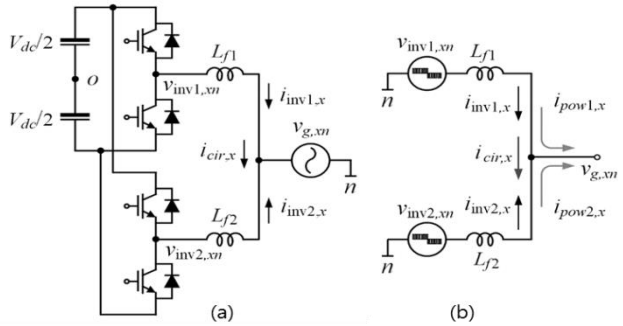

Fig. 4. Single phase of directly connected parallel VSIs.

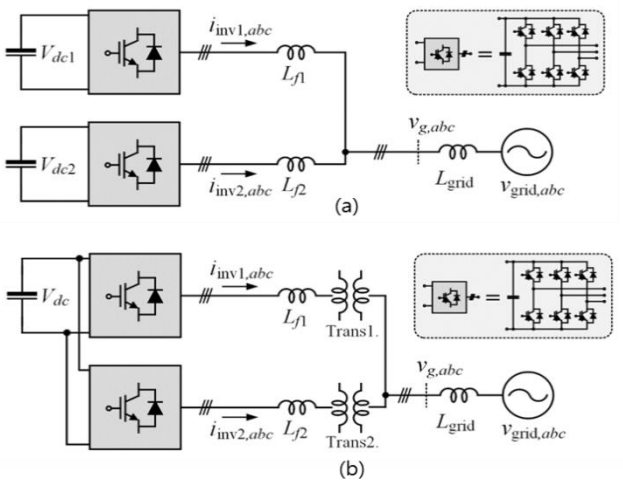

Fig. 5. Methods for removing the path of the circulating current.

$$v_{inv1,xn} - v_{inv2,xn} = L_{f1}\frac{di_{inv1,x}}{dt} - L_{f2}\frac{di_{inv2,x}}{dt}. \tag{5}$$

Assuming that L_{f1} and L_{f2} are equal to each other as in L_f, Equation (5) becomes

$$v_{inv1,xn} - v_{inv2,xn} = L_f\frac{d\left(i_{inv1,x} - i_{inv2,x}\right)}{dt}. \tag{6}$$

To investigate the circulating current as a zero sequence, Equation (6) is extended to the three-phase system. The difference equation of the zero-sequence voltage is obtained by

$$v_{inv1,zn} - v_{inv2,zn} = L_f\frac{d\left(i_{inv1,z} - i_{inv2,z}\right)}{dt}, \tag{7}$$

where

$$\begin{aligned}v_{inv1,zn} &= \left(v_{inv1,an} + v_{inv1,bn} + v_{inv1,cn}\right)/3\\ v_{inv2,zn} &= \left(v_{inv2,an} + v_{inv2,bn} + v_{inv2,cn}\right)/3\\ i_{inv1,zn} &= \left(i_{inv1,a} + i_{inv1,b} + i_{inv1,c}\right)/3\\ i_{inv2,zn} &= \left(i_{inv2,a} + i_{inv2,b} + i_{inv2,c}\right)/3\end{aligned}.$$

In addition, according to the defined currents in Equation (4), the zero-sequence currents of the inverters can be modified as those in the ZSCC in inverters 1 and 2, with the assumption that the currents for the power flow are balanced.

$$i_{inv1,z} = \frac{i_{cir,a} + i_{cir,b} + i_{cir,c}}{3} = i_{cir,z} \quad (8)$$

$$i_{inv2,z} = -\frac{i_{cir,a} + i_{cir,b} + i_{cir,c}}{3} = -i_{cir,z}. \quad (9)$$

Equations (8) and (9) result in

$$i_{inv1,z} = -i_{inv2,z} = i_{cir,z}\ . \quad (10)$$

The result shows that ZSCC is a complete zero-sequence current of the inverters. Lastly, Equation (7) can be rearranged in terms of the ZSCC.

$$\frac{di_{cir,z}}{dt} = \frac{v_{inv1,zn} - v_{inv2,zn}}{2L_f} \quad (11)$$

Equation (11) shows that the ZSCC occurs as a difference in the zero-sequence inverter voltages $v_{inv1,zn} - v_{inv2,zn}$, and its amplitude is determined by the sum of the filter inductances $2L_f$ for the inverters. Therefore, if the filter inductances cannot sufficiently suppress the circulating current, then the stability of the direct parallel three-phase VSIs is not guaranteed.

B. Alternative Methods for ZSCC

Alternatives for the ZSCC have been presented in many papers. The methods are generally classified into hardware and software.

In direct parallel three-phase VSIs, ZSCC flows through the connection of the DC- and AC-side terminals. Therefore, DC- or AC-side disconnection can be a means of removing the pathway for ZSCC (i.e., galvanic isolation). DC-side isolation is achieved using a separated DC source, as shown in Fig. 5(a), or connecting the AC output terminals of individual inverters to each AC isolation transformer, as shown in Fig. 5(b). These procedures are effective approaches to removing the ZSCC. However, as a result, the system volume becomes bulky and additional electrical components increase the costs. Meanwhile, high impedance is inserted on the ZSCC path for the high-frequency circulating current.

The presented software methods reduce ZSCC by modifying the zero-sequence signals of inverters. The difference in zero-sequence signals between modulation signals of the inverters were removed by mathematical manipulation [7] or modification of space vector PWM (SVM) [15], zero-sequence filter [14], harmonic elimination PWM (HEPWM), and selective harmonic elimination PWM (SHEPWM). Alternatively, proportional–integral (PI) [6], [9], [10], nonlinear, hysteresis [16], deadbeat controllers [9], and zero-vector feed-forward control strategy [8] were used for zero-sequence current feedback control (i.e., closed-loop methods). As aforementioned, other factors, except for the modulation signals obtained from the controllers, affect the circulating current. This condition means that open-loop methods cannot remove the circulating current effectively. Therefore, closed-loop methods (i.e., feedback control with the zero-sequence current) are recommended.

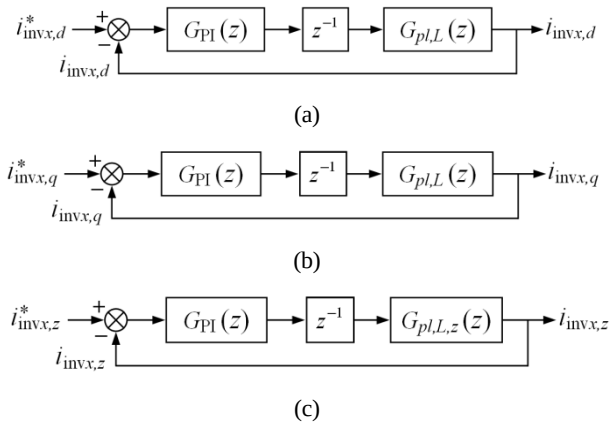

Fig. 6. Simplified block diagrams of conventional closed-loop current control in *z*-domain. (a) *d*-axis, (b) *q*-axis, and (c) *z*-axis current control loops.

III. CURRENT CONTROLLER DESIGN

A. Description of Current Controller for Parallel SVIs

Several papers have presented the controllers for ZSCC. In the case of different current sharing or filter parameters, the performance of conventional controllers for the ZSCC is degraded. Xueguang et al. [8], [9] proposed the feedforward strategy using non-zero vectors with the deadbeat or PI controller. However, this method should share the duty-cycle data of other inverters within the communication line. In this paper, a zero-sequence current controller that uses an RC with good performance and simple implementation is presented. This controller is needed to prevent the saturation of inserted coupled inductors from high impedance when the interleaving is applied. The currents in the synchronous reference frame are controlled by the PI controller, whereas the zero-sequence current is controlled by the PI controller in the *z*-axis [6], [8]. The zero-sequence current is also controlled by various kinds of controllers, such as nonlinear, hysteresis [16], and deadbeat [9].

Fig. 6 shows simplified block diagrams of conventional closed-loop control for the *dqz*-axis inverter currents in the *z*-domain. $G_{\mathrm{PI}}(z)$ is the PI controller and is discretized by a backward transformation.

$$G_{PI}(z) = K_P + K_i \frac{T_s z}{z-1}, \quad (12)$$

where K_p is the proportional gain, K_i is the integral gain, and T_s is the sampling frequency. z^{-1} is the computation delay, and transfer functions $G_{pl,L}(z)$ and $G_{pl,L,z}(z)$ are discretized by the zero-order hold method for PWM delay. These delays should be considered in designing the controller in a digital control system. According to Equations (2), (3), and (11),

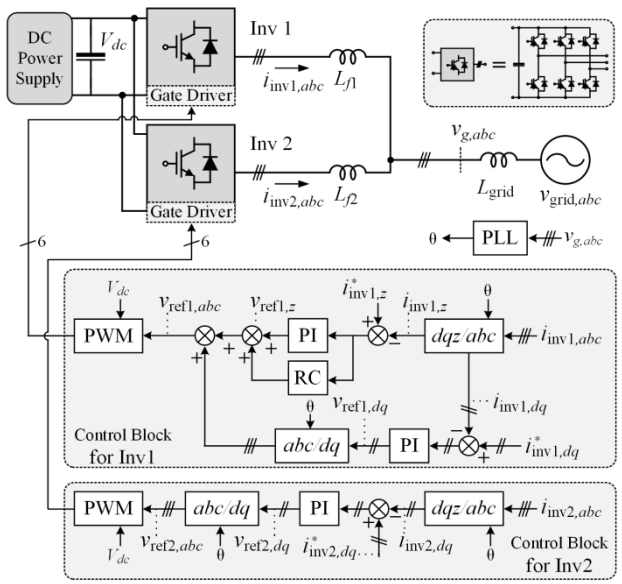

Fig. 7. Proposed current controller for parallel three-phase VSIs.

transfer functions from inverter voltages to currents in Fig. 6 are given by

$$G_{pl,L}(z) = \frac{T_s}{(z-1)L_{f,x}} \tag{13.a}$$

$$G_{pl,L,z}(z) = \frac{T_s}{(z-1)(L_{f1}+L_{f2})}, \tag{13.b}$$

where $L_{f,x}$ is the filter inductance for inverters 1 and 2 (i.e., subscript x denotes 1 or 2).

Fig. 7 shows the proposed current controller for parallel three-phase VSIs. This controller considers the RC in the z-axis to control the zero-sequence current.

B. Designing the Current Controller

The magnitude of the transfer function, such as delays (i.e., computation and PWM), is given by

$$\left|G_{pld}(z)\right| = \left|\frac{T_s}{z(z-1)L_f}\right|. \tag{14}$$

This can be approximated to K_p at the crossover frequency f_c (i.e., $\omega_c = 2\pi f_c$). The magnitude of the open-loop gain [i.e., $K_p\ G_{pld}(z)$] is unity at the crossover frequency. Hence, K_p is given by

$$K_p = \frac{2L_f\left|\sin\left(\frac{\omega_c T_s}{2}\right)\right|}{T_s}. \tag{15}$$

The crossover frequency determining the phase margin (PM) of the controller is typically restricted to be lower than the sampling frequency f_s after attenuation of high-frequency noise is considered. Therefore, crossover frequency can be calculated using the desired PM [17].

$$\omega_c = \frac{\pi/2 - PM}{3T_s/2}. \tag{16}$$

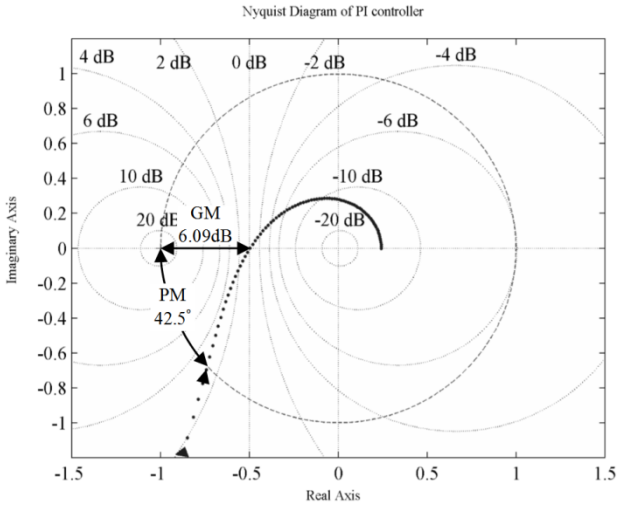

Fig. 8. Nyquist diagram of PI controller.

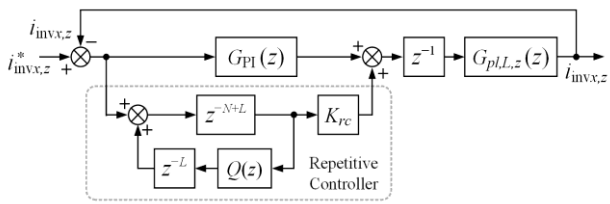

Fig. 9. Proposed ZSCC control loop.

Additionally, K_i has an effect on the PM. To prevent the PM from decreasing through K_i and simplify the controller design, the integral time constant T_i (=K_p/K_i) is calculated to ensure that its phase contribution is small at the crossover frequency.

$$T_i \approx \frac{10}{\omega_c}. \tag{17}$$

Fig. 8 shows the Nyquist diagram according to the PI controller design. The gain margin is 6.09 dB and the phase margin is 42.5°. This system is stable because the Nyquist diagram does not include the critical point (−1.0).

In this paper, the RC is employed to improve the performance of the controllers for each inverter in terms of control performance in the steady-state response and independence.

Fig. 9 shows the zero-sequence current control loop using the RC. The transfer function of the RC in Fig. 8 is given by

$$G_{RC}(z) = K_{rc}\frac{z^{-N+L}}{1 - z^{-N}\cdot Q(z)}, \tag{18}$$

where K_{rc} is the repetitive control gain, N is the ratio of the sampling frequency f_s to the alternating component of the z-axis f_z, L is the delay compensation factor, and $Q(z)$ is the low pass filter. $Q(z)$ is used to improve controller stability. Pure RC is critically stable due to a pole on the unit circle [19]. Therefore, $Q(z)$ satisfies the following condition.

$$\left|Q(z)\right| \le 1. \tag{19}$$

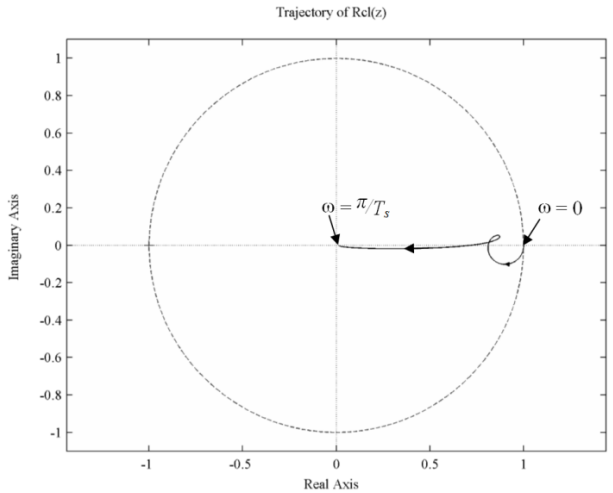

Fig. 10. Trajectory of $R_{cl(z)}$.

In most papers, non-causal finite impulse response filters were used for the zero-phase characteristics. This general form is given by

$$Q(z) = \sum_{i=0}^{m} \alpha_i z^{i} + \sum_{i=1}^{m} \alpha_i z^{-i}, \tag{20}$$

where α_i is the coefficient of the filter (i = 0,1, …, m; m = 0,1, …, N/2). A first-order filter is sufficient to ensure stability, and Equation (20) is simplified as follows:

$$Q(z) = \alpha_1 z + \alpha_0 + \alpha_1 z^{-1}. \tag{21}$$

According to Equation (19), coefficient α_i is determined by the following conditions:

$$2\alpha_1 + \alpha_0 = 1, \quad \alpha_0, \alpha_1 \rangle 0. \tag{22}$$

However, high-frequency periodic disturbances are not absolutely canceled by $Q(z)$. Therefore, a tradeoff is made between tracking performance and system stability.

z^{L} is the phase lead compensator for the delays in the plant and control loop. The compensator's main purpose is to improve system stability margins by introducing a leading action on the controller at periodic frequencies. Designing this parameter should be based on the number of delay samples, which well approximates the delay of transfer function at harmonic frequencies. A good approximation of the phase is about three sample periods.

Although the $Q(z)$ and L used for system stability and margin improvement are non-causal operators, the transfer function [Equation (18)] becomes implementable because pure RC uses previous values in the buffers. Delay compensation factor L is smaller than N (i.e., N > L).

To obtain repetitive control gain, a stability analysis should be conducted. The transfer function from the reference on the zero-sequence current $i_z^*(z)$ to the zero-sequence current $i_z(z)$ is given by

$$G_{cl,z}(z) = \frac{i_z(z)}{i_z^*(z)} = \frac{z^{-1}\left(G_{PI}(z) + G_{RC}(z)\right)G_{pl,z}(z)}{1 + z^{-1}\left(G_{PI}(z) + G_{RC}(z)\right)G_{pl,z}(z)}. \tag{23}$$

To simplify the stability analysis, the open-loop gain for PI controller is defined by

$$P(z) = z^{-1}G_{PI}(z)G_{pl,z}(z), \tag{24}$$

and the open-loop gain for RC is given by

$$R(z) = z^{-1}G_{RC}(z)G_{pl,z}(z). \tag{25}$$

Equation (23) can be modified with Equations (24) and (25) as follows:

$$G_{cl,z}(z) = \underbrace{\frac{1}{1+P(z)}}_{P_{cl}(z)} \underbrace{\frac{P(z)+R(z)}{1+\dfrac{R(z)}{1+P(z)}}}_{R_{cl}(z)}. \tag{26}$$

The poles of $P_{cl}(z)$ coincide with those of the PI control loop. Assuming that these poles yield a stable system, the overall stability analysis can be concluded by considering the remaining part of $R_{cl}(z)$. With this approach, the following conditions for system stability are presented.

1) If $|P_{cl}(z)| < 1$,
   then the closed-loop system without RC is stable.
2) If $|R_{cl}(z)| < 1$,
   then the closed-loop system, which consists of the PI controller and RC, is stable.

Fig. 10 depicts the trajectory of $R_{cl}(z)$. All frequency domains below the Nyquist frequency meet condition B. Therefore, the proposed system is stable.

The RC aims to compensate for the steady-state error. RC gain should be kept smaller compared to that of the PI controller, such that the slow dynamics of the RC does not influence the transient response. The gain of the PI controller coincides with that at approximately within and beyond the limit frequencies of the PI bandwidth. Therefore, selecting K_{rc} in the range of K_p/5–K_p/20 is recommended.

IV. Simulation and Experimental Results

A. Simulation Results

A series of simulations was carried out to verify the performance of the proposed controller by comparing the conventional controller in the zero-sequence current control loop.

Table I lists the simulation parameters. When current sharing and filter inductances vary, the modulation signals of individual inverters achieve differing values. This variation results in the difference in zero-sequence signals between inverters. The larger the difference in the sharing current and parameters, the worse the phenomenon. The low-frequency zero-sequence current cannot be fully controlled to zero using the PI controller because of this phenomenon. In the simulation, SVM is used for the PWM scheme. The differences in the setup of inverters 1 and 2 are as follows:

TABLE I
SI BASE UNITS

Parameters	SYMBOLS	Values
Total rated power	$P_{rated,tot}$	14 [kW]
Individual rated power	$P_{rated,ind}$	7 [kW]
Line-to-line voltage	$V_{grid,ll}$	190 [V]
Grid frequency	f_g	60 [Hz]
Total rated current	$i_{rated,tot}$	42.53 [A]
Individual rated current	$i_{rated,inv}$	21.27 [A]
DC link voltage	V_{dc}	380 [V]
Switching frequency	f_{sw}	8.4 [kHz]
Filter inductance	L_{f1}&L_{f2}	2 & 3 [mH]
Proportional gains	K_p	8 and 12
Integral gains	K_i	3000 and 4500

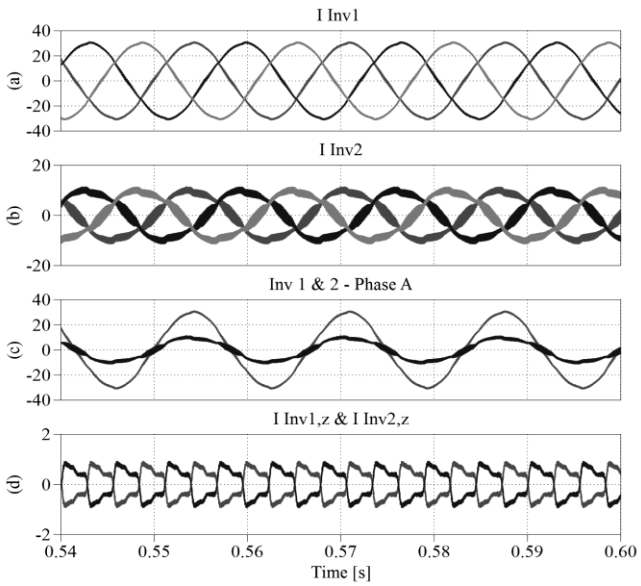

Fig. 11. Simulated waveforms with conventional ZSCC. (a) Currents of inverters 1. (b) Currents of inverters 2. (c) Inverter 1 and 2 currents in phase a. (d) ZSCC.

A. Inverter 1: L_{f1} = 2 mH, $i^*_{inv1,d}$ = 30 A

B. Inverter 2: L_{f2} = 3 mH, $i^*_{inv2,d}$ = 10 A

According to the varied filter inductances, PI controller gain is also applied as shown in Table I.

Fig. 11 shows that the ZSCC is retained using the conventional controller. Furthermore, the inverter currents are distorted by the remaining zero-sequence current.

To improve the steady-state response, RC is applied in parallel with the PI controller without any information of other inverters. The important parameters of RC are selected by

$$Q(z) = \frac{z^1 + 2 + z^{-1}}{4},\ L = 3,\ K_{rc} = 2. \quad (27)$$

Fig. 12 depicts the performance of the proposed controller.

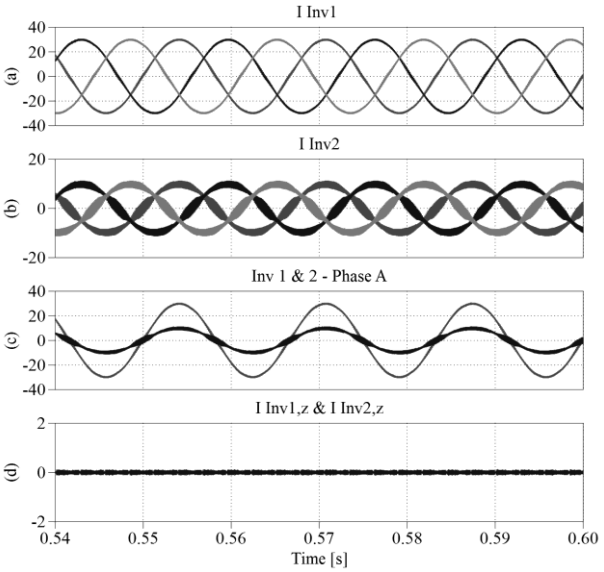

Fig. 12. Simulated waveforms with the proposed ZSCC. (a) Currents of inverters 1. (b) Currents of inverters 2. (c) Inverter 1 and 2 currents in phase a. (d) ZSCC.

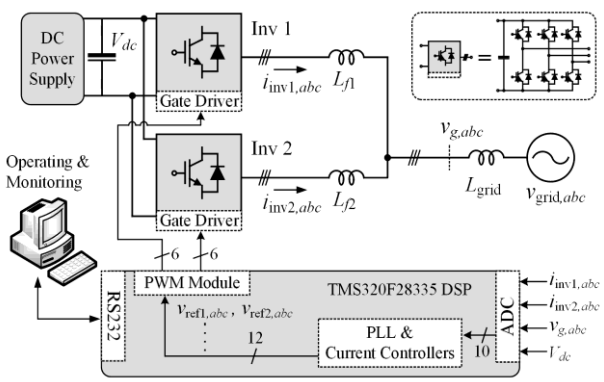

Fig. 13. Diagram of parallel three-phase VSIs with *L* filters.

Compared with the conventional controller, the low-frequency components of the zero-sequence current are almost removed. The inverter currents are improved by the reduction of the zero-sequence current as well.

B. Experimental Results

In this section, the proposed controller for the zero-sequence current is experimentally verified through comparison with the conventional controller. A prototype of the 14 kW parallel three-phase VSIs is used. Its specifications are the same as the parameters listed in Table I for the simulation. The prototype is controlled by a control platform composed of a digital signal processor (DSP).

Fig. 13 depicts the experimental setup. The carriers for inverters 1 and 2 are synchronized, and the experiments are equally performed by SVM with the simulation. To cause a large difference in the zero-sequence signals between inverters, two cases are experimented.

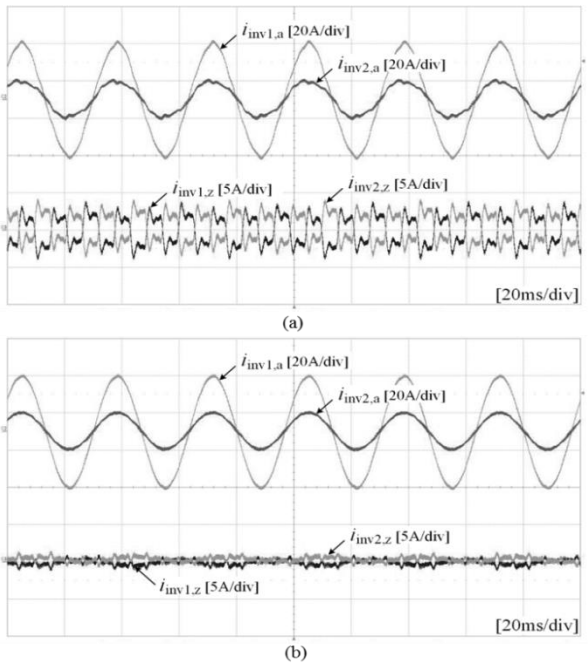

Fig. 14. Experimental result of the current waveforms. (a) Conventional controller. (b) Proposed controllers with the different current references($i^*_{inv1,d}$ =30 A, $i^*_{inv2,d}$ =10 A) and filter inductances(L_{f1} = 2 mH and L_{f1} = 3 mH).

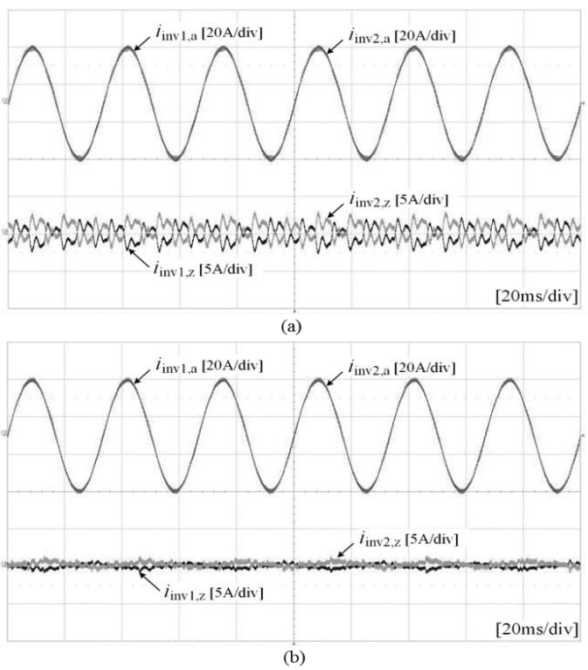

Fig. 15. Experimented current waveforms. (a) Conventional controller. (b) Proposed controllers with the same current reference ($i^*_{inv1,d}$ =30A, $i^*_{inv2,d}$ =30A) and different filter inductances(L_{f1} = 2 mH and L_{f1} = 3 mH).

Fig. 14 shows that the current references for both inverters are different as denoted by $i^*_{inv1,d}$ =30 A and $i^*_{inv2,d}$ =10 A with differences in filter inductance at L_{f1} = 2 mH and L_{f1} = 3 mH. Fig. 14(a) shows that the zero-sequence current flows severely when the conventional controller is used. The maximum peak value of the measured zero-sequence currents $i_{inv1,z}$ and $i_{inv2,z}$ is 4.21 A. Furthermore, both inverter currents are distorted by the remaining zero-sequence currents. However, as shown in Fig. 14(b), the zero-sequence current is considerably reduced by the proposed controller. Hence, the distortion of the inverter currents is improved. Other experiments with diverse filter inductances were also performed as shown in Fig. 15. The current references for inverters are also at 30 A and filter inductances at L_{f1} = 2 mH and L_{f1} = 3 mH.

Although the current references of both inverters are identical, the conventional controller does not sufficiently suppress the zero-sequence current, as shown in Fig. 15(a). For the further reduction of the zero-sequence current, the proposed controllers are applied as shown in Fig. 15(b), in which the remaining zero-sequence current is considerably suppressed by the proposed controller.

V. CONCLUSIONS

In this study, we based our understanding on circulating currents for parallel three-phase VSIs. A novel ZSCC controller that adopts the RC for parallel three-phase VSIs was proposed. The RC was employed to improve the reduction of the zero-sequence current and was experimentally verified. In addition, a complicated and high bandwidth communication system to meet the control period was unnecessary due to the no-sharing control data. A proposed controller for the zero-sequence current was experimentally verified after comparison with the conventional controller. A prototype of the 14 kW parallel three phase VSIs was used. Results showed that the proposed controller exhibits a good performance.

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