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# Development of a Switched Diode Asymmetric Multilevel Inverter Topology

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## Abstract

This paper presents a new asymmetrical multilevel inverter with a reduced number of power electronic components. The proposed multilevel inverter is analyzed using two different configurations: i) First Configuration (with a switched diode) and ii) Second Configuration (without a switched diode). The presented topologies are compared with recent multilevel inverter topologies in terms of number of switches, gate driver circuits and blocking voltages. The proposed topologies can be cascaded to generate the maximum number of output voltage levels and they are suitable for high voltage applications. Various power quality issues are addressed for both of the configurations. The proposed 11-level inverter configuration is simulated using MATLAB and it is validated with a laboratory based experimental setup.

**Key words:** Asymmetric cascaded multilevel inverter, Nearest level modulation, Reduced switches, Total harmonic distortion

## I. INTRODUCTION

In recent decades, multilevel inverters have come to play a major role and have received a lot of attention from industries in the field of power electronics, due to their modularity and high power capability. There are a number of conventional multilevel inverters. (i) The Cascaded H-Bridge (CHB) [1] multilevel inverter topology patent was recorded in 1970 by Baker. The CHB topology has a few advantages such as modularity, soft switching and that fact that it does not require any additional clamping diodes or capacitors. (ii) In 1975, Nabae introduced a Neutral Point Clamp (NPC) multilevel inverter [2]. The NPC has a high efficiency and reactive power control. It is more suitable for the bidirectional power flow applications in HVDC links. (iii) The Flying Capacitor (FC) [3] was introduced to overcome the challenges of balancing the voltage across the series connection of dc-link capacitors. It provides better voltage ride through capability and it can control both the real and reactive power.

The unique drawbacks of conventional multilevel inverters are an increase in the number of switches for increasing the number of levels, which in turn increases the complexity of the installation, the complexity of the switching pattern, the number of gate driver circuits and the size of the inverter layout [4]. Numerous new multilevel inverter topologies have been introduced by researchers to minimize the switch count, gate driver circuits, dc sources and the voltage rating of the switches. In [5], a new cascaded topology was proposed to increase the number of output voltage levels, and various algorithms have been introduced to determine the magnitude of DC sources. However, as the number of levels increases, it is necessary to have different voltage rating for the switches. The ladder structure multilevel inverter topology is presented in [6] with a reduced number of IGBTs and DC sources. A modular structured single dc source multilevel inverter without a transformer and with a low switching frequency is discussed in [7]. A basic module with a capacitor unit is proposed in [8]. This topology has good modularity and is applicable for high voltage applications with a minimized switch count. In [9], a novel transformer based topology was presented for high voltage applications. This topology is configured in an asymmetric method to produce the maximum output voltage levels. However, this topology requires a different transformer turns ratio which makes it difficult to construct. A seven level inverter with a reduced switch count is presented in [10]. A single dc source is used

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in this topology with three dc-link capacitors and a voltage balancing algorithm for the dc-link capacitor.

In these studies, many new multilevel inverter topologies are presented with the following objectives: a reduced number of switches, a reduced number of sources, an increased output voltage level, etc. In this paper a new structure for an asymmetic multilevel inverter topology is proposed with a reduced number of IGBTs as well as reduced dc sources and low blocking voltages across the switches. This topology is also capable of cascading to generate the maximum number of voltage levels and it is suitable for high voltage and medium power applications. A comparison of the proposed topology with recent multilevel inverters [11]-[20] is also presented.

## II. Proposed Fundamental 11-Level Inverter

A new 11-level multilevel inverter topology with two different configurations: with and without a switched diode is presented. A diagram of the proposed MLI with a switched diode is shown in Fig. 1. This fundamental module is divided into three parts namely the packed H-bridge, the right arm and the left arm. A single dc source is connected in the right arm while the left arm side consists of two dc sources, four dc-link capacitors ($C_1$-$C_2$) and ($C_3$-$C_4$), switch ($S_1$) and diode ($D_1$) as shown in Fig. 1. The packed H-bridge inverter consists of the switches ($S_2$-$S_5$), the upper switch ($S_U$) and the lower switch ($S_L$). The magnitude of the right arm dc source voltage is $V_{dc}$ and the left arm dc source's magnitudes are $2V_{dc.}$ The switching sequence used to generate an 11-level voltage is given in Table I. For safe operation and to avoid short circuits, the switch pairs ($S_2$,$S_3$), ($S_4$,$S_5$) and ($S_U$, $S_L$) should not be turned on simultaneously.

Various modes of operation for the fundamental 11-level inverter are illustrated in Fig. 2. The switches $S_3$, $S_4$ and $S_L$ are turned ON to produce the first output voltage level $+V_{dc}$ across the load. For level 2, the voltages of the capacitors $C_1$ and $C_4$ are added together with a combination of the switches $S_2$, $S_5$, $D_1$ and $S_L$ to supply $+2V_{dc}$ across the load.

Level 3 ($+3V_{dc}$): Switches $S_2$, $S_4$, $V_{dc}$, $S_L$, $C_4$, $D_1$ and $C_1$.

Level 4 ($+4V_{dc}$): Switches $S_2$, $S_5$, $S_L$, $S_1$ and $C_1$- $C_4$

Level 5 ($+5V_{dc}$): Switches $S_1$, $S_2$, $S_4$, $S_L$, $V_{dc}$ and $C_1$- $C_4$.

In order to generate the negative cycle output levels of the switches $S_U$, $S_3$, $S_5$ and $S_4$ are turned on. Similarly, all of the levels are generated by proper switching of the corresponding switches as given in the Table I. In levels 2 and 3, a diode plays a major role in providing the current path. However, the diode is a unidirectional device which allows a current of either positive or negative polarity.

This leads to the origin of a spike on the output voltage which can be overcome by two different approaches: (i) connecting an LC filter across the load to minimize the voltage spike, and (ii) replacing the diode with a switch containing an anti-parallel diode.

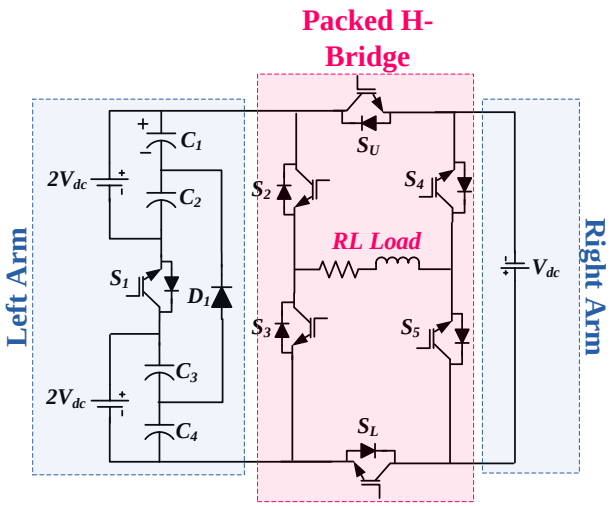



Fig. 1. Basic unit of the proposed multilevel inverter.

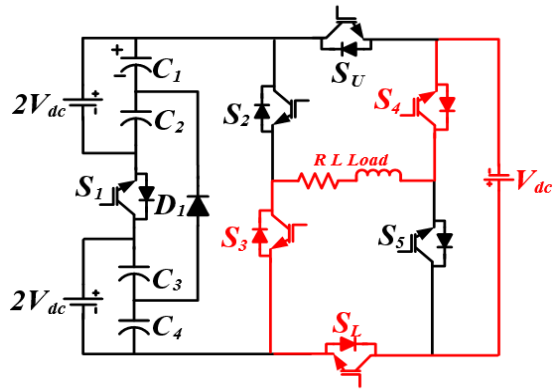
TABLE I
Switching Sequence for the Proposed 11-Level Inverter

| Output Voltage ($V_{Out}$) | | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $D_1$ | $S_U$ | $S_L$ |
|---|---|---|---|---|---|---|---|---|---|
| Positive Level | $1V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| | $2V_{dc}$ | 0 | 1 | 0 | 0 | 1 | $D_1$ | 0 | 1 |
| | $3V_{dc}$ | 0 | 1 | 0 | 1 | 0 | $D_1$ | 0 | 1 |
| | $4V_{dc}$ | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| | $5V_{dc}$ | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| Zero Level | 0 | 0<br>0 | 1<br>0 | 0<br>1 | 1<br>0 | 0<br>1 | 0<br>0 | 1<br>0 | 0<br>1 |
| Negative Level | $-1V_{dc}$ | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| | $-2V_{dc}$ | 0 | 0 | 1 | 1 | 0 | $D_1$ | 1 | 0 |
| | $-3V_{dc}$ | 0 | 0 | 1 | 0 | 1 | $D_1$ | 1 | 0 |
| | $-4V_{dc}$ | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| | $-5V_{dc}$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

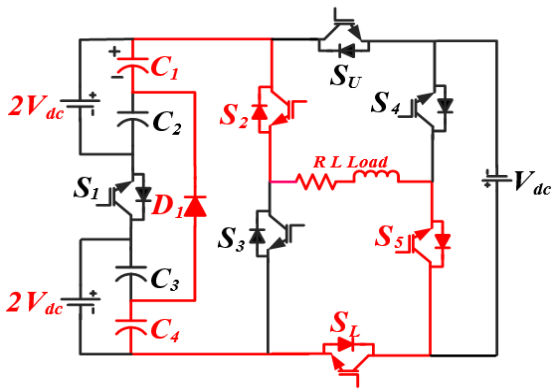
* Dead time considered is 4 µs

The use of an LC filter design in the first approach is more complicated and the power losses are higher in the passive components when compared to the active devices. Therefore, in this paper the second approach of replacing the diode with a switch is used. A circuit diagram of the proposed 11-level MLI without a switched diode is shown in Fig. 3. In this circuit, the diode ($D_1$) is replaced by the switch ($S_6$) to provide a bidirectional current path.

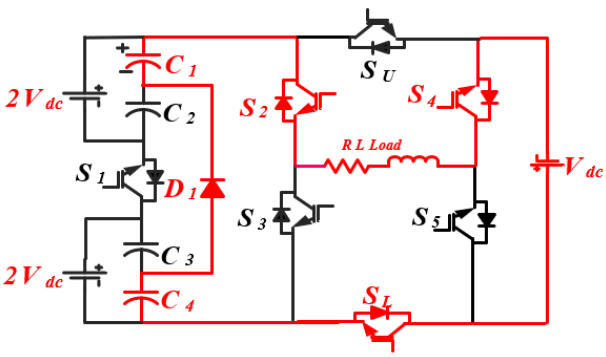
To increase the number of levels with a reduced number of switches, a cascaded structure of the basic module can be used as shown in Fig. 4. The required number of switches,


2Vdc
C1
C2
S1
D1
C3
2Vdc
C4
SU
S2
S4
R L Load
S3
S5
SL
Vdc

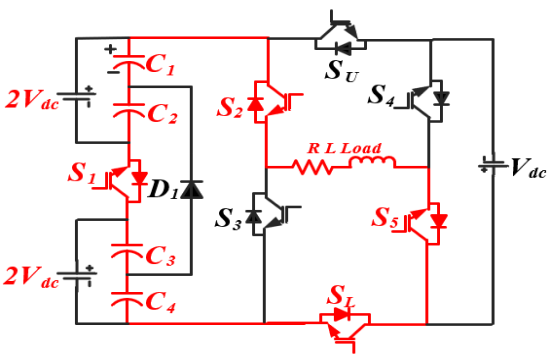
(a)


2Vdc
C1
C2
S1
D1
C3
2Vdc
C4
SU
S2
S4
R L Load
S3
S5
SL
Vdc

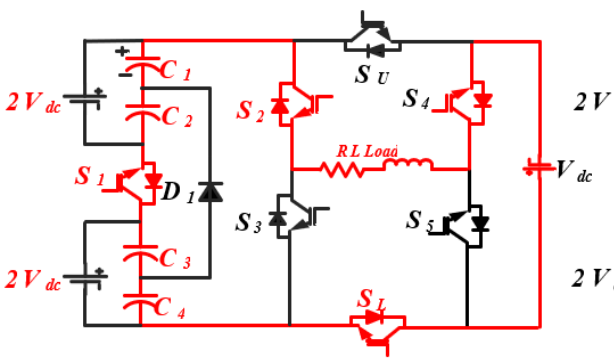
(b)


2Vdc
C1
C2
S1
D1
C3
2Vdc
C4
SU
S2
S4
R L Load
S3
S5
SL
Vdc

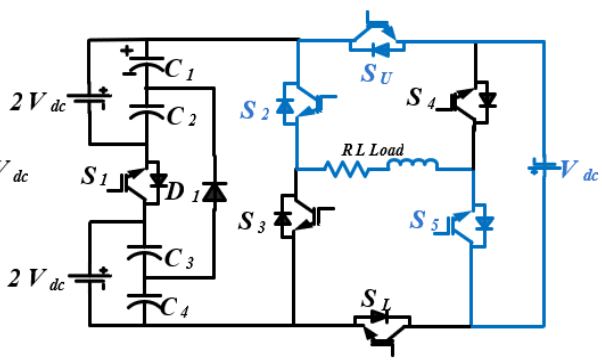
(c)


2Vdc
C1
C2
S1
D1
C3
2Vdc
C4
SU
S2
S4
R L Load
S3
S5
SL
Vdc

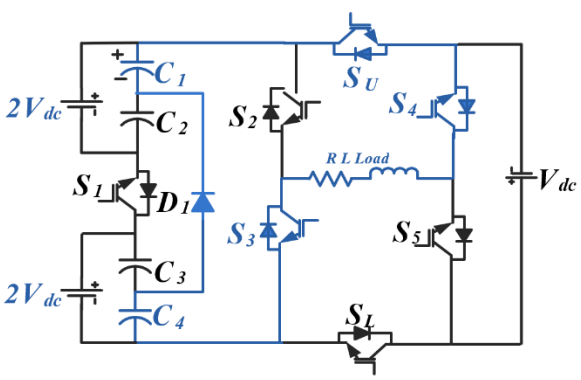
(d)


2Vdc
C1
C2
S1
D1
C3
2Vdc
C4
SU
S2
S4
R L Load
S3
S5
SL
Vdc

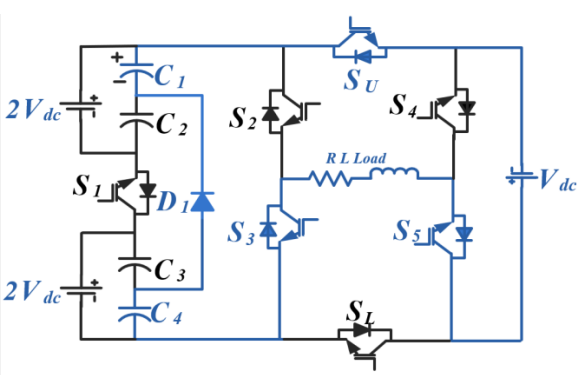
(e)


2Vdc
C1
C2
S1
D1
C3
2Vdc
C4
SU
S2
S4
RL Load
S3
S5
SL
Vdc

(f)


2Vdc
C1
C2
S1
D1
C3
2Vdc
C4
SU
S2
S4
R L Load
S3
S5
SL
Vdc

(g)


2Vdc
C1
C2
S1
D1
C3
2Vdc
C4
SU
S2
S4
R L Load
S3
S5
SL
Vdc

(h)

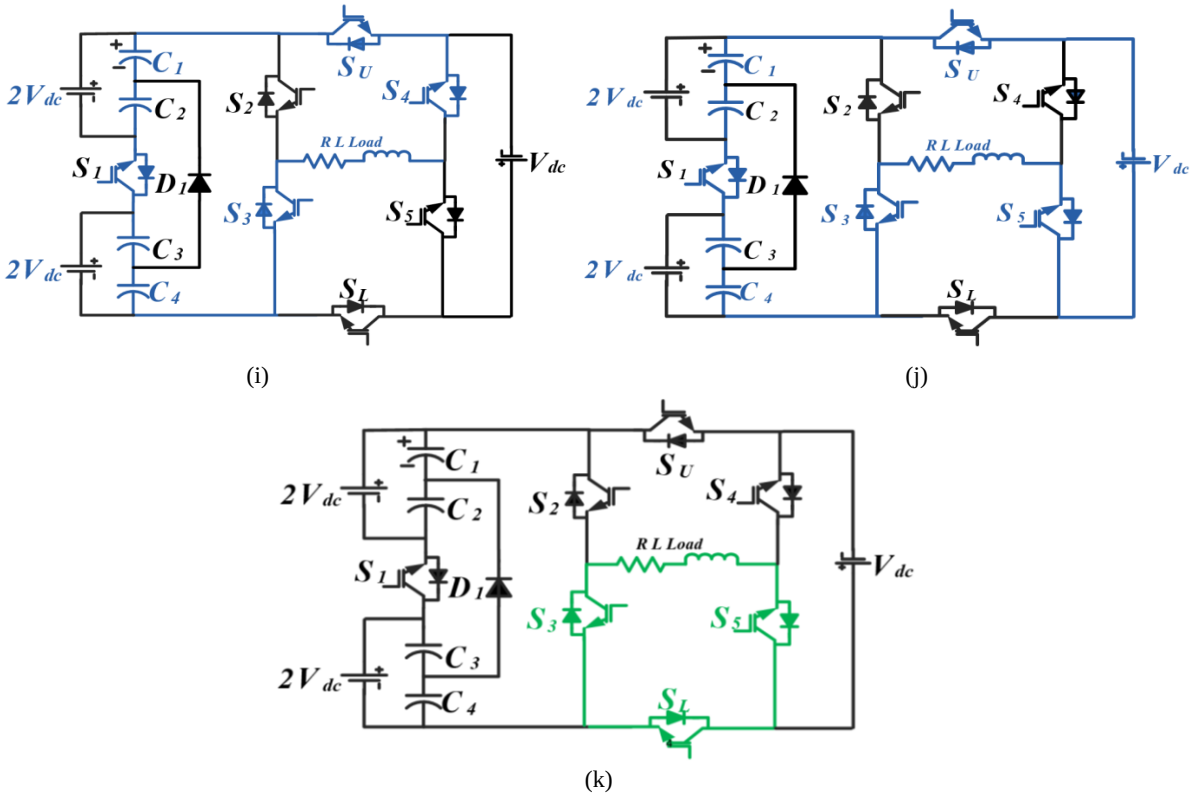



Fig. 2. Various modes of operation for the proposed 11-level inverter.

TABLE II
COMPARISON OF THE PROPOSED TOPOLOGY IN TERMS OF THE FUNDAMENTAL MODULE AND THE NUMBER OF LEVELS

| Description | Based on Cascaded Topology | Based on desired levels |
|---|---|---|
| Number of Level | 10n+1 | $N_{Level}$ |
| Number of Switches | 8n | $4*(N_{Level}+1)/6$ |
| Number of Diodes | 8n | $4*(N_{Level}+1)/6$ |
| Number of Gate Driver Circuits | 8n | $4*(N_{Level}+1)/6$ |
| Number of DC-Link Capacitor | 5n | $5*(N_{Level}+1)/2$ |
| Number of DC Sources | 3n | $N_{Level}+1$ |
| Total Standing Voltage(TSV) | 24n | $2*(N_{Level}+1)$ |

Where "n" denotes number of module and "$N_{Level}$ "denotes Number of level.

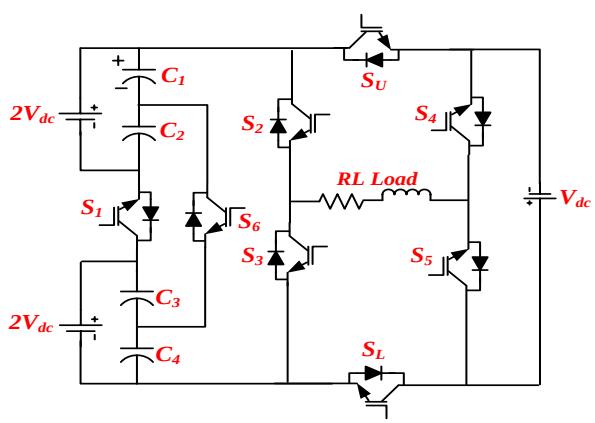



Fig. 3. Proposed multilevel inverter without a switched diode.

gate driver circuits, total standing voltage, number of DC-Link capacitors and number of dc sources are listed in Table II.

To avoid this condition, the voltage balancing circuit presented in [21] is recommended, and is shown in Fig. 5. The voltage balancing circuit is a combination of capacitors and diodes. In Fig. 5(a), the dc source voltage is boosted by a boost converter and this voltage is balanced across the dc-link capacitors. This type of converter is more suitable for photovoltaic applications. Fig. 5(b) shows the absence of boost converters. This is more suitable for regulated dc sources.

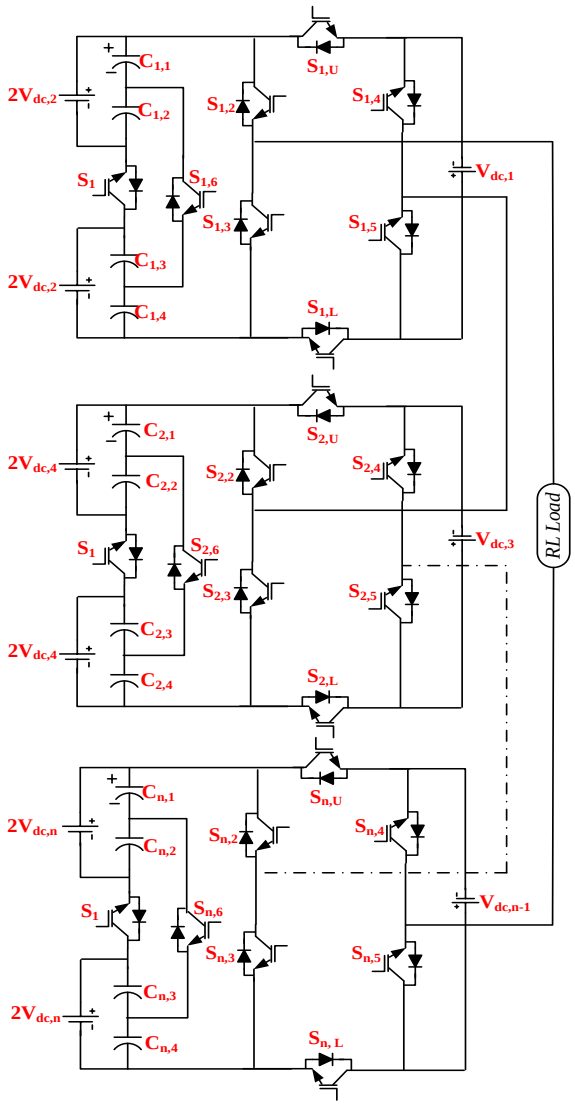



Fig. 4. Proposed cascaded multilevel inverter topology.

## III. DC- Link Capacitor Voltage Balancing and Ripple Voltage Calculation

Series connected dc-link capacitors do not provide balanced output voltages on the switches, which leads to the production of over voltages on the switches.

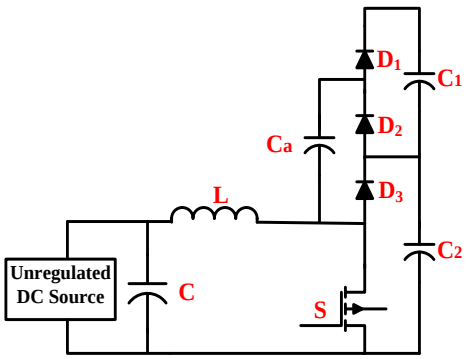
The voltage balancing of each capacitor is determined as follows:

The boost converter output voltage is determined by equation (1) with respect to the duty cycle (D) of the converter.

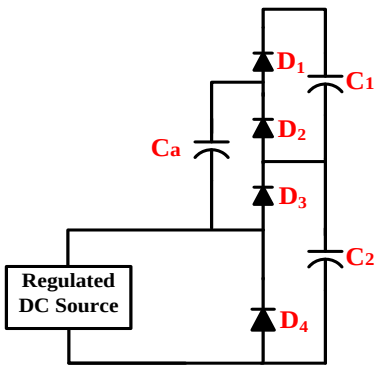
$$\frac{V_C}{V_{in}} = \frac{1}{1-D} \tag{1}$$

The current across the load with respect to the duty cycle is expressed in equation (2):

$$I_L = \frac{1}{(1-D)R_L} \tag{2}$$




(a)




(b)

Fig. 5. Voltage balancing circuits: (a) for an unregulated dc source (b) for a regulated dc source.

Finally, the "N" number of capacitors is connected in series and the voltage across each of the capacitors is expressed in terms of the duty cycle and the number of capacitor in (3):

$$\frac{V_C}{V_{in}} = \frac{1}{((1-D)/N) + (N R_{esrL}/(1-D)/R_L)} \tag{3}$$

$$\frac{V_C}{V_{in}} = \frac{1}{(1/N) + (N R_{esrL}/R_L)} \tag{4}$$

The general expression for the "N" number of dc-link capacitor is expressed in equation (5):

$$V_{Out} = NV_C - (N-1)4V_d \tag{5}$$

Where $V_C$ is the lower voltage of the capacitor, $V_d$ is the assumption of a voltage drop across the switch and diode, *N*- is the number of dc/dc levels and $R_{esL}$ is the inductor ESR value.

The expression for the dc-link capacitor voltage for the proposed inverter is presented in equation (6):

$$V_{Out} = 4(V_C - 3V_d) \tag{6}$$

The capacitance values are designed with reduced voltage ripples and improved efficiency of the inverter [22].

The following factors are considered to measure the power calculation of the proposed multilevel inverter: (i) switching losses (ii) conduction losses and (iii) capacitor losses.

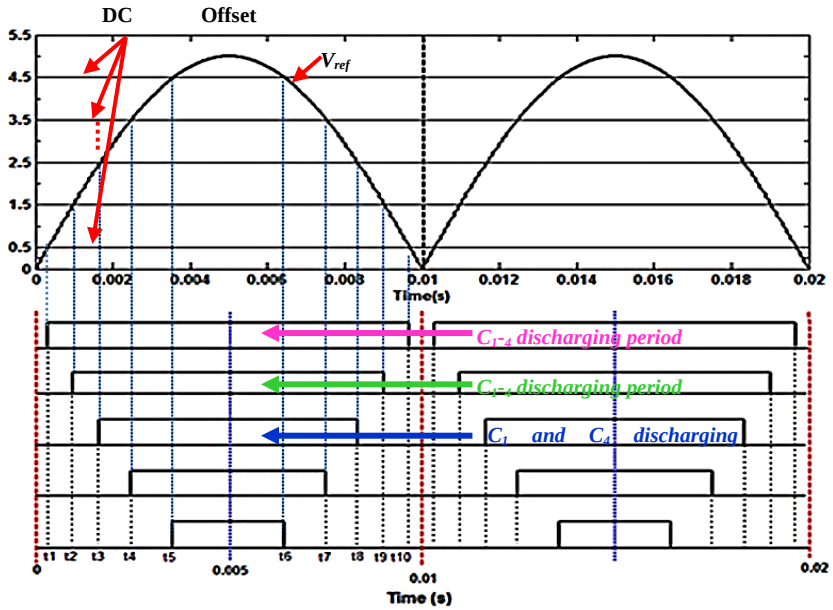



Fig. 6. Pulse generation waveform for an 11-level inverter with a DC-link capacitor discharging period.

The switching losses mainly depend on the switching frequency and blocking voltage of the switches, and the conduction losses depend on the voltage drop across the switches and the rms current flowing through that particular switch. The capacitor losses depend on the voltage ripples and the ESR (Equivalent Series Resistance) values of the capacitors. The proposed inverter supplies the load power from both the dc source and the dc-link capacitors. The inverter output voltages are kept constant by balancing the voltage magnitude of the dc-link capacitors. However, the load draws a continuous current $i_0$ and this influences the voltage ripples across the capacitors. The capacitor discharging period $C_{1,4}$ starts when the switch $S_6$ is turned ON and ends when $S_6$ is turned OFF.

$$\Delta V_i = \frac{1}{C_{1,4}} \int_{t_2}^{0.01-t_2} i_0 dt + \frac{1}{C_{2,3}} \int_{t_4}^{0.01-t_4} i_0 dt \qquad (7)$$

Where $t_2$ is the capacitor $C_{1\text{-}4}$ start and end time, and 0.01-$t_2$, ($t_9$) is the capacitor $C_{2\text{-}3}$ start and end time of the discharging duration for a half period of the fundamental frequency as shown in Fig. 6. For the fundamental switching method, the time interval is represented as the angle of conduction of the switch $S_1$, $S_6$ or $S_1$ diode pair. In the first configuration (with a switched diode) diode is always in conduction and the second part of equation (7) does not exist, since the proposed modulation technique is a half period method and "t", the simplified equation for the voltage ripple ($\Delta V_i$) is expressed in (8).

$$\Delta V_i = \frac{1}{2\pi fs}\left( \frac{1}{C_{1,4}} \int_{\theta_2}^{\pi-\theta_2} i_0 dt + \frac{1}{C_{2,3}} \int_{\theta_4}^{\pi-\theta_4} i_0 dt \right) \qquad (8)$$

where $\theta_1$- $\theta_4$ are the switching angles. The amount of charge $\Delta Q_i$ is calculated by the approximate discharge period and is given in equation (9):

$$\Delta Q_i \cong \frac{V_{in}}{2\pi R\ fs} \sum_{a=1}^{4} (\pi - 2\theta_a)(a) \qquad (9)$$

where "R" is the load resistance (unity power factor) and "a" is the number of capacitors in a basic unit. Finally, the voltage ripple is derived as:

$$\Delta V_i = \frac{V_{in}}{2\pi R\ C_{1\text{-}4}\ fs} \sum_{a=1}^{4} (\pi - 2\theta_a)(a) \qquad (10)$$

The capacitance is inversely proportional to the voltage ripples and directly proportional to the load current. In practical implementation, the capacitor should be able to supply the maximum current with the minimum voltage ripples.

## IV. Comparison with Other Recent Topologies

Recently proposed topologies are designed to minimize the number of switches, the number of dc sources and the voltage stress across the switches. A few of these topologies are considered for comparison with the proposed topology. In Fig. 7(a) multiple dc sources are used and all of the dc sources are connected with a series/parallel combination of switches to produce multiple dc voltages with equal magnitudes. The full bridge inverter is used in the output side to change the polarity of the output voltage.

The maximum blocking voltage for each of the switches connected in cascaded is $V_{dc}$. However, the full bridge inverter switches should withstand for the sum of the voltages connected in series ($nV_{dc}$) as discussed in [11]. In [12], a new

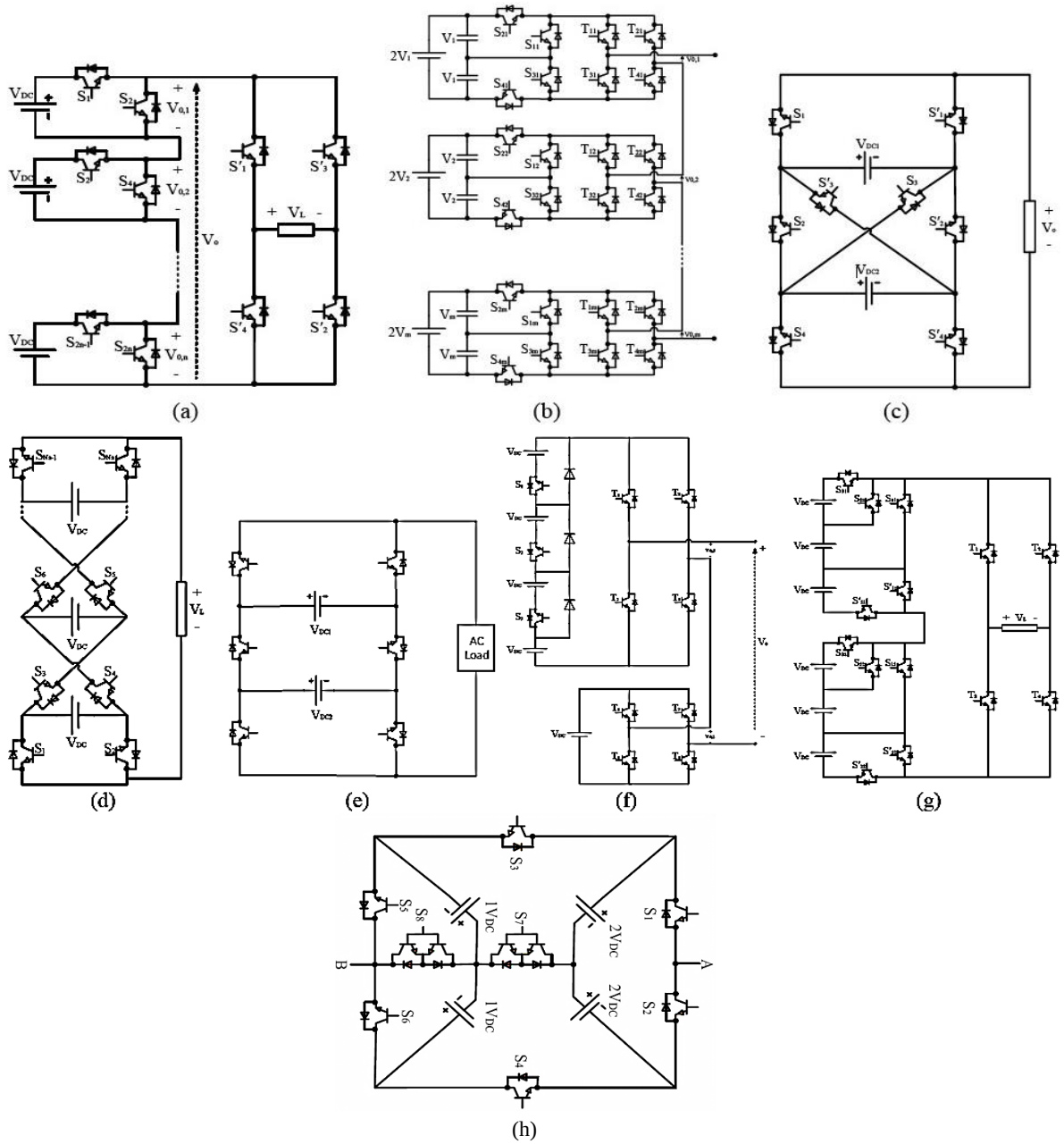



Fig. 7. Different multilevel inverter topologies with a reduced switch count.

cascaded design for a multilevel inverter is presented as shown in Fig. 7(b), where the basic unit is constructed with six switches and two dc link capacitors with a single dc source. The basic unit is connected in cascaded to produce the maximum output voltage level with a reduced blocking voltage. However, the switches count is still high. Cross connected switches in a packed h-bridge is presented in Fig. 7(c). In this topology, the maximum output voltage level is generated with reduced dc sources, even though the number of switches and blocking voltages are high as detailed in [13].

In Fig. 7(d) and Fig. 7(e) both of the topologies are different in structure. However, in terms of their output voltage level, the number of switches is equal with same blocking voltage [14], [15]. In addition, various multilevel inverter topologies and control techniques are discussed in [16], [17]. A hybrid topology is presented in [18] and its circuit diagram is shown in Fig. 7(f). The hybrid connection of a full bridge inverter with a basic unit is proposed for switch reduction and blocking voltage minimization. However, this topology uses a unidirectional switch which affects the output voltage waveform when the load is highly inductive.

The topology shown in Fig. 7(g) is proposed for a reduced number of dc sources. Each basic unit is connected in series to generate the maximum number of voltage levels for the minimum number of dc sources as presented in [19].

In [20], an E-type topology for the asymmetric configuration

TABLE III
COMPARISONS OF DIFFERENT MULTILEVEL INVERTER TOPOLOGIES FOR VARIOUS PARAMETERS

| | NPC | FC | CHB | [11] | [12] | [14] | [15] | [19] | [20] | Proposed |
|---|---|---|---|---|---|---|---|---|---|---|
| No. of Switches | $2(N_L-1)$ | $2(N_L-1)$ | $2(N_L-1)$ | $N_L+3$ | $N_L+1$ | $N_L+1$ | $N_L+1$ | $N_L-1$ | $5(N_L-1)/6$ | $4(N_L+1)/6$ |
| No. of DC Link Capacitors | $(N_L-1)/2$ | $(N_L-1)/2$ | $(N_L-1)/2$ | $(N_L-1)/2$ | $(N_L-1)/2$ | $(N_L-1)/2$ | $(N_L-1)/2$ | $(N_L-1)/2$ | $(N_L-1)/3$ | $(N_L-1)/2$ |
| No. of Switches in terms of DC links | 4 | $2+2/(N_L-2)$ | 4 | $1/3+4/3(N_L-1)$ | $2+4/(N_L-1)$ | $2+4/(N_L-1)$ | $2+4/(N_L-1)$ | 3 | 5/2 | 8/5 |
| TSV($V_{dc}$) | $2(N_L-1)$ | $2(N_L-1)$ | $2(N_L-1)$ | $3(N_L-1)$ | $2(N_L-1)$ | $2(N_L-1)$ | $2(N_L-1)$ | $3(N_L-1)$ | $10(N_L-1)/6$ | $2(N_L+1)$ |
| Number of Source | 1 | 1 | $(N_L-1)/2$ | $(N_L-1)/2$ | $(N_L-1)/2$ | $(N_L-1)/2$ | $(N_L-1)/2$ | $(N_L-1)/2$ | $(N_L-1)/3$ | $(N_L+1)/4$ |

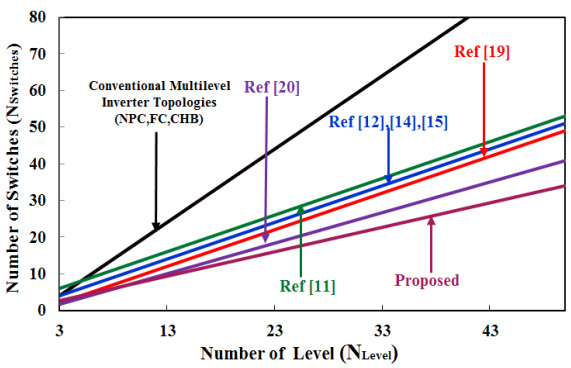
is proposed with a reduced switch count. In this topology, both unidirectional and bidirectional switches are used as shown in Fig. 7(h). Many topologies require a larger number of switches with reduced blocking voltages. However, the number of dc sources used is high. Conventional and recent topologies are compared with the proposed topology in table III for various parameters such as the number of switches, number of DC link capacitors, Total Standing Voltage (TSV) and number of dc sources. The proposed topology requires a lower number of switches in terms of the DC link capacitors and a reduced number of DC sources.

### *A. Number of Level Vs Number of Switches:*

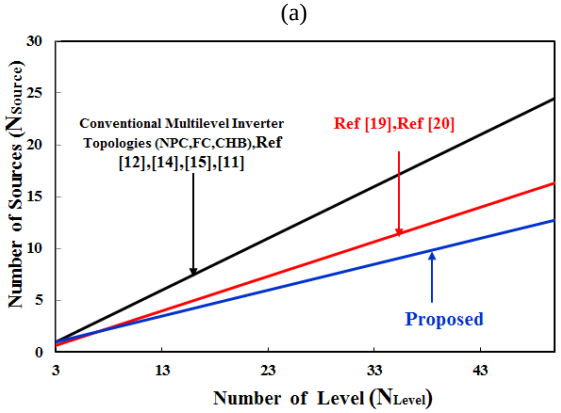
One of the objectives of the proposed inverter is to reduce the number of power switches, which is plotted in Fig. 8(a). Various metrics are involved to evaluate the reliability of the multilevel inverter. In this, the switch count is one of the major parameters. Existing multilevel inverters CHB, NPC, FC, [11], [12], [14], [15] and [19], [20] use a larger number of switches whereas the proposed topology requires a smaller number of switches. If the number of switches is high, the number of gate driver circuits also increases, which in turn reduces the reliability of the inverter.

### *B. Number of Level Vs Number of Sources:*

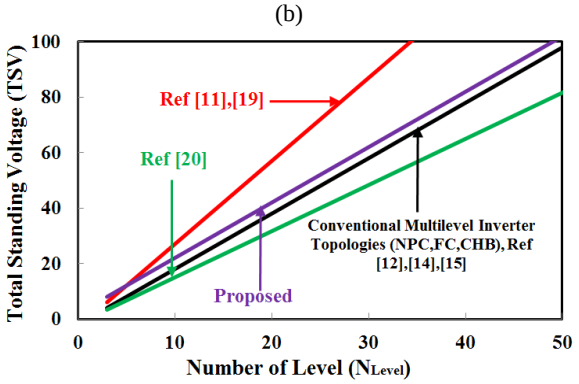
The required number of dc sources is another important factor in multilevel inverter. This is due to the fact that the multilevel inverter requires an increased number of dc sources with respect to the number of levels. However, the availability and provision of dc sources are more complicated in some applications such as electric vehicles. The proposed topology uses a reduced number of DC sources to produce the maximum number of levels as shown in Fig. 8(b). In Fig. 7(h), the basic cell requires a maximum of four dc sources to generate a 13-level output with ten switches, whereas proposed topology uses three dc sources to produce the maximum of 11-level outputs with eight switches.




(a)




(b)




(c)

Fig. 8. Various comparison results: (a) $N_{Level}$ Vs $N_{Swicthes}$; (b) $N_{Level}$ Vs $N_{Sources}$; and (c) $N_{Level}$ Vs TSV.

### *C. Number of Level Vs Total Standing Voltage:*

One of the advantages of multilevel inverters is the minimum voltage stress across the switches. Except for the conventional topologies all of the other recent multilevel inverter topologies have a high standing voltage since the number of switches is inversely proportional to the standing voltage on the switches.

The total standing voltage on the switches is calculated as the sum of the individual blocking voltages on the switches. In Fig. 8(c), the total standing voltage of the proposed topology is higher than that of the conventional topology and [20]. However, it is less than that in [11] and [19]. Here, it is worth mentioning that the proposed topology uses minimum number of switches when compared to the conventional topologies.

## V. Simulation and Experimental Results

The proposed structure is simulated using Matlab/Simulink software. The Nearest Level Modulation (NLM) method is used to generate the switching pulses, which operate with the fundamental switching frequency (50Hz). The NLM method produces low switching losses and is easy for hardware implementation. The NLM method generates more harmonics in output voltage for lower levels and this is suitable for a higher number of levels [23] due to the low harmonics in higher levels.

The harmonic voltage is expressed in terms of a Fourier series equation as follows:

$$V_o(t) = \sum_{n=1,3,5.....}^{\infty} \frac{4V_{dc}}{n\pi}\cos(n\theta_j)\sin(n\omega t) \tag{11}$$

$$THD = \sqrt{\frac{\sum_{h=3,5,7....}^{\infty} V_{oh}}{V_{o1}}} = \sqrt{\left(\frac{V_{orms}}{V_{o1}}\right)^2 - 1} \tag{12}$$

where h (the odd order of the harmonic) = 3, 5, 7…. and $V_{o1}$ is the fundamental voltage. $V_{oh}$ is the order of the harmonics. $V_{o,rms}$- is the rms value of the output voltage. The magnitude of $V_{o1}$ and $V_{o,\ rms}$ can be calculated using the following relations:

$$V_{o,rms} = \frac{2\sqrt{2}V}{\pi} \times \sqrt{\sum_{h=odd}^{\infty}\left(\sum_{j=1}^{N_{Level}} \frac{\cos(h\theta_j)}{h}\right)^2} \tag{13}$$

$$V_{o1} = \frac{2\sqrt{2}V}{\pi} \times \left(\sum_{j=1}^{N_{Level}} \frac{\cos(h\theta_j)}{h}\right) \tag{14}$$

where $\theta_1$, $\theta_2$… $\theta_{NLevel}$ are switching angles, which are calculated using equation (15):

$$\theta_j = \sin^{-1}\left(\frac{j-0.5}{N_{Level}}\right) \quad j=1,2,3....N_{Level} \tag{15}$$

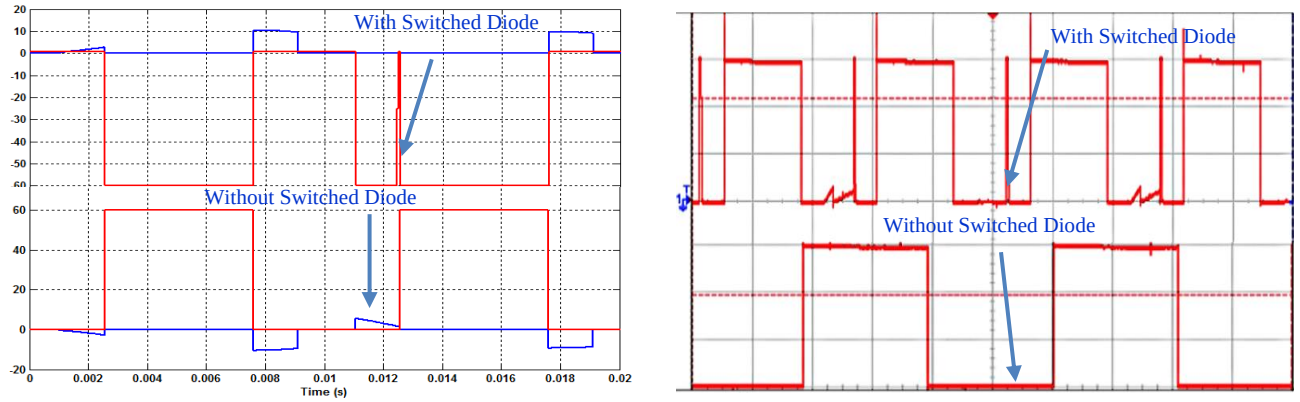
The voltage waveforms across the diode and switch for both of the topologies, for the simulation and the hardware setup are shown in Fig. 9. The first configuration (switched diode based) topology produces voltage spikes due to the non-conduction of the opposite current, whereas in the second configuration (without a switched diode) the voltage spikes are eliminated. Fig. 9(a) shows the conduction current in the forward and reverse directions during the simulations without the use of a switched diode as illustrated in blue. A similar waveform for the experimental results of the voltage is shown in Fig. 9(b). In conclusion, the diode based topology is not suitable for all applications except where a unidirectional current is required.

The proposed 11-level inverter output voltage by simulations for both of the configurations are presented in Fig. 10. For the first configuration (switched diode), due to the diode, voltage spikes are present in every half cycle of the output voltage waveform, as shown in Fig. 10(a), with an increased voltage THD of 9.87 % and current THD of 1.33%. For the second configuration (without switched diode), the simulation results are presented in Fig. 10(b) with voltage and current THDs of 7.61% and 1.11%, respectively.

In the experimental test, the value of the right arm dc source is 30V and the left arm dc sources are each 60V. The R-L load with R=80 Ω and L=100 mH is used for this topology and the values of the dc-link capacitors $C_1$-$C_4$ are 100μF. The second method (without a switched diode) circuit diagram is used to balance the dc-link capacitor voltages, and the balanced voltages are illustrated in Fig. 11(a). According to the proposed circuit diagram, the levels are: 0, ±30V, ±60V… ±120V, ±150V. In the experimental test, eight IGBTs (BUP400D) with $V_{CE}$ = 600V and $I_C$ = 22A and eight gate driver circuits (HCPL316j) are used. The blocking voltages of the switches $S_L$=$S_U$=150V, $S_6$=$S_1$=60V, $S_3$=$S_2$= 120V and $S_5$=$S_4$=30V as shown in Fig. 11(b). For both of the configurations the voltage and current waveforms obtained from the experimental setup are given in Fig. 12 and Fig. 14. The FFT spectrum, obtained from the power quality analyzer, for both of the configurations are given in Fig. 13 and Fig. 15, respectively.

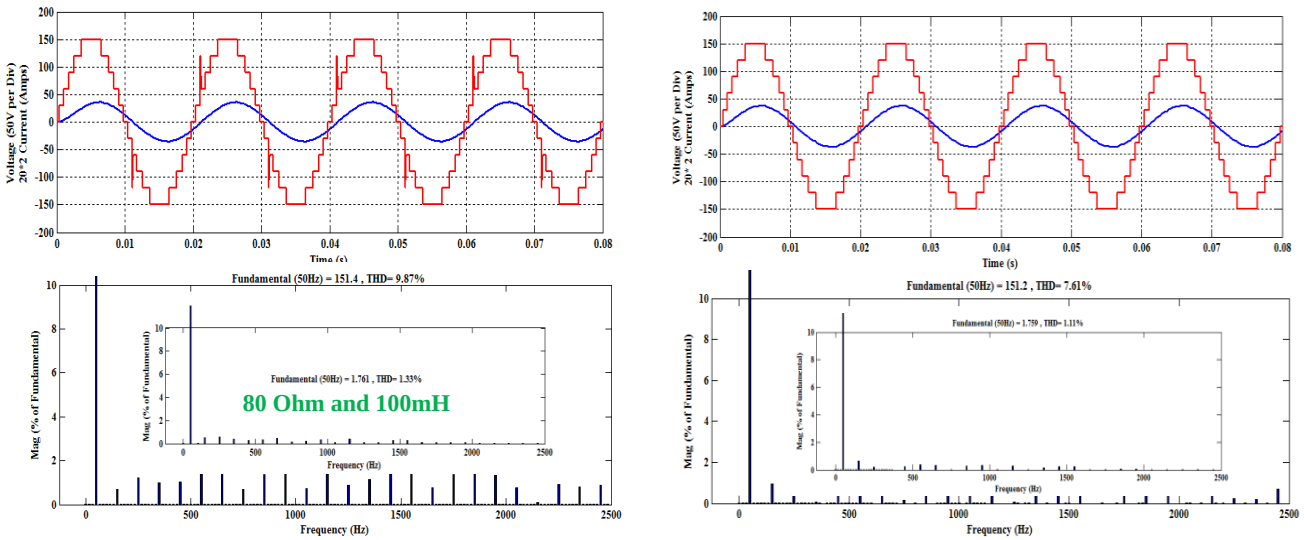
For the first configuration the RMS value of the output voltage is 114.04V and the output power is 118.37W, whereas for the second configuration (without a switched diode), the RMS value of output voltage is 102.89V and the output power is 113.84 W. Similarly the voltage and current THDs for the first configuration are 10.54% and 6.53 %, whereas for the second configuration they are 7.712% and 2.876%, respectively. From these results it is evident that replacing a diode by a switch eliminates the spikes in the voltage waveforms [refer to Fig. 12 and Fig. 14]. Hence, the second configuration (without a switched diode) produces a better quality output when compared to the first configuration (with a switched diode).

A summary of the results obtained for the proposed configurations for the simulation and hardware setup are



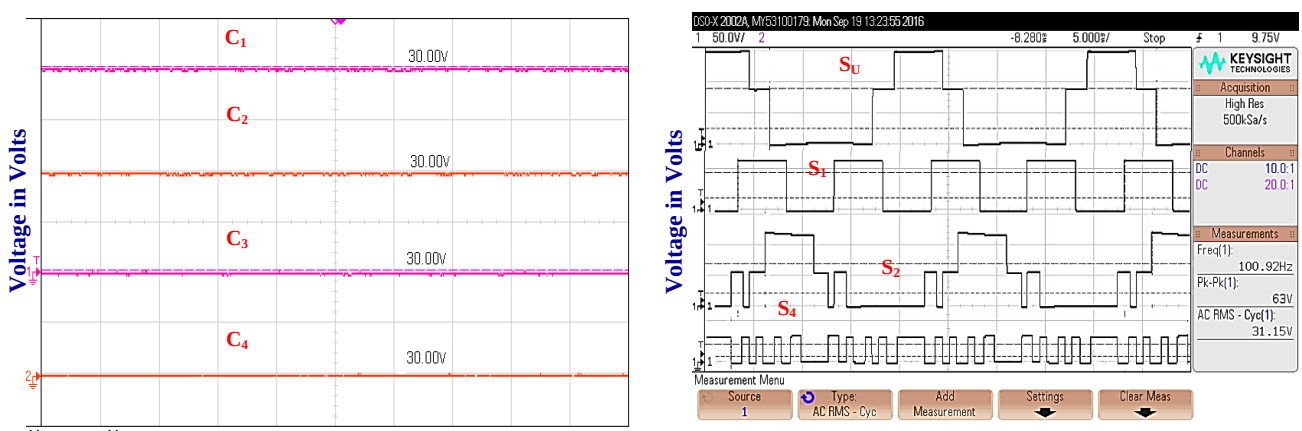

(a) (b)

Fig. 9. Voltage waveform across the diode and switch: (a) simulation results; (b) experimental results.




(a) (b)

Fig. 10. Simulation results of: (a) the first configuration output voltage and current waveform with a FFT spectrum; (b) the second configuration output voltage and current waveform with a FFT Spectrum.




(a) (b)

Fig. 11. (a) Balanced input voltage by balancing the circuits; and (b) blocking voltage across various switches in an 11-level inverter.

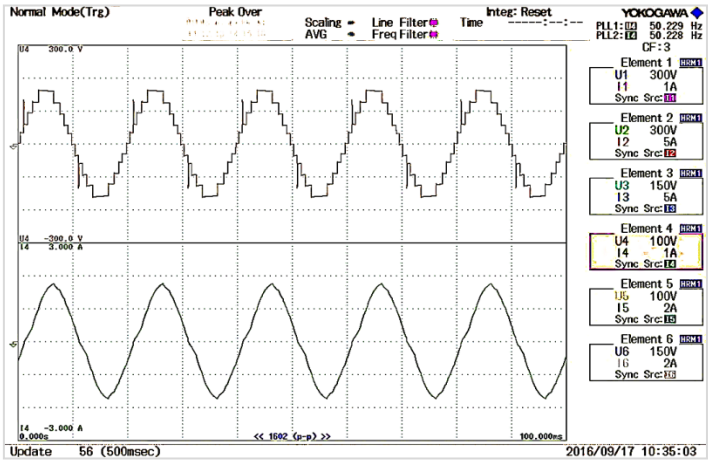



Fig. 12. Output voltage and current waveforms of switched-diode configuration.

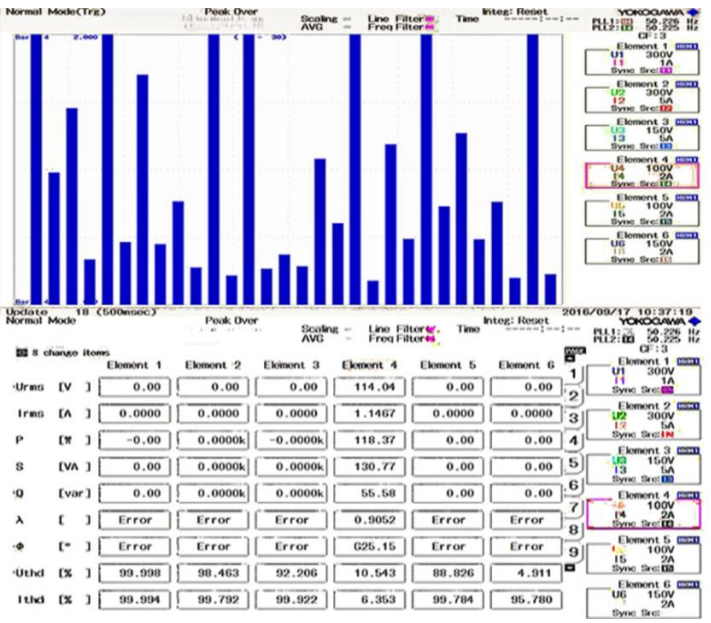



Fig. 13. Experimental results of a switched-diode with a voltage FFT spectrum and power quality analyzer output.

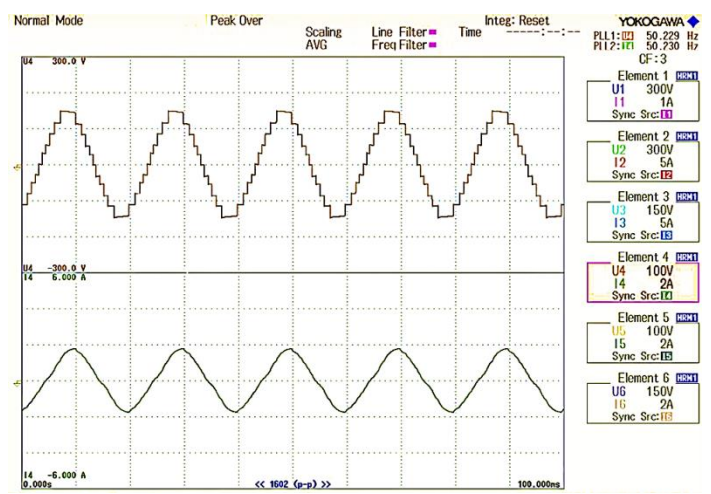



Fig. 14. Output voltage and current waveforms of the second configuration.

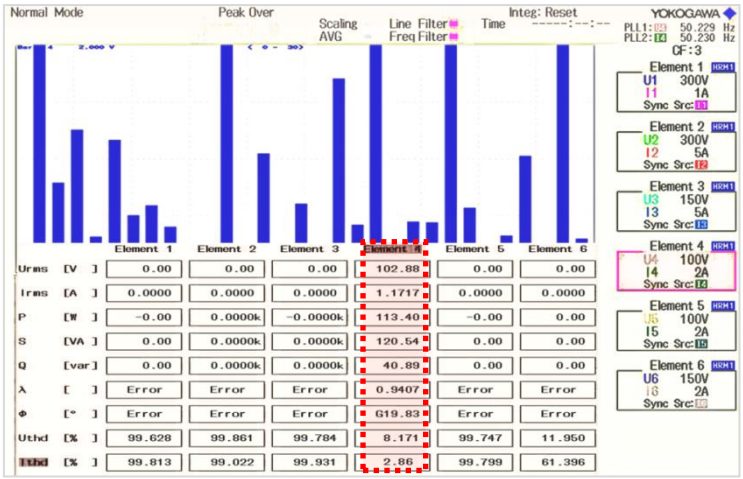



Fig. 15. Experimental results of the second configuration with a voltage FFT spectrum and power quality analyzer output.

TABLE IV
SUMMARY OF BOTH CONFIGURATIONS OF THE PROPOSED TOPOLOGY

| Configuration | Results | $V_{in}$ | R (Ω) | L (mH) | $V_{rms}$ (V) | $I_{rms}$ (A) | V THD (%) | I THD (%) | $P_{in}$ (W) | $P_{out}$ (W) | Efficiency η (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| First Configuration (With a Switched Diode) | Simulation | 150V | 80 | 100 | 107.56 | 1.25 | 9.87 | 1.33 | 134.45 | 124.1 | 92.30 |
| | Experimental | 150V | 80 | 100 | 114.8 | 1.14 | 10.54 | 6.35 | 130.87 | 118.37 | 90.45 |
| Second Configuration (Without a Switched Diode) | Simulation | 150V | 80 | 100 | 107.22 | 1.24 | 7.61 | 1.11 | 132.95 | 125.8 | 94.65 |
| | Experimental | 150V | 80 | 100 | 102.89 | 1.17 | 7.71 | 2.87 | 120.38 | 113.40 | 94.20 |

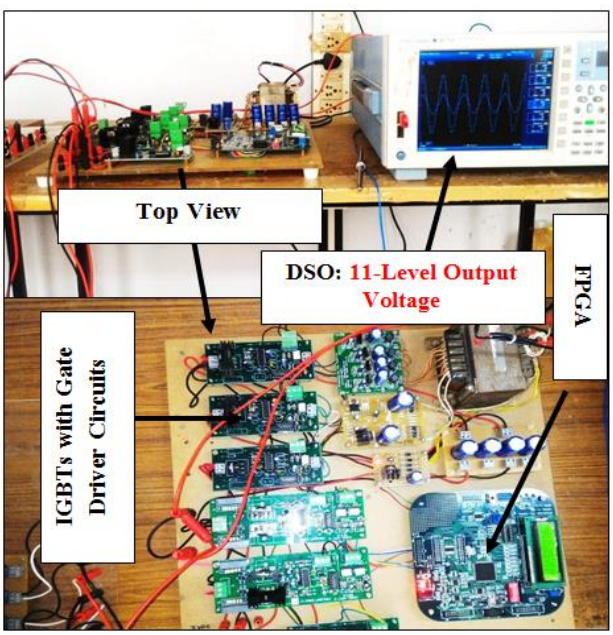



Fig. 16. Photograph of the experimental model.

shown in Table IV. The RMS voltage and output power of the first configuration is higher than that of the second configuration. However, its overall efficiency is low. A photograph of the experimental setup is shown in Fig. 16.

## VI. CONCLUSION

A new multilevel inverter structure with two different configurations is described in this paper. The proposed configurations generates an 11-level output voltage with a reduced number of power electronic components. The proposed topology can be cascaded for high voltage applications with a low voltage stress and low power electronic devices. It is confirmed that the proposed configuration generate a higher number of output voltage levels when compared to some of the other multilevel inverters presented in this paper. The first configuration (with a switched diode) has a spike in the output voltage and has a higher voltage and current THD, whereas the second configuration (without a switched diode) has a better output voltage without a spike and the voltage and current THD is low. Therefore, the second configuration with a cascaded structure is recommended for high voltage applications.

## REFERENCES

[1] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura. "State-of-charge (SOC)-balancing control of a battery energy storage system based on a cascade PWM converter," *IEEE Trans. Power Electron*, Vol. 24, No. 6, pp. 1628-1636, Jun. 2009.

[2] K. Himour, K. Ghedamsi, and E. M. Berkouk, "Supervision

and control of grid connected PV-Storage systems with the five level diode clamped inverter," *Energy Conversion and Management*, Vol. 77, pp. 98-107, Oct. 2013.
[3] M. F. Escalante, J.-.C. Vannier, and A. Arzandé, "Flying capacitor multilevel inverters and DTC motor drive applications," *IEEE Trans. Ind. Electron*, Vol. 49, No. 4, pp. 809-815, Aug. 2002.
[4] K. Ramani, M. A. J. Sathik, and S. Sivakumar, "A new symmetric multilevel inverter topology using single and double source sub-multilevel inverters," *J. Power Electron.*, Vol. 15, No. 1, pp. 96-105, Jan. 2015.
[5] A. Mokhberdoran and A. Ajami. "Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology," *IEEE Trans. Power Electron.*, Vol. 29, No. 2, pp. 6712-6724, Dec. 2014.
[6] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "Optimal design of new cascaded switch-ladder multilevel inverter structure," *IEEE Trans. Ind. Electron.*, Vol. 29, No. 12, pp. 6712-6724, Dec. 2014.
[7] R. Samanbakhsh and A. Taheri, "Reduction of power electronic components in multilevel converters using new switched capacitor-diode structure," *IEEE Trans. Ind. Electron.*, Vol. 63, No. 11, pp. 7204-7214, Nov. 2016.
[8] E. Babaei and S. S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 9, pp. 4614-4621, Sep. 2014.
[9] A. Farakhor, R. Reza Ahrabi, H. Ardi, and S. N. Ravadanegh, "Symmetric and asymmetric transformer based cascaded multilevel inverter with minimum number of components," *IET Power Electron.*, Vol. 8, No. 6, pp. 1052-1060, Jun. 2015.
[10] J. S. Choi and F. S. Kang, "Seven-level PWM inverter employing series-connected capacitors paralleled to a single DC voltage source," *IEEE Trans. Ind. Electron.*, Vol. 62, No. 6, pp. 3448-3459, Jun. 2015.
[11] E. Babaei and S. H. Hosseini., "New cascaded multilevel inverter topology with minimum number of switches," *Energy Conversion and Management*, Vol. 50, No. 11, pp. 2761-2767, Jul. 2009.
[12] E. Babaei, M. F. Kangarlu, and M. Sabahi, "Extended multilevel converters: An attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters," *IET Power Electron.*, Vol. 7, No. 1, pp. 157-166, Jan. 2014.
[13] K. K. Gupta and S. Jain. "Topology for multilevel inverters to attain maximum number of levels from given DC sources," *IET Power Electron.*, Vol. 5, No. 4, pp. 435-446, Apr. 2012.
[14] M. F. Kangarlu and E. Babaei, "Cross-switched multilevel inverter: an innovative topology," *IET Power Electron.*, Vol. 6, No. 4, pp. 642-651, Apr. 2013.
[15] Y. Ounejjar, K. Al-Haddad, and L. A. Dessaint, "A novel six-band hysteresis control for the packed U cells seven-level converter: Experimental validation," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 10, pp. 3808-3816, Oct. 2012.
[16] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.*, Vol. 31, No. 1, pp. 135-151, Jan. 2016.
[17] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Perez, and J. Leon., "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2553-2580, Aug. 2010.
[18] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels," *IET Power Electron.*, Vol. 7, No. 1, pp. 96-104, Jan. 2014.
[19] M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Trans. Power Electron.*, Vol. 28, No. 2, pp. 625-636, Feb. 2013.
[20] E. Samadaei, S. A. Gholamian, A. Sheikholeslami, and J. Adabi, "An envelope type (E-type) module: Asymmetric multilevel inverters with reduced components," *IEEE Trans. Ind. Electron.*, Vol. 63, No. 11, pp. 7148-7156, Nov. 2016.
[21] M. A. J. Sathik, S. H. E. A. Aleem, R. Kannan, and A. F. Zobaa, "A new switched DC-link capacitor-based multi-level converter ($SDC^2MLC$)," *Electric Power Components and Systems*, Vol. 45, No. 9, pp. 1001-1015, Jun. 2017.
[22] Y. Ye, K. W. E. Cheng, J. Liu, and K. Ding, "A step-up switched-capacitor multilevel inverter with self-voltage balancing," *IEEE Trans. Ind. Electron*, Vol. 61, No. 12, pp. 6672-6680, Dec. 2014.
[23] M. Perez, J. Rodriguez, J. Pontt, and S. Kouro, "Power distribution in hybrid multi-cell converter with nearest level modulation," *IEEE International Symposium on Ind. Electron*, pp. 736-741, 2007.

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