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Isolated PFC Converter Based on an ADAB Structure with Harmonic Modulation for EV Chargers

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Abstract

This paper presents an isolated power factor correction converter for general-purpose electric vehicle chargers with a wide output voltage range. The converter is based on an asymmetrical dual active bridge structure so that the voltage stress of switching devices can be eliminated by transferring the transformer leakage inductance to the circuit parameters. Harmonic and output controls are performed by secondary switches, and primary switches are only operated at a fixed frequency with a 50% duty ratio. A harmonic modulation technique is also adopted to obtain a near-unity power factor without input current monitoring. The feasibility of the proposed charger is verified with a 3.3 kW prototype.

Key words: Battery charger, Electric vehicles, PFC converter

I. INTRODUCTION

New transportation methods are required to solve air pollution and reduce greenhouse gas emission, and vehicle electrification has been proposed as a solution. Various types of plug-in vehicles (xEVs) are available, and examples include battery electric vehicles (BEVs), hybrid EVs, plug-in hybrid EVs, and fuel-cell EVs (FCEV). These vehicles can also be classified as long-range and neighborhood EVs. Except for FCEV, most xEVs use battery packs as power sources, and they are designed with various battery voltages depending on battery usage [1]-[3]. A dedicated design is possible because on-board chargers mounted on vehicles deal with a specified battery only. However, off-board chargers utilized for electric bicycles and various vehicles should possess a wide output voltage range [4], [5]. In the near future, general-purpose on-board chargers will be required due to the increase in the production of xEVs. In single-phase applications, on-board and off-board chargers have a common conventional two-stage structure composed of a non-isolated boost converter as a harmonic pre-regulator, and various isolated DC/DC converters are used for electrical isolation and charging control [6], [7]. The most popular topology for isolated DC/DC converters is the phase-shift full-bridge (PSFB) converter that involves the "buck-type" operation; hence, it is applicable for general-purpose chargers due to its wide output voltage range. However, the PSFB converter cannot achieve high efficiency due to disadvantages, such as voltage stress of secondary circuits, large circulating current, narrow zero-voltage-switching (ZVS) range, and loss of snubber circuits [8]-[11]. Many resonant topologies have been introduced, and high efficiencies have also been reported due to the good characteristics, such as soft switching, low electrical stress in the rectifier, and absence of additional snubber circuits, of these topologies. However, they do not have wide output voltage ranges, and they are adequate for a charger design dedicated to a specified battery only [12]-[17]. Moreover, pulse-width modulation (PWM) resonant converters, which possess the same structure as series resonant converters (SRC) but adopt the PWM operation, can produce output voltages larger than those of resonant converters given an appropriate design. However, widening the output voltage

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range to be used for general-purpose chargers is difficult [18]. To obtain a wide output voltage range that is sufficient for general-purpose chargers, a two-stage structure composed of isolated power factor correction (PFC) and non-isolated DC/DC converters can be considered. Given that non-isolated converters can be designed to achieve high efficiency, the entire efficiency of the charger is determined by the efficiency of the isolated PFC converter. Most of the topologies available for isolated PFC converters use a current-fed structure. However, this structure suffers from serious voltage spikes in the primary switches caused by transformer leakage inductance, and auxiliary snubber circuits are required to suppress the voltage spikes. High-voltage-rating devices are still required, which pose an obstacle to obtaining good efficiency and increased switching frequency [19]-[25]. Another method for isolated PFC converters is the valley-fill circuit based on SRC. This method has good topological merits due to the voltage-fed structure, but it suffers from high current stress caused by resonant operation and has various problems caused by a low switching frequency at a light load [26]. Several isolated PFC approaches that use an asymmetrical dual active bridge (ADAB) converter have been presented; the ADAB structure has various operational modes [27]. Among these modes, the "boost discontinuous conduction mode (DCM) operation" is adequate in reducing the switching loss of the primary switch due to ZV-ZCS switching characteristics and can provide the availability of IGBT and MOSFET as switching devices. However, this operational mode has the disadvantages of low power factor and high switching loss of the secondary switch, which pose obstacles to high-power designs, such as EV battery chargers.

This paper presents an isolated PFC converter design based on the ADAB structure. By operating the converter under the boost-DCM operation, the primary switches can be operated at a fixed frequency with a 50% duty ratio, which leads to good switching conditions of zero-voltage turn-on and zero-current turn-off. All harmonic and output controls are performed by secondary switches, and the harmonic modulation technique [28] is adopted to obtain a near-unity power factor without input current monitoring. It provides a simple control scheme so that a simple digital controller is available. To verify the feasibility of the proposed circuit, the circuit is implemented and tested using a 3.3 kW charger.

II. Proposed Converter

Fig. 1 presents a schematic of the charger composed of the proposed isolated PFC converter with harmonic modulation technique and a buck converter for battery charging control. Galvanic isolation and harmonic regulation are accomplished in the PFC stage, and charging control is performed by the simple non-isolated buck converter. Primary switches M_1–M_4 are high-frequency inverter-operated at a fixed frequency and

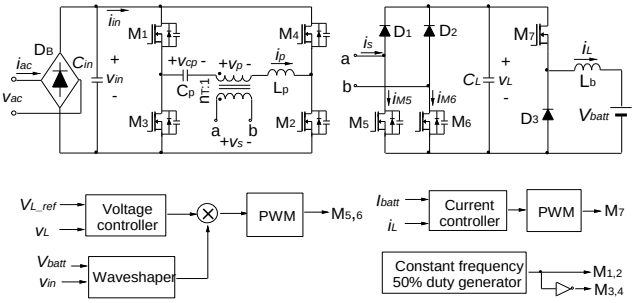


Fig. 1. Schematic of a charger composed of the proposed isolated PFC converter with harmonic modulation and a buck converter.

a 50% duty ratio. All controls of the output voltage and line current regulations of the PFC stage are performed only by secondary switches M_5 and M_6. A detailed operational analysis is provided as follows.

A. Mode Analysis of the Proposed PFC Converter

Fig. 2 shows the key waveforms of the proposed PFC converter, and Fig. 3 presents its operational mode diagrams. Prior to the analysis, the following assumptions are made.

- Link voltage refers to the primary side v_L/n_T being always higher than the rectified input voltage v_{in}, where n_T is the transformer turns ratio.
- Transformer secondary-side current i_s is zero before mode 1.
- DC-blocking capacitor C_p is sufficiently large to be ignored.

Mode 1 ($t_0 \le t < t_1$): When M_1, M_2, M_5, and M_6 are turned on at t_0 simultaneously, primary current i_p flows through M_1, M_2, inductor L_p, and the transformer primary side. Secondary current i_s flows through M_5, M_6-body diode, and the transformer secondary side. Given that the transformer secondary side is shorted by M_5 and M_6, i_s is increased from zero with the slope of $V_{in}/(n_T L_p)$, and magnetizing current i_{Lm} is kept constant with the initial condition of $i_{Lm}(t_0)$. i_p is equal to the sum of i_{Lm}, and the secondary current refers to the primary $n_T i_s$. They can be expressed as

$$i_s(t) = (v_{in} / n_T L_p)(t - t_0) \quad , \tag{1}$$

$$i_{Lm}(t) = i_{Lm}(t_0) \quad , \tag{2}$$

$$i_p(t) = i_{Lm}(t_0) + (v_{in} / L_p)(t - t_0) \quad . \tag{3}$$

Mode 2 ($t_1 \le t < t_2$): When M_5 and M_6 are turned off, mode 2 begins. The current path in the primary side during mode 2 is maintained as that of mode 1, but the current path in the secondary side forms through D_5 and M_6-body diode. Accordingly, the voltage applied across the transformer primary side v_p becomes V_L/n_T, and i_s decreases with the slope of $(v_{in}\text{-}V_L/n_T)/(n_T L_p)$. During mode 2, i_s, i_{Lm}, and i_p can be expressed as follows:

$$i_s(t) = \frac{v_{in}}{n_T L_p} d_p T_s + \frac{v_{in} - V_L / n_T}{n_T L_p}(t - t_1) \quad , \tag{4}$$

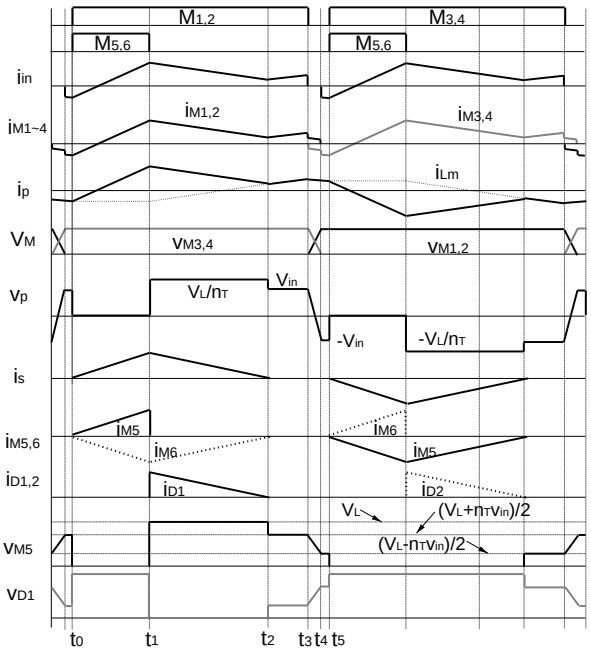


Fig. 2. Key waveforms of the proposed PFC converter.

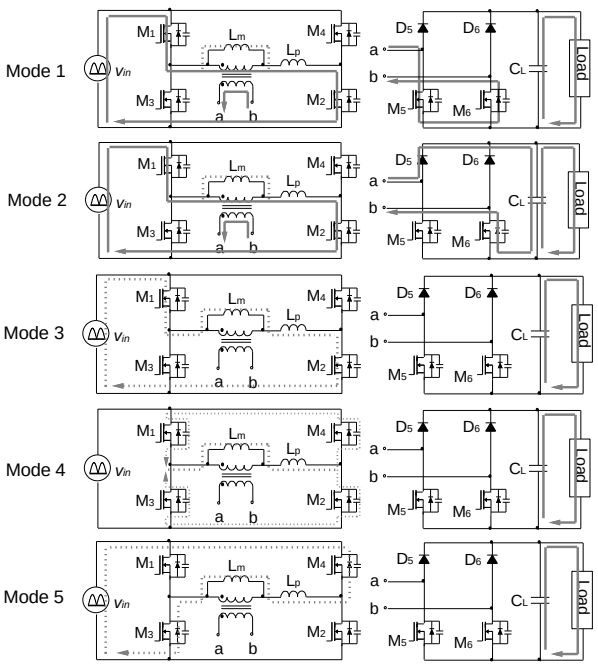


Fig. 3. Mode diagrams of the proposed PFC converter.

$$i_{Lm}(t) = i_{Lm}(t_1) + \frac{V_L / n_T}{L_m}(t - t_1) = i_{Lm}(t_0) + \frac{V_L / n_T}{L_m}(t - t_1) \quad (5)$$

$$i_p(t) = i_{Lm}(t_0) + \frac{V_L / n_T}{L_m}(t - t_1) + \frac{v_{in}}{L_p} d_p T_s + \frac{v_{in} - V_L / n_T}{L_p}(t - t_1) \quad (6)$$

where d_p is the duty ratio of M_5 and M_6. Mode 2 continues until i_s is reduced to zero, and its time duration can be derived from Eq. (4) as follows:

$$t_2 - t_1 = d_{p2} T_s = (v_{in} / (V_L / n_T - v_{in})) d_p T_s \quad , \quad (7)$$

where d_{p2} is the time ratio of mode 2.

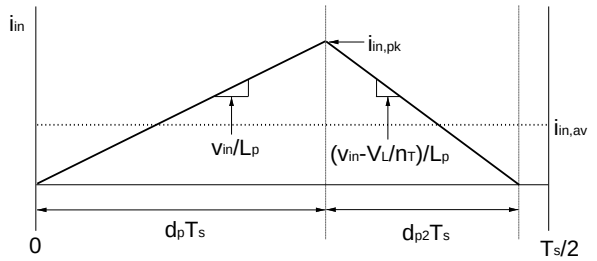


Fig. 4. Input current, excluding the magnetizing current, during one switching cycle.

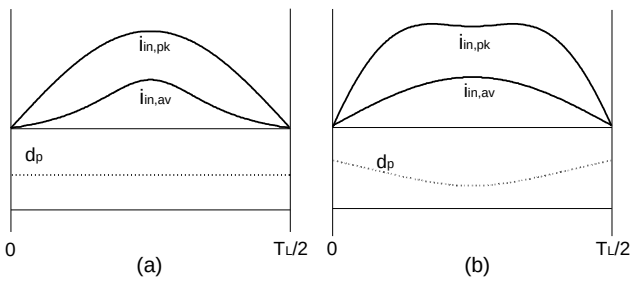


Fig. 5. Inductor current envelope and line current waveform of conventional DCM operation (a) and those adopting a harmonic controller (b).

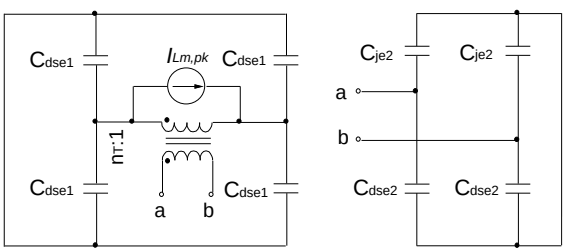


Fig. 6. Equivalent circuit during dead times between gate signals of the primary side switches.

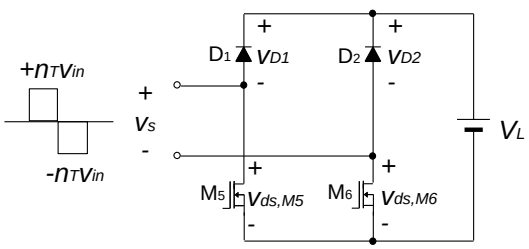


Fig. 7. Equivalent circuit in the secondary side when the drain-source voltages of all primary switches change from zero to v_{in} or from v_{in} to zero.

Mode 3 ($t_2 \le t < t_3$): During this mode, only the magnetizing current circulates through M_1 and M_3, as shown in the mode diagram of mode 3 in Fig. 2. v_p is changed to input voltage v_{in}. Hence, i_s, i_{Lm}, and i_p can be expressed as

$$i_s(t) = 0 \quad , \quad (8)$$

$$i_{Lm}(t) = i_{Lm}(t_2) + (v_{in} / L_m)(t - t_2) = i_p(t) \quad . \quad (9)$$

The initial condition of i_{Lm} in this mode can be derived from Eqs. (5) and (7) as follows:

$$i_{Lm}(t_2) = i_{Lm}(t_0) + v_{in}V_L/(L_m(V_L - n_T v_{in}))d_p T_s \quad . \tag{10}$$

Modes 4 and 5 ($t_3 \le t < t_5$): When the primary switches of M_1 and M_2 are turned off, the magnetizing current is used for the potential exchange of all drain-to-source voltages in primary switches. After completing the potential change, the magnetizing current starts to flow through the body diodes of M_3 and M_4 so that the ZVS condition can be achieved. Assuming that the total duration of modes 4 and 5 (i.e., the dead time between upper and lower switches) is short enough that the magnetizing current is maintained at a constant value, i_{Lm} during these two modes can be written as

$$i_{Lm}(t) \approx -i_{Lm}(t_0) \quad . \tag{11}$$

Under this assumption, the initial condition of $i_{Lm}(t_0)$ can be derived using Eqs. (9), (10), and (11) as follows:

$$i_{Lm}(t_0) = -(v_{in}/2L_m)T_s \quad . \tag{12}$$

B. Harmonic Controller in the Proposed PFC Converter

Given that the magnetizing current is the circulating current whose value averaged over the switching cycle is zero, it does not affect the switching average value of input current i_{in}. Thus, analysis of the input current waveform can be performed by removing the magnetizing current. Fig. 4 shows the input current excluding the magnetizing current in the proposed converter. The peak and switching average values of input currents $i_{in,pk}$ and $i_{in,av}$ can be derived as

$$i_{in,pk}(t) = (v_{in}/L_p)d_p T_s \quad , \tag{13}$$

$$i_{in,av}(t) = (d_p^2 v_{in} T_s/L_p)(V_L/(V_L - n_T v_{in})) \quad . \tag{14}$$

Fig. 5(a) presents the inductor current envelope and the line current waveform of conventional DCM operation whose d_p is constant. The envelope of the input current follows the input voltage waveform, but the switching average value of the input current that is equal to the rectified line current is distorted. This characteristic is similar to that of a conventional DCM PFC converter. To obtain a pure sinusoidal line current waveform, the power factor should be unity, that is, the output power is equal to the apparent input power. This condition can be expressed as

$$P_o = I_{ac,rms}V_{ac,rms} \quad . \tag{15}$$

Considering that $I_{ac,rms}V_{ac,rms}$ is equal to $I_{in,pk}V_{in,pk}/2$, $I_{in,pk}$ can be derived as

$$I_{in,pk} = 2P_o/V_{in,pk} \quad . \tag{16}$$

Thus, the line current for the unity power factor is derived as follows:

$$i_{ac} = (2P_o/V_{in,pk})\sin\omega_L t \quad , \tag{17}$$

where ω_L is the angular frequency of line voltage. If the switching average value of input current $i_{in,av}$ in Eq. (14) is equal to the absolute value of i_{ac} in Eq. (17), then the line current can have a unity power factor, which can be accomplished by modulating duty ratio d_p. Given that v_{in} can be written as $v_{in}=V_{in,pk}|\sin\omega_L t|$, the duty ratio for the unity power factor can be derived from Eqs. (14) and (17) as follows:

$$d_p = \sqrt{2L_p P_o/T_s V_{in,pk}^2} \times \sqrt{1 - n_T v_{in}/V_L} \equiv D_p \times M_f \quad . \tag{18}$$

The modulated duty ratio is composed of a constant value of D_p generated by the voltage controller and modulation factor M_f for improving the power factor. Fig. 5(b) shows a case that adopts this technique. As shown in the figure, sinusoidal line current can be obtained by modulating d_p.

III. Loss Analysis and Design

A. Effective Parasitic Capacitances of Switching Devices

Effective capacitances of semiconductor devices, such as drain-source capacitance of MOSFET and junction capacitance of diodes, should be derived as a function of the voltage applied across the semiconductor devices to analyze the performance of the proposed converter. The drain-source capacitance of MOSFET varies in accordance with blocking voltage v_{ds} and is approximately expressed as

$$c_{ds}(v_{ds}) \approx C_T\sqrt{V_T/v_{ds}} \quad , \tag{19}$$

where C_T is the drain-source capacitance at test voltage V_T. The energy stored in the drain-source capacitance while the drain-source voltage rises from 0 to V_{ds} is

$$W_{Cds} = \int_0^{V_{ds}} v_{ds}C_T\sqrt{V_T/v_{ds}}\,dv_{ds} = \frac{1}{2}\times\frac{4}{3}c_{ds}(V_{ds})\times V_{ds}^2 \quad . \tag{20}$$

From Eq. (20), the effective capacitances of MOSFET when the drain-source voltage is increased from 0 to V_{ds} can be derived as

$$C_{dse} = \frac{4}{3}c_{ds}(V_{ds}) = \frac{4}{3}C_T\sqrt{V_T/V_{ds}} = 1.33C_T\sqrt{V_T/V_{ds}} \quad . \tag{21}$$

Simply, the drain-source capacitance calculated at the center of varying voltages can be used for effective capacitance, which is

$$C_{dse} = c_{ds}((V_1+V_2)/2) = C_T\sqrt{V_T/((V_1+V_2)/2)} \quad , \tag{22}$$

where V_1 and V_2 denote the start and end voltages, respectively. By using Eq. (22), the effective drain-source capacitances of MOSFET when the drain-source voltage is increased from 0 to V_{ds} can be written as follows:

$$C_{dse} = 1.41C_T\sqrt{V_T/V_{ds}} \quad . \tag{23}$$

C_{dse} in Eq. (23) is only 6% larger than that in Eq. (21). Hence, Eq. (23) can be used to determine the effective capacitances and is more useful when V_1 is not zero. The effective junction capacitance of diodes can also be determined with Eq. (23).

B. L_p for DCM Operation

To guarantee the DCM operation of the transformer primary current, the following condition should be satisfied:

$$d_{p2}T_s = (v_{in}/(V_L/n_T - v_{in}))d_p T_s \le (1/2 - d_p)T_s \tag{24}$$

By using this inequality and the modulated duty ratio given in Eq. (18), L_p that meets the DCM condition can be written as

$$L_p \le T_s V_{in,pk}^2 (V_L - n_T v_{in}) / 8 P_o V_L \quad . \tag{25}$$

The worst case occurs at the maximum output power $P_{o,max}$ and peak line voltage $V_{in,pk}$. Thus, the maximum inductor value to meet the DCM condition over the entire line and load voltages can be derived as

$$L_{p,\max} = T_s V_{in,pk}^2 (V_{LT} - n_T V_{in,pk}) / 8 P_{o,\max} V_L \quad . \tag{26}$$

C. L_m Selection for Soft Switching

Fig. 6 presents the equivalent circuit during dead times between gate signals of the primary side switches under the assumption that the input and output capacitors of C_{in} and C_L are sufficiently large to be shorted during dead times. Given that the magnetizing current during dead times between gate signals of upper and lower switches T_{dead} is used for ZVS currents of primary and secondary side switches, the ZVS condition can be written as

$$I_{Lm,pk} = \frac{v_{in}}{2L_m} T_s \ge \frac{v_{in}(4C_{dse1} + n_T^2(2C_{dse2} + 2C_{je2}))}{T_{dead}} \quad . \tag{27}$$

Hence, L_m for ZVS can be calculated as

$$L_m \le T_{dead} T_s / (8C_{ds1e} + 4n_T^2 (C_{dse2} + C_{je2})) \equiv L_{m,\max} \quad . \tag{28}$$

Considering that the drain-source voltages of all primary switches experience the voltage change of zero to v_{in} or v_{in} to zero, the effective capacitance of primary switches C_{dse1} can be established as

$$C_{dse1} = 1.41 C_T \sqrt{V_T / v_{in}} \quad . \tag{29}$$

The change in the drain-source voltage of the primary switches appears on the transformer secondary side and can be expressed with a variable voltage source that varies between $+n_T v_{in}$ and $-n_T v_{in}$, as shown in Fig. 7. The voltage applied across secondary devices during dead times can be derived as

$$v_{D1} = (V_L + v_s)/2 = v_{ds,M6} \quad , \tag{30}$$

$$v_{D2} = (V_L - v_s)/2 = v_{ds,M5} \quad . \tag{31}$$

In cases where complete ZVS is accomplished, transformer secondary voltage v_s is changed between $+n_T v_{in}$ and $-n_T v_{in}$ so that the center voltage experienced by secondary devices is $V_L/2$. Therefore, the effective capacitances of secondary MOSFETs C_{dse2} and diodes C_{je2} can be written as follows:

$$C_{dse2} = 1.41 C_T \sqrt{V_T / V_L} \quad , \tag{32}$$

$$C_{je2} = 1.41 C_{Tj} \sqrt{V_{Tj} / V_L} \quad , \tag{33}$$

where C_{Tj} is the junction capacitance at test voltage V_{Tj}. Investigation of Eqs. (28), (29), (32), and (33) indicates that $L_{m,max}$ is dependent on the line voltage, and a very small magnetizing inductance is required to meet ZVS under the entire line voltage magnitude. Thus, an appropriate ZVS start voltage V_{is} defined by the minimum input voltage to meet the ZVS of primary switches should be selected by considering the effect of the switching loss caused by the output capacitances of switching devices.

D. Loss Analysis

Assuming that the switching frequency is sufficiently high that all parameters during the switching cycle are regarded as time-invariant ones, loss analysis can be performed at each switching cycle.

1) Losses of Primary Side Switches

The switching losses in the primary switches are caused by the device turn-off time t_f and the drain-source capacitance of MOSFET because the transformer primary current has a DCM operation. The switching loss due to the drain-source capacitance of MOSFET $P_{Cds1}[n]$ and that due to turn-off time $P_{off1}[n]$ generated by a single switch in the n_{th} switching cycle can be written as follows:

$$P_{Cds1}[n] = C_{dse1}[n] v_{in}[n]^2 f_s / N \quad , \tag{34}$$

$$P_{off1}[n] = I_{Lm,pk}[n] v_{in}[n] t_f f_s / 2N \quad , \tag{35}$$

where

$$C_{dse1}[n] = 1.41 C_T \sqrt{V_T / v_{in}[n]}$$

$$I_{Lm,pk}[n] = (v_{in}[n] / 2L_m) T_s$$

$$v_{in}[n] = V_{in,pk} \sin \omega_L n T_s \quad .$$

N is the total switching number of the PFC converter during half of the line cycle $T_L/2$ and is calculated by int($T_L/T_s/2$). Assuming that L_m is sufficiently large that the magnetizing current is ignored, the RMS switch current in the n_{th} switching cycle can be derived as follows:

$$I_{sw,rms}[n] = I_{sw,pk}[n] \sqrt{(d_p[n] + d_{p2}[n])/3} \quad , \tag{36}$$

where

$$I_{sw,pk}[n] = (v_{in}[n] / L_p) d_p[n] T_s$$

$$d_p[n] = \sqrt{2L_p P_o / T_s V_{in,pk}^2} \times \sqrt{1 - n_T v_{in}[n] / V_L}$$

$$d_{p2}[n] = (v_{in}[n] / (V_L / n_T - v_{in}[n])) d_p[n] \quad .$$

With this expression, the conduction loss generated by a single switch in the n_{th} switching cycle can be written as follows:

$$P_{con1}[n] = I_{sw,rms}[n]^2 R_{ds} / N \quad . \tag{37}$$

Therefore, the total loss of the primary switches over the entire line cycle can be derived as

$$P_{SW1} = 4 \sum_{n=1}^{N} (P_{Cds1}[n] + P_{off1}[n] + P_{con1}[n]) \quad . \tag{38}$$

2) Losses of Secondary Side Switches

Fig. 2 depicts the voltages applied across the secondary switches and diodes in key waveforms. The voltages experience many potential changes during the single switching period, but potential changes at t_0 and t_1 contribute to the switching losses because others are not significant. From Eq. (19), the effective capacitances of secondary switches at t_0 C_{dse20} and at t_1 C_{dse21} can be written as

$$C_{dse20}[n] = 1.41 C_T \sqrt{V_T / [(V_L + n_T v_{in}[n])/2]} \quad , \tag{39}$$

$$C_{dse21}[n]=1.41C_T\sqrt{V_T/V_L}. \quad (40)$$

The switching loss of a single secondary switch caused by the drain-source capacitance of MOSFET $P_{Cds2}[n]$ in the n_{th} switching cycle can be written as follows:

$$P_{Cds2}[n]=\frac{1}{N}\left(\frac{1}{2}C_{dse20}[n]\left(\frac{n_T v_{in}[n]+V_L}{2}\right)^2+\frac{1}{2}C_{dse21}[n]V_L^2\right)f_s \quad (41)$$

The switching loss of a single secondary switch caused by turn-off time $P_{off2}[n]$ is

$$P_{off2}[n]=(I_{sw,pk}[n]/n_T)V_L t_f f_s/2N \quad . \quad (42)$$

The conduction loss of MOSFET is produced by the on-resistance and on-drop voltage of the body diode. According to Fig. 2, the conduction loss of a single secondary switch in the n_{th} switching cycle can be derived as follows:

$$P_{con2}[n]=(I_{M5,channel,rms}[n]^2R_{ds}+I_{M5,diode,avg}[n]V_{on})/N, \quad (43)$$

where

$$I_{M5,channel,rms}[n]=(I_{sw,pk}[n]/n_T)\sqrt{d_p[n]/3}$$

$$I_{M5,diode,avg}[n]=(I_{sw,pk}[n]/n_T)(d_p[n]+d_{p2}[n])/2.$$

Thus, the total loss of secondary switches over the entire line cycle can be derived as

$$P_{SW2}=2\sum_{n=1}^{N}(P_{Cds2}[n]+P_{off}[n]+P_{con2}[n]). \quad (44)$$

3) Losses of Secondary Side Diodes

Diode loss is composed of the switching loss due to junction capacitance and the conduction loss due to on-drop voltage. Similar to the case of MOSFET, the dominant switching loss occurs at t_0 and t_1. The effective capacitances of diodes at t_0 C_{je20} and at t_1 C_{je21} can be written as

$$C_{je20}[n]=1.414C_{Tj}\sqrt{V_{Tj}/[(3V_L-n_T v_{in}[n])/2]}, \quad (45)$$

$$C_{je21}[n]=1.414C_{Tj}\sqrt{V_{Tj}/V_L} \quad . \quad (46)$$

The switching loss of a single diode caused by junction capacitance $P_{Cj2}[n]$ in the n_{th} switching cycle can be written as follows:

$$P_{Cj2}[n]=\frac{1}{N}\left(\frac{1}{2}C_{je20}[n]\left(\frac{n_T v_{in}[n]+V_L}{2}\right)^2+\frac{1}{2}C_{je21}[n]V_L^2\right)f_s \quad (47)$$

Given that the switching average current of diodes is

$$I_{D1,avg}[n]=(I_{sw,pk}[n]/n_T)d_{p2}[n]/2, \quad (48)$$

the conduction loss generated by a single diode in the n_{th} switching cycle can be written as follows:

$$P_{con2\_D}[n]=I_{D1,avg}[n]V_{on}/N \quad . \quad (49)$$

Therefore, the total loss of diodes over the entire line cycle can be derived as

$$P_{D2}=2\sum_{1}^{N}(P_{Cj2}[n]+P_{con2\_D}[n]) \quad . \quad (50)$$

4) Losses of Transformer and Inductor

The core loss occurring in the n_{th} switching cycle can be written as

$$P_{T,core}[n]=(a(f_s/10^3)^c B_T[n]^d\times V_{eT}/10^3)/N \quad , \quad (51)$$

where $B_T[n]$ is the flux swing in kilo-Gauss and V_{eT} denotes the core volume in cm^3 [29]. In addition, *a*, *c*, and *d* represent coefficients based on the core materials provided by the core manufacturers. The flux swing of the transformer core $B_T[n]$ is proportional to $d_{p2}[n]T_s$ and can be written as follows:

$$B_T[n]=B_{T,design}d_{p2}[n]T_s/T_{design} \quad , \quad (52)$$

where $B_{T,design}$ denotes the flux swing designed at specific time T_{design}. The primary and secondary RMS currents of the transformer are written as

$$I_{p,rms}[n]=\sqrt{2}I_{sw,rms}[n] \quad , \quad (53)$$

$$I_{s,rms}[n]=\sqrt{2}I_{sw,rms}[n]/n_T, \quad (54)$$

so the copper loss in the n_{th} switching cycle can be derived with the primary and secondary winding resistances of R_p and R_s as follows:

$$P_{T,copper}[n]=(I_{p,rms}[n]^2R_p+I_{s,rms}[n]^2R_s)/N \quad . \quad (55)$$

Similarly, the core and copper losses of the primary inductor in the n_{th} switching cycle can be derived with the core volume V_{ei} in cm^3, the flux swing $B_i[n]$ in kilo-Gauss, and the winding resistance of inductor R_L. They are expressed as

$$P_{I,core}[n][W]=(a(f_e/10^3)^c B_i[n]^d\times V_{ei}/10^3)/N \quad , \quad (56)$$

$$P_{I,copper}[n]=I_{p,rms}[n]^2R_L/N \quad , \quad (57)$$

where

$$B_i[n]=B_{i,design}I_{sw,pk}[n]/I_{design}$$

and f_e is the effective operating frequency of the primary inductor, which is equal to $2f_s$. $B_{i,design}$ denotes the flux swing designed at specific inductor current I_{design}. Therefore, the total loss of the transformer and the primary inductor over the entire line cycle is

$$P_M=\sum_{1}^{N}(P_{T,core}[n]+P_{T,copper}[n]+P_{I,core}[n]+P_{I,copper}[n]). \quad (58)$$

5) Conduction Loss of Bridge Diode

The conduction loss of the bridge diode with the on-drop voltage of $V_{on,BR}$ in the n_{th} switching cycle can be expressed as

$$P_{con,BR}[n]=2I_{in,av}[n]V_{on,BR}/N \quad , \quad (59)$$

and the switching average value of input current is expressed as

$$I_{in,av}[n]=(d_p[n]^2 v_{in}[n]T_s/L_p)(V_L/(V_L-n_T v_{in}[n])). \quad (60)$$

Thus, the conduction loss of the bridge diode can be determined as follows:

$$P_{con,BR} = \sum_{1}^{N} P_{con,BBR}[n] \quad (61)$$

6) Peak Current of the Primary Inductor

By referring to Fig. 4, the peak current of the primary inductor in the proposed converter with the harmonic modulator can be written as

$$i_{p,pk}(t) = \frac{v_{in}}{L_p} d_p T_s = \frac{v_{in} T_s}{L_p} \sqrt{\frac{2L_p P_o}{T_s V_{in,pk}^2}} \times \sqrt{1 - \frac{V_{in,pk}}{V_L / n}}, \quad (62)$$

where L_p is the value selected by Eq. (26). If the converter is under the conventional DCM operation without the harmonic modulator, then the operational duty ratio is a constant value over the entire line cycle, which can be derived as follows:

$$D_p = \sqrt{\frac{2L_p}{(R_o / n_T^2)(T_s / 2)} \frac{(V_L / n_T)^2 - V_{in,rms}(V_L / n_T)}{V_{in,rms}^2}}. \quad (63)$$

By using the DCM condition given by Eqs. (24) and (63), the primary inductor for the conventional DCM operation L_{pc} can be derived as

$$L_{pc} \le \frac{(V_L / n_T - V_{in,rms})^2}{4(V_L / n_T)^2} \frac{V_{in,rms}^2}{(V_L / n_T)^2 - V_{in,rms}(V_L / n_T)} \frac{R_o T_s}{4 n_T^2}, \quad (64)$$

where R_o is the effective load resistor of the PFC converter. Thus, the peak current of the primary inductor in the conventional case $i_{pc,pk}$ can be obtained as follows:

$$i_{pc,pk}(t) = \frac{v_{in} T_s}{L_{pc}} \sqrt{\frac{2L_p}{(R_o / n_T^2)(T_s / 2)} \frac{(V_L / n_T)^2 - V_{in,rms}(V_L / n_T)}{V_{in,rms}^2}}. \quad (65)$$

The next chapter shows that the harmonic modulator contributes to the reduction of the current stress of switching devices because a high value can be used for the primary inductor and a low operational duty ratio can be obtained at the peak line voltage where the maximum current stress occurs.

IV. Design and Experimental Results

A prototype PFC converter is designed with the following specifications.

- Grid characteristics: 3.3 kW/15 A/60 Hz
- Maximum output power: 3.3 kW
- Input voltage: 220 V_{rms}±15%
- Output voltage: 500 V

Fig. 8 presents the experimental prototype for validation excluding the output electrolytic capacitor. Table 1 shows the key component list of the prototype PFC converter together with the buck converter for test use. In this design, the ZVS start voltage V_{is} is set to 60 V, and L_m is calculated as 492 μH from Eqs. (28), (29), (32), and (33) and the selected switching devices in Table 1. For the implementation, 500 μH is used.

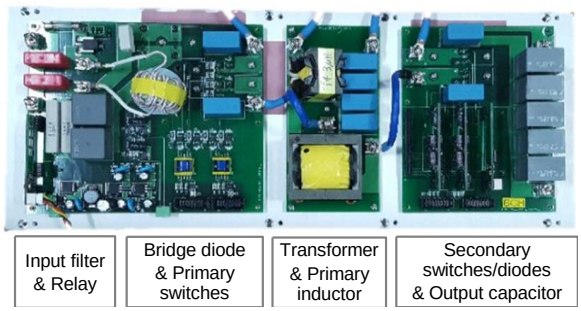
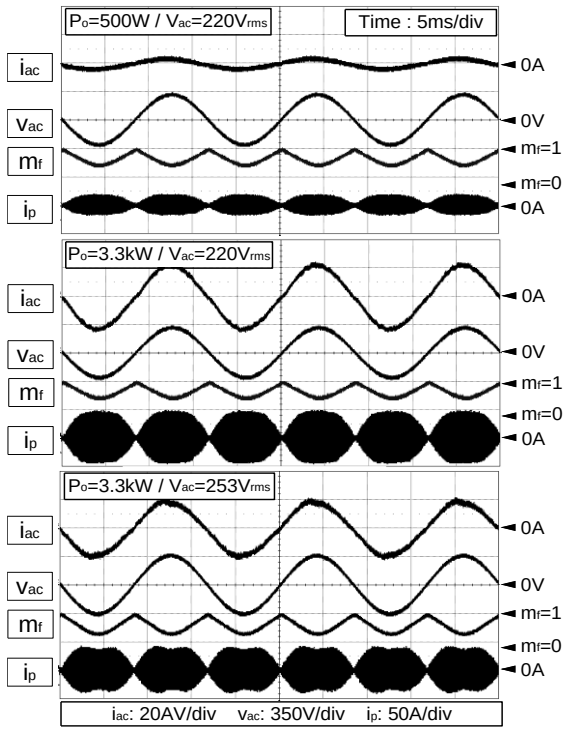


Fig. 8. Experimental prototype for performance validation.

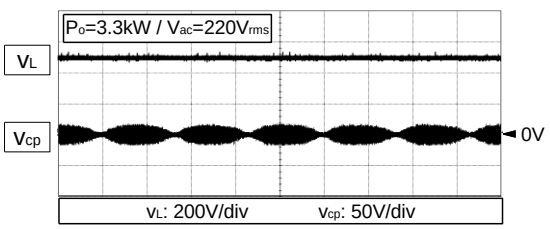
TABLE I
Key Component List of the Prototype Converter

Component	Value
M_1~M_7	IPW65R041CFD×1
D_1~D_3	FFH50US60S×1
C_L	1020μF EL capacitor//50uF film capacitor
C_p	8μF
f_s	50kHz
L_p	14.3μH (Core: PQ40/40)
L_b	900μH (Core: CH467125×2)
Transformer	L_m =500μH/L_{lkg}=5.7μH/n_T =0.89 (Core: 47228EC)
Controller	DSP TMS320F28335

Given that the peak value of the input voltage occurs at the maximum input voltage of 253 V_{rms}, L_p is calculated as 20.4 μH. Considering the leakage inductance of the transformer, 14.3 μH is used for L_p. Fig. 9(a) presents the measured waveforms of line voltage v_{ac}, line current i_{ac}, primary current i_p, and modulation factor M_f in accordance with load and line voltage variations. Fig. 9(b) displays the output voltage of the PFC converter v_L and the DC-blocking capacitor voltage v_{cp}. Modulation factor M_f is plotted using a digital-to-analog converter in the DSP controller. The figure shows that clean sinusoidal current waveforms can be obtained under wide load ranges by changing operational duty ratios continuously in accordance with M_f. The maximum current of the primary inductor at V_{ac}=220 V_{rms} is calculated as 45.6 A by using the designed parameters and Eq. (62). The measured current of Fig. 9 also has a similar value. If the converter is designed to have the conventional DCM operation without the harmonic modulator, then the primary inductor and operational duty ratio are calculated as 9.4 μH and 0.258 from Eqs. (63) and (64), respectively. Accordingly, the maximum current of the primary inductor becomes 169.7 A, which is much larger than that of the proposed converter with the harmonic modulator. Moreover, the prototype design guarantees normal operation under the given line voltage range. Fig. 10 presents the switching waveforms in accordance with load changes. They agree well with the theoretical analysis, except for the parasitic resonance due to pattern inductances in the printed circuit board. Fig. 11 shows the ZVS status in the primary switches in accordance with the input voltage magnitudes. In the figure, turn-on and turn-off instants of M_1 are indicated



(a)



(b)

Fig. 9. Measured waveforms in accordance with load and line voltage variations.

with arrows. ZVS is well accomplished from the designed ZVS start voltage. Fig. 12 displays the measured waveforms of the buck converter. The cascaded structure of the proposed PFC converter and the buck converter can cope with a wide output voltage range. Fig. 13 presents the measured power factor and efficiency plots in accordance with load variations. A high power factor can be obtained under a wide load range, and the power factor is over 0.983 at the output power of more than 1 kW. In addition, the efficiency is recorded as 95.6% at V_{ac}=220 V_{rms} and P_o=3.3 kW, and the maximum efficiency of 96.2% occurs at V_{ac}=253 V_{rms} and P_o=3.0 kW. The overall efficiency including the buck converter can be obtained as 94.8% at V_{ac}=220 V_{rms} and P_o=3.3 kW. Fig. 14 shows the measured harmonics and total harmonic distortion (THD) of the input current at the rated condition. THD is well regulated below 5%. Fig. 15 depicts the loss distribution of the proposed PFC converter calculated using the loss equations in Section III. The calculated efficiency is 94.5% at V_{ac}=220 V_{rms} and P_o=3.3 kW, which is similar to the measured efficiency. The switching device losses are

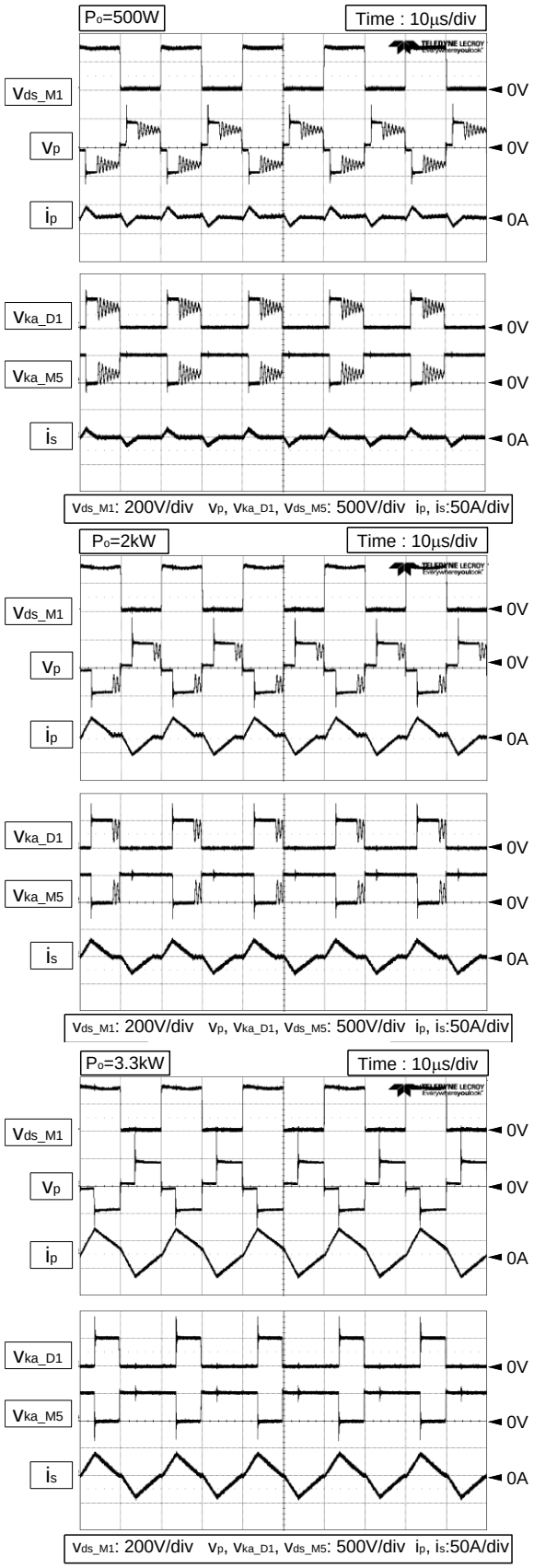


Fig. 10. Switching waveforms in accordance with load changes at V_{ac}=220 V_{rms}/V_L=500 V.

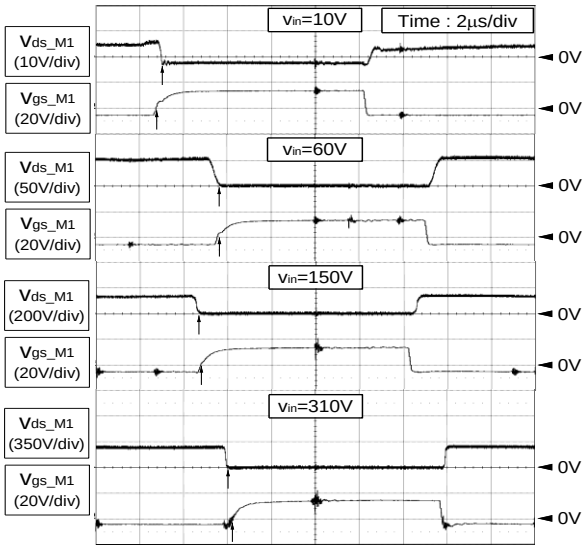


Fig. 11. ZVS status of primary switches in accordance with input voltage magnitudes.

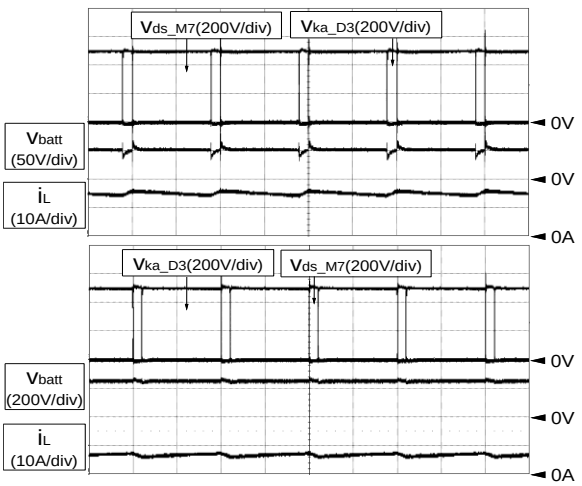


Fig. 12. Measured waveforms of the buck converter.

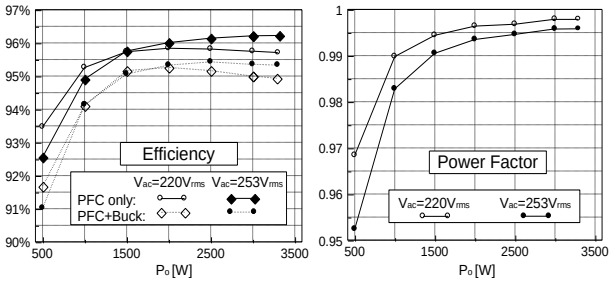


Fig. 13. Measured power factor and efficiency plots in accordance with load variations.

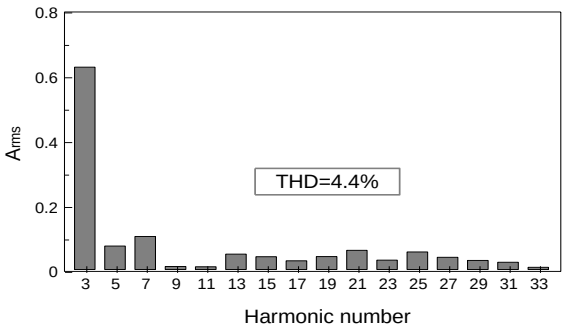


Fig. 14. Measured harmonics and total harmonic distortion (THD) of the input current at the rated condition.

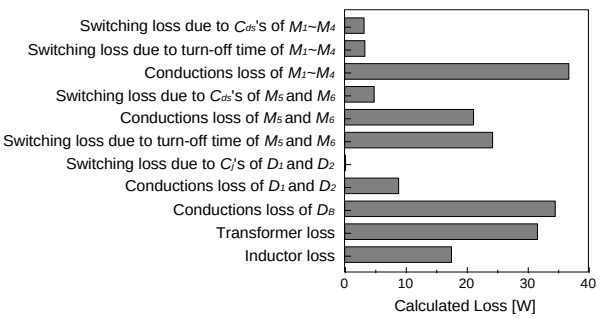


Fig. 15. Calculated losses at V_{ac}=220 V_{rms}/P_o=3.3 kW.

TABLE II
PERFORMANCE COMPARISON TABLE

	CF-FB PWM [21]	**CF-FB PWM [22]**	**CF-FB PWM [23]**	**CF-FB PWM [24]**	**VF-FB PFM SRC [26]**	**Proposed**
P_o	1kW	1kW	3kW	3kW	1.7kW	3.3kW
V_{ac} ($V_{ac,max}$)	220V (240V)	220V (-)	220V (-)	208V (-)	220V (242V)	220V (253V)
V_o	380V	384V	400V	400V	62-82V	500V
f_s	37.5kHz	87kHz	50kHz	10kHz	Max. 125kHz	50kHz
Switching device structure (Except for bridge diode)	4 switch (1200V MOSFET) 5 diode (FRD)	6 switch (500V MOSFET) 4 diode (FRD)	8 switch (600V MOSFET) 4 diode (FRD)	5 switch (650V IGBT) 9 diode (FRD)	6 switch (600V IGBT) 8 diode (FRD)	6 switch (650V MOSFET) 2 diode (FRD)
Transformer (Structure)	43:40 (-)	1:1 (-)	2:1 (-)	58:66 (Two EE85)	1:1 (Two PQ4040)	1:1.1 (47228EC)
Inductor	1.3mH	500μH	350μH×2	650μH	5.5μH×2	17.5μH
Full load efficiency	89.3% @ 220V/1kW	93.6% @ 220V/1kW	Not provided	92.7% @ 208V/3kW	92.1% @ 220V/1.7kW	95.6% @ 220V/3.3kW
Power Factor @ 220V	> 0.985@ over 500W	> 0.995@ over 400W	> 0.99	> 0.984 @ over 874W	0.992 @ .7kW	> 0.990 @ over 1kW
Control method	Current control + Voltage control	Current control + Voltage control	Current control + Voltage control	Current control + Voltage control	Voltage control + Valley-fill control	Voltage control + Harmonic control

TABLE III
EFFICIENCY COMPARISON BETWEEN THE PROPOSED CHARGER AND PREVIOUS WORK

Ref #	Topology	Power conversion type	P_o	Battery charging voltage range	Efficiency @ Battery Voltage	
					DC/DC stage	Charger
[30]	Hybrid (LLC+FB)	DC/DC	3.3kW	250V~450V	97.4% @450V	-
[31]	3-level LLC	DC/DC	6.6kW	225V~ 378V	98.1% @368V	-
[32]	LLC	DC/DC for 3ϕ use(V_{in}=750V)	20kW	300V~550V	98.2% @550V	-
[18]	Resonant PWM	DC/DC	6.6kW	250V~415V	97.4% @360V	95.1% @360V
[28]	DCM PFC+ LLC+Buck	AC/DC	6.6kW	250V~450V	97.2% @400V	94.8% @400V
[33]	SEPIC+LLC	AC/DC	1kW	100V~420V	97.1% @420V	93.5% @420V
Proposed	Isolated PFC+Buck	AC/DC	3.3kW	50V~450V	99.1% @450V	94.8% @450V

calculated as approximately 139.5 W. The conduction losses of the primary switches and bridge diode and the switching losses of the secondary switches account for 70% of the switching device losses. The loss of the transformer and primary inductor is 49.7 W, which accounts for approximately 26.3% of the total loss of 189.2 W. Table II presents performance comparisons between the proposed PFC converter and recently reported topologies. The table shows that the proposed PFC converter is not inferior to recent ones in terms of structure and efficiency. Table 3 displays the efficiency comparison at the charger level. The overall efficiencies of the single-phase chargers in [31] and [32] were not provided, but they can be expected using the PFC converter efficiency of 97.6%, which is the measured data in reference [19]. Using the data, the overall efficiencies of the chargers in [31] and [32] are expected to be 95.1% and 95.7%, respectively. Investigation of the tables indicates that the proposed PFC converter and the charger using PFC and buck converters are not inferior to recent ones in terms of structure and efficiency.

V. CONCLUSIONS

Another candidate for an isolated PFC converter that can be used for EV chargers is proposed based on the ADAB structure. This candidate is unaffected by the parasitic inductance of the transformer due to the voltage-fed structure. The operation is based on DCM, and the harmonic modulation method is applied to overcome the low power factor featured in general DCM operations. All operations, including harmonic regulation and output control, are performed only by secondary switches with a simple control algorithm, which provides another advantage in terms of controller and circuit design. The design equations are established from the operational analysis, and several loss equations are derived for the quantitative analysis of efficiency. Analysis of the operating characteristics of a 3.3 kW prototype shows that a power factor of over 0.983 is recorded at over 1 kW, and efficiency is recorded as approximately 95.6% at V_{ac}=220 V_{rms} and P_o=3.3 kW. Therefore, the proposed circuit can be used in general-purpose battery chargers by configuring it with a simple non-isolated converter.

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