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A Forward-Integrated Buck DC-DC Converter with Low Voltage Stress for High Step-Down Applications

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Abstract

The combination of a buck converter and a forward converter can be considered to accomplish a high step-down non-isolated converter. To decrease the insufficient step-down ratio of a regular buck converter and to distribute switch voltage stress, a forward-integrated buck (FIB) converter is proposed in this paper. The proposed interleaved DC-DC converter provides an additional step-down gain with the help of a forward converter. In addition to its simple structure, the transformer flux reset problem is solved and an additional magnetic core reset winding is not required. The operational principle and an analysis of the proposed FIB converter are presented and verified by experimental results obtained with a 240 W, 150 V/24 V prototype.

Key words: Buck converter, Electromagnetic interference, High step-down DC/DC conversion, Voltage stress

I. INTRODUCTION

Non-isolated high step-down conversion techniques are widely used in DC-DC applications such as battery chargers, distribution power systems and electric vehicles [1]-[4]. Among the non-isolated converters, the conventional buck converter is usually preferred due to its lower voltage stress, lower non-inverting voltage gain and smaller number of reactive components [5], [6]. Among isolated converters, the forward converter is usually preferred at low to medium power levels due to its reduced number of semiconductor components. However, the conventional buck converter suffers from an extremely low duty cycle and high voltage stress for the switches in high step-down applications with a high input voltage [7], [8]. Although a high step-down conversion ratio with a proper duty cycle can be obtained in the conventional forward converter by adjusting the turn-ratio of the transformer, the switch voltage stress is approximately equal to twice the input voltage. In addition, the stored energy in the leakage inductance of the transformer discharges to the switch output capacitor and causes a voltage spike on the switch leading to more electromagnetic interference (EMI). Moreover, the conventional forward converter suffers from transformer flux reset problems especially for higher-input voltages [7]. So far, most of the research on step-down convestion techniques have been carried out to solve the above mentioned problems [8]-[19].

In [8]-[11], coupled inductors are used to provide a high step-down conversion ratio and to extend the duty cycle. However, the voltage stress of the switches in these converters remains high in applications with a high input voltage. In addition, the converter proposed in [8] suffers from a high output current ripple and it has a limitation on the conversion ratio. In [9] and [10], interleaved two-phase derivations of [8] are considered, and the output current ripple is reduced by adding a third winding. However, the circuit complexity is increased. In [11], a single-input dual-output buck is introduced using a coupled inductor. However, there are voltage spikes and a high-frequency ringing across the switches and the freewheeling diode, which can increase the EMI.

A family of high step-down converters based on switched-capacitor schemes is presented in in [12], where the step-down conversion ratio increases exponentially with their orders. However, the application of these converters is limited due to a lack of voltage regulation. In addition, the number of switches

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and diodes is high which leads to a reduction in efficiency and an increase in cost.

In [13]-[18], improved multiple-phase interleaved buck converters are presented. The converters proposed in [13], [14] provide a higher step-down voltage gain and lower voltage stress on the power switches when compared to the conventional buck converter. However, for high input voltage and low output voltage applications, the voltage conversion ratio is not low enough and extremely small operating duty cycles are required, which makes the converter efficiency low. In order to upgrade the step-down conversion ratio, multiphase interleaved buck converters with low voltage stresses on switches and diodes are presented in [15]-[18]. These converters have a higher step-down voltage gain when compared to the converters in [13], [14]. Therefore, the duty cycle is extended and the corresponding conduction losses can be reduced. As a result, the efficiency can be improved. However, these converters use too many components and need at least four active switches. Thus, they are suitable for high output current or high power level applications. In addition, the input and output grounds of the converters proposed in [16]-[18] are separated, which leads to limitations in terms of applications and a complicated control circuit. In [19], a buck converter with a tapped inductor is proposed. However, the operation mode is only the critical conduction mode (CRM).

One way to obtain a high step-down ratio in a non-isolated topology is to insert a dc voltage source into the input of a buck converter as shown in Fig. 1. Accordingly, the voltage gain of the converter is:

$$\frac{V_o}{V_{in}} = D.(1-\frac{V_{dc}}{V_{in}}) \quad (1)$$

where D is the duty cycle of S_1. V_{dc} can be implemented by a capacitor. However, an isolated converter should be added to provide the ampere-second balance of the capacitor. By properly selecting an isolated converter, many advantages such as high step-down capability and distributed voltage stresses can be achieved. To implement the circuit, a buck converter and a forward converter can be simply integrated. As a result, a forward integrated buck (FIB) converter is derived as shown in Fig. 2, where C_1 acts as the V_{dc} of Fig. 1. There are two capacitors in series, which are connected to the DC input voltage like a regular half-bridge converter, where C_1 and C_2 are charged by a DC input voltage with a positive current. The C_1 current is negative when S_1 is turned on, and C_2 current is negative when S_2 is turned on.

The proposed converter uses two active switches where the voltage stress of one switch is equal to the input voltage. However, this switch is turned on at a voltage that is much less than the input voltage. Consequently, its capacitive turn-on losses are reduced. In addition, the mentioned switch turns on under the zero current switching (ZCS) condition. The voltage stress of the other switch is much less than the input voltage. In the proposed converter, the transformer flux reset problem is solved and there is no need to use any reset winding, which leads to a simpler structure. Moreover, the energy stored in the leakage inductance is absorbed by C_2 and is recycled. This paper is organized as follows. The proposed high step-down converter is explained in Section II. Its operational principles and design considerations are presented in Section III, and experimental results are shown in Section IV. Section V presents some concluding remarks.

II. OPERATING PRINCIPLES

In the proposed converter, two active switches are controlled by two PWM pulses that are 180◦ out of phase. The converter has seven distinct operating intervals in a switching period. Fig. 3 shows typical key waveforms at the steady state, and Fig. 4 illustrates the equivalent circuit of the proposed converter for each interval. In order to simplify the analysis, the following assumptions are made.

- All of the active switches and diodes are ideal.
- The capacitors C_1, C_2 and C_o are large enough so that their voltage variations can be ignored.
- L_1 and L_2 are equal and large enough to assume that their currents are approximately constant.

Before the first interval, it is assumed that both of the switches are turned off, the diodes D_3 and D_4 are reversed biased, and the diodes D_1 and D_2 are conducting.

Interval 1 [t_0-t_1]: This interval begins when the switch S_1 turns on and the voltage V_{C1} is applied to the inductor L_{lk}. Therefore, i_{lk} increases linearly from zero. The smooth increment of the current through the inductor L_{lk} ensures the zero current switching (ZCS) turn-on condition for the switch S_1 and the diode D_3. During this interval, the diodes D_4 is reverse biased and S_2 is turned off. This interval ends when the diode D_1 turns off under the ZCS condition. The important equations of this interval are as follows:

$$i_{S1}(t) = i_{lk}(t) = \frac{V_{C1}}{L_{lk}}.(t-t_0) \quad (2)$$

$$i_{D3}(t) = \frac{N_P}{N_S}.i_{S1}(t) \quad (3)$$

$$i_{L1}(t) = i_{L1}(t-t_0) - \frac{V_O}{L_1}(t-t_0) \quad (4)$$

$$i_{L2}(t) = i_{L2}(t-t_0) - \frac{V_O}{L_2}(t-t_0) \quad (5)$$

$$i_{D1}(t) = i_{L1}(t) - \frac{N_P}{N_S}.i_{S1}(t) \quad (6)$$

Interval 2 [t_1-t_2]: During this interval, V_{C1} is applied to L_{lk}+L_m. Therefore, V_{NP} is equal to $V_{C1}.L_m/(L_m+L_{lk})$. During this interval i_{S1} and i_{D3} are obtained as follows:

$$i_{D3}(t) = i_{L1}(t_1) + \frac{V_{C1}.\frac{L_m}{L_m+L_{LK}}.\frac{N_S}{N_P} - V_O}{L_1}.(t-t_1) \quad (7)$$

$$i_{S1}(t) = i_{lk}(t) = i_{D3}(t).\frac{N_S}{N_P} + \frac{V_{C1}}{L_m+L_{LK}}.(t-t_1)\cdot \quad (8)$$

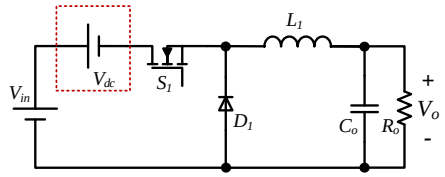


Fig. 1. Buck converter with a series input dc voltage.

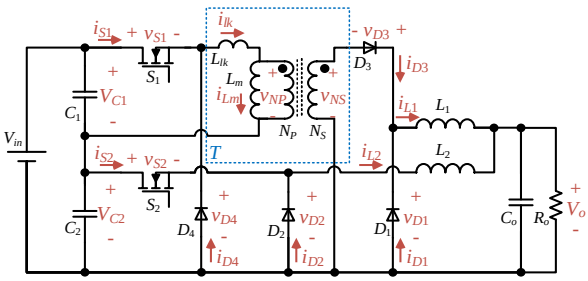


Fig. 2. Proposed forward integrated buck (FIB) converter.

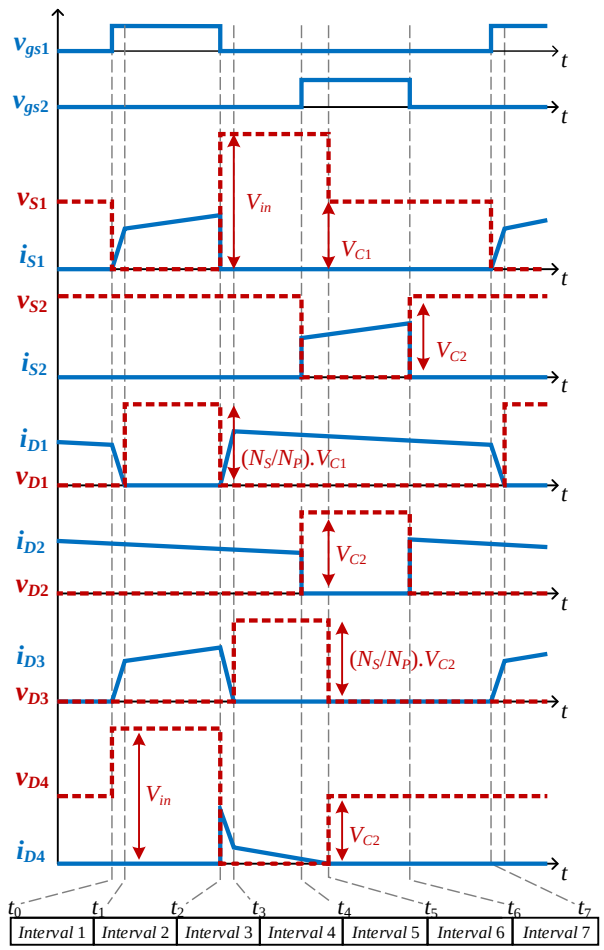


Fig. 3. Key waveforms of the proposed converter.

Interval 3 [t_2-t_3]: At the beginning of this interval, the switch S_1 turns off and the diodes D_4 and D_1 start conducting. By the conduction of D_4, the voltage across S_1 is clamped to V_{in}. The voltage V_{C2} is inversely applied to the inductor L_{lk}, and its current decreases until it reaches $i_{Lm}(t_2)$. In this way, the leakage energy is absorbed and the voltage spikes across the switch S_1 are eliminated, which is an advantage from an electromagnetic compatibility (EMC) viewpoint. The current difference between i_{Lm} and i_{lk} is transferred to the secondary side of the transformer. When i_{lk} becomes equal to $i_{Lm}(t_2)$, the diode D_3 turns off under the ZCS condition and this interval ends.

$$i_{D4}(t) = i_{lk}(t_2) - \frac{V_{C2}}{L_{lk}}.(t - t_2) \tag{9}$$

$$i_{D3}(t) = \frac{N_P}{N_S}.i_{D4}(t) \tag{10}$$

$$i_{L1}(t) = i_{L1}(t_2) - \frac{V_o}{L_1}.(t - t_2) \tag{11}$$

$$i_{D1}(t) = i_{L1}(t) - i_{D3}(t). \tag{12}$$

Interval 4 [t_3-t_4]: During this interval, V_{C2} is reversely applied to L_{lk}+L_m. Therefore, the current of D_4 is smoothly decreased. The diodes D_1 and D_2 are conducting. As a result, L_1 and L_2 are discharged. In this interval, both of the switches are turned off and D_3 is reverse biased. The important equations of this interval are as follows:

$$i_{L1}(t) = i_{L1}(t_3) - \frac{V_o}{L_1}.(t - t_3) \tag{13}$$

$$i_{D4} = i_{Lm}(t_3) - \frac{V_{C2}}{L_{lk} + L_m}.(t - t_3). \tag{14}$$

Interval 5 [t_4-t_5]: At t_4 the switch S_2 is turned on. Therefore, the diode D_2 turns off. The voltages -V_o and V_{C2}-V_o are applied to the inductors L_1 and L_2, respectively. Therefore, the inductor L_1 is discharged and the inductor L_2 is charged. During this interval, i_{D4} is still decreased. When i_{D4} reaches zero, D_4 turns off under the ZCS condition and this interval ends.

$$i_{L1}(t) = i_{L1}(t_4) - \frac{V_o}{L_1}.(t - t_4) \tag{15}$$

$$i_{D4}(t) = i_{Lm}(t_4) - \frac{V_{C2}}{L_m + L_{lk}}.(t - t_4) \tag{16}$$

$$i_{L2}(t) = i_{L2}(t_4) + \frac{V_{C2} - V_o}{L_2}.(t - t_4). \tag{17}$$

Interval 6 [t_5-t_6]: In this interval, the switch S_2 and the diode D_1 are turned on and all of the other semiconductor devices are off. In addition, L_1 is discharged and L_2 is charged. This interval continues until S_2 turns off at t_6.

Interval 7 [t_6-t_7]: At t_6, S_2 is turned off. Therefore, D_2 starts conducting. In this interval, the inductors L_1 and L_2 are discharged. This interval continues until the switch S_1 turns on again. At t_7, one switching cycle is completed and the operation is repeated.

$$i_{L2}(t) = i_{L2}(t_6) - \frac{V_o}{L_2}.(t - t_6) \tag{18}$$

$$i_{L1}(t) = i_{L1}(t_6) - \frac{V_o}{L_1}.(t - t_6). \tag{19}$$

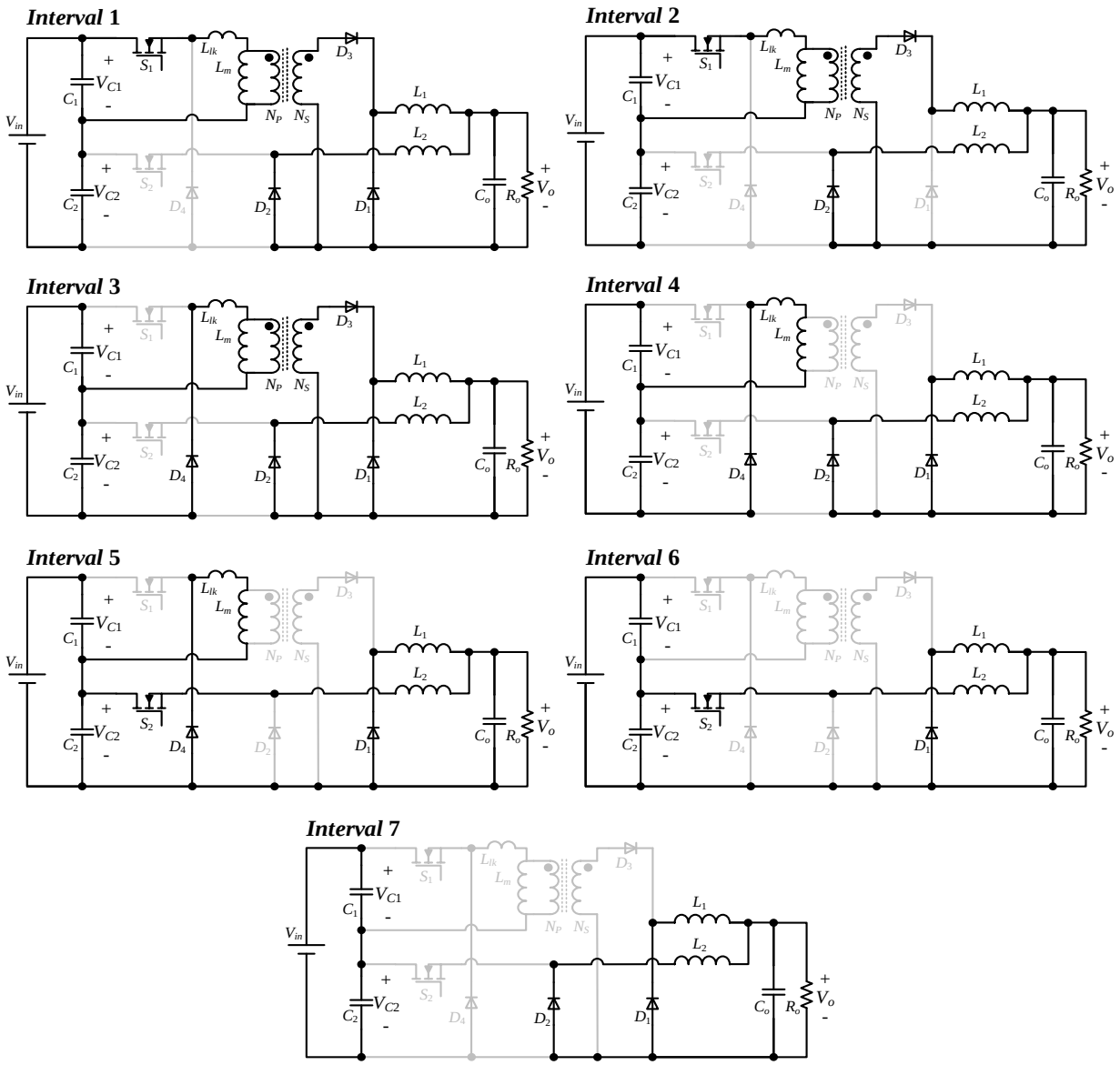


Fig. 4. Equivalent circuit for each of the operating intervals.

III. Converter Analysis and Design Considerations

A. DC Conversion Ratio

The voltages of V_{C1} and V_{C2} can be obtained from the volt-second-balance of L_1 and L_2, respectively.

$$V_{C1} = \frac{n.V_o}{D} \tag{20}$$

$$V_{C2} = \frac{V_o}{D'}. \tag{21}$$

where n is the turn ratio N_P/N_S, D is the duty cycle of S_1, and D' is the duty cycle of S_2. Since V_{in} is equal to $V_{C1}+V_{C2}$, the DC conversion ratio of the converter is obtained as follows:

$$V_{in} = V_{C1} + V_{C2} = (\frac{n}{D} + \frac{1}{D'}).V_o \tag{22}$$

$$G = \frac{V_o}{V_{in}} = \frac{D.D'}{n.D' + D}. \tag{23}$$

If $D' = D$, then

$$G = \frac{V_o}{V_{in}} = \frac{D}{n+1}. \tag{24}$$

Fig. 5 shows a comparison between the voltage conversion ratio versus the duty cycle of the proposed converter under n =1, both the conventional buck converter and the conventional forward converter under n=1, and the buck converter with a tapped inductor (turn ratio, n=1), which presents the benefit of the proposed converter for achieving a high step-down conversion ratio. Although the cost and size of the buck converter with a tapped inductor in [19] are lower, the proposed converter has a better conversion ratio. To make sure that L_m is reset in the proposed converter:

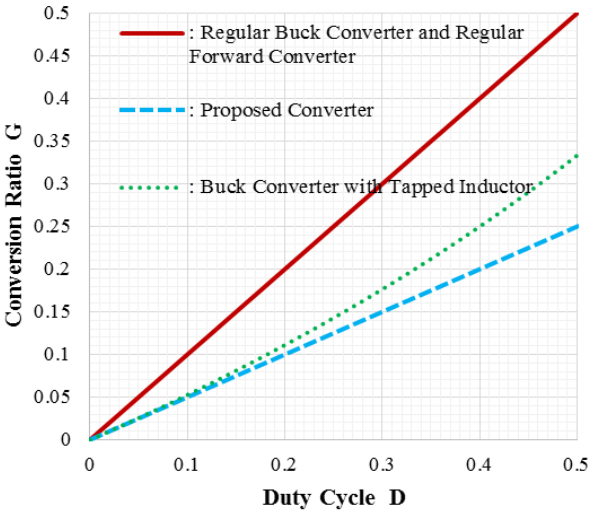


Fig. 5. Voltage conversion ratio versus the duty cycle of the proposed converter with n=1 for a regular buck converter, a regular forward converter (n=1) and the buck converter with a tapped inductor (n = 1).

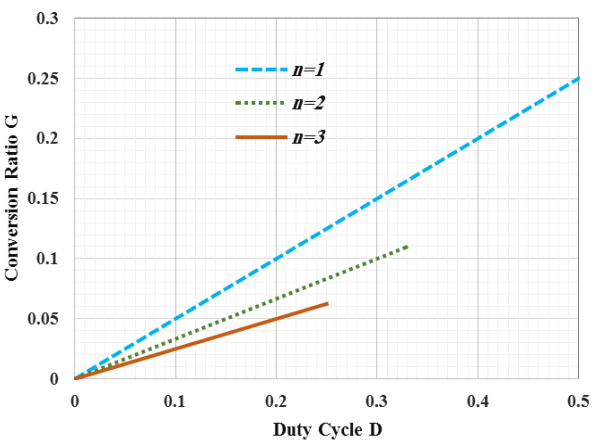


Fig. 6. Voltage conversion ratio versus the duty cycle of the proposed converter under different turn ratios.

$$\overline{D} < \frac{1}{n+1} \tag{25}$$

According to (25), $\overline{D}$ is limited to 0.5 like the conventional forward converter for n=1. Fig. 6 shows the voltage conversion ratio versus the duty cycle of the proposed converter under different turn ratios. In Table I, the proposed converter is compared to the conventional interleaved buck converter and the converters proposed in [13] and [14].

B. Semiconductor Stress Analysis

When S_1 turns off, its voltage stress is equal to V_{in}. Since, the switch S_1 turns on at a voltage that is equal to V_{C1}, the switch capacitive turn-on loss (which is proportional to the square value of the switch voltage at the turn-on time) decreases too much. When S_1 turns on, the D_4 voltage stress is equal to V_{in}. In addition, when S_2 is off, its voltage stress is equal to V_{C2} and the voltage stress of D_2 is equal to V_{C2}. A voltage stress analysis is shown in Table I, and the current stresses are summarized in Table II.

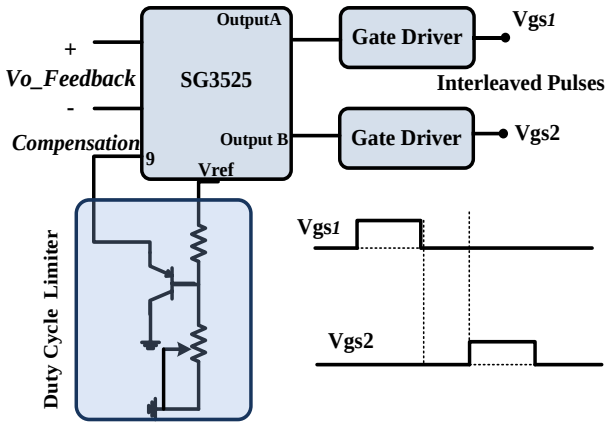


Fig. 7. PWM control scheme of the proposed converter.

TABLE I
COMPARISON BETWEEN THE PROPOSED CONVERTER AND THREE OTHER CONVERTERS

Items	Interleaved Buck	Converter in [13]	Converter in [14]	Proposed Converter
Conversion ratio	D	$\frac{D}{2-D}$	$\frac{D}{2}$	$\frac{D}{1+n}$
Voltage stress of switches	V_{in} , V_{in}	$\frac{V_{in}}{2-D}$, $\frac{V_{in}}{2-D}$	V_{in} , $\frac{V_{in}}{2}$	V_{in} , $\frac{V_{in}}{1+n}$
Voltage stress of diodes	V_{in} , V_{in}	$\frac{V_{in}}{2-D}$, $\frac{V_{in}}{2-D}$	$\frac{V_{in}}{2}$, $\frac{V_{in}}{2}$	$\frac{V_{in}}{1+n}$, $\frac{V_{in}}{1+n}$, $\frac{V_{in}}{n.(1+n)}$, V_{in}

TABLE II
SEMICONDUCTOR CURRENT STRESS ANALYSIS

Items	Formula
RMS current stress of S_1	$\frac{I_o}{2.n}.\sqrt{D}$
RMS current stress of S_2	$\frac{I_o}{2}.\sqrt{D'}$
Average current stress of D_1	$\frac{I_o}{2}.(1-D)$
Average current stress of D_2	$\frac{I_o}{2}.(1-D')$
Average current stress of D_3	$\frac{I_o}{2}.D$
Average current stress of D_4	$\frac{n^2.D'^2.D.V_{in}}{2.L_m.f_{sw}.(n.D'+D)}$

In order to implement the control circuit of the proposed converter, a SG3525 PWM controller IC is used and it has the capability of generating two pulses with a proper delay as shown in Fig. 7. Therefore, two interleaved pulses are produced. The duty cycle limiter limits the maximum duty cycle according to the value determined by (25) for a given n by adjusting the resistor. Since the maximum duty cycle ratio of the SG3525 is 50%, the limiter section is removed for n=1.

TABLE III
PARAMETERS OF THE IMPLEMENTED PROTOTYPE

Parameter	Value
Switching frequency	100 kHz
Switch S_1	IRF640
Switch S_2	IRF540
Diodes D_1, D_2 and D_3	BYV32-150
Diode D_4	BYV27-200
n,	1
L_m , L_{lk}	500μH, 10μH
Inductors L_1 and L_2	300μH
Capacitors C_1 and C_2	4.7μF / 100V
Capacitor C_o	22μF / 50V

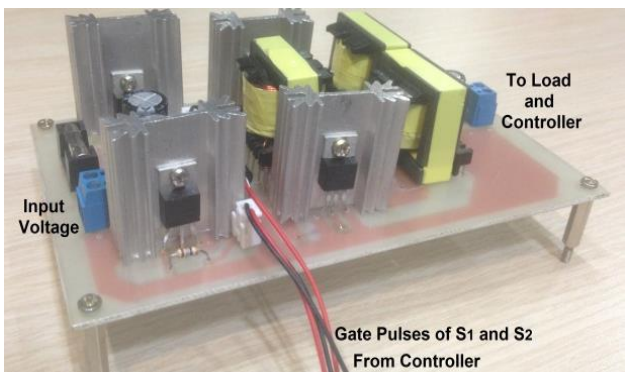
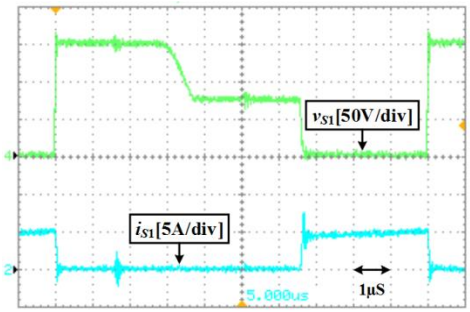


Fig. 8. Photo of the power section of the prototype.

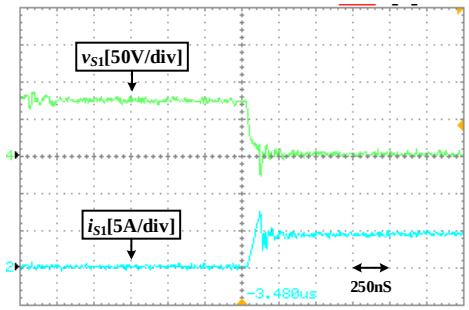
IV. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, a 150 V to 24 V/10A prototype of the proposed converter is implemented as shown in Fig. 8. The specification and components of the proposed converter are illustrated in Table III. The values of the magnetizing inductance, output inductor and output capacitor of the forward and buck converter sections are designed like regular forward and buck converters, where the inductors L_1 and L_2 are calculated to operate in the continuous current mode at 240-W of output power. The capacitors C_1 and C_2 are 4.7 μF to have a negligible voltage variation.

Fig. 9 shows voltage and current waveforms of the switch S_1 and the diodes D_1, D_3 and D_4. As can be observed from Fig. 9(a), the voltage stress of the switch S_1 is equal to V_{in}. Before S_1 turns-on, the voltage across S_1 is equal to V_{C1}, which is much lower than V_{in}. Hence, the switch capacitive turn-on losses decrease too much. There are no considerable high voltage spikes across S_1 which is beneficial to the EMC [20]. On the other hand, with a regular high step-down buck converter with a tapped-inductor, the leakage inductance causes huge voltage spike [8]. Moreover, S_1 turns on under the ZCS condition as shown in Fig. 9(b).



(a)



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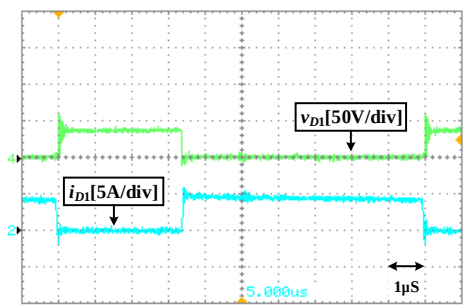
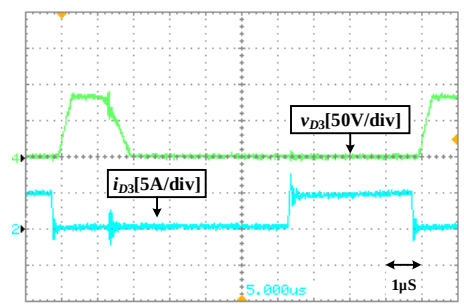
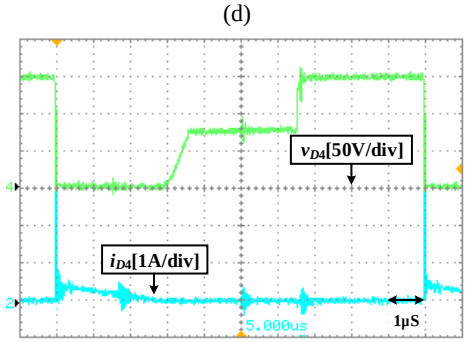


(c)

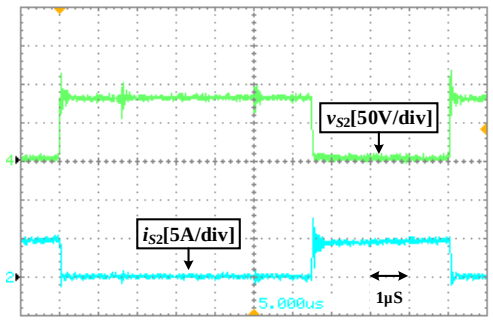


(d)

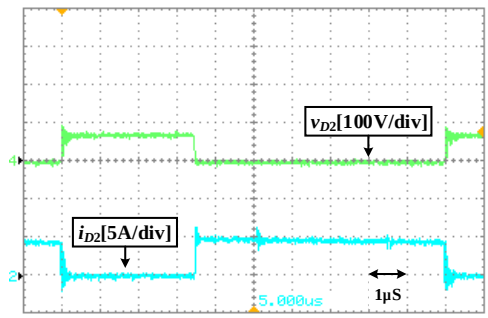


(e)

Fig. 9. Voltage and current waveforms of: (a) S_1 (time scale 1μS/div), (b) S_1 (time scale 250nS/div), (c) D_1, (d) D_3, (e) D_4.



(a)



(b)

Fig. 10. Voltage and current waveforms of: (a) S_2, (b) D_2.

According to Fig. 9 (c), (d) and (e), the voltage stresses of the diodes D_1 and D_3 are less than the diodes voltage stress in a conventional interleaved buck converter. Moreover, the voltage stress of the diode D_4 is equal to the input voltage. Fig. 10 shows voltage and current waveforms of the switch S_2 and the diode D_2. From this figure, it can be seen that the voltage stress of S_2 and D_2 is about 80 V, which is less than the voltage stress of the switches in conventional interleaved buck and conventional interleaved forward converters. Table IV shows a loss analysis of the proposed converter.

Fig. 11 shows a comparison between the efficiencies of the proposed converter and a conventional interleaved buck converter. For the conventional interleaved buck converter, IRF640 and MUR840 are used as switches and diodes, respectively. In addition, the value of the inductors is selected as 300µH. According to Fig. 11, the proposed converter provides a higher efficiency, and its efficiency at full load is around 92.7%. Since the buck section of the proposed circuit has a lower input voltage with respect to the regular interleaved buck converter, a MOSFET with a lower voltage stress and a lower $R_{ds}(on)$ is employed for the buck section. Consequently, the conduction loss of the proposed converter is reduced in comparison to the conventional interleaved buck converter. It should be mentioned that to achieve a higher step-down conversion ratio, the turn ratio n is increased in the proposed converter. In this condition with a similar output power, the output voltage is decreased and the current of the components is increased which can result in more conduction losses according to the formulas in Table IV, and the efficiency may be reduced. The dynamic response of the proposed converter

TABLE IV
IMPORTANT LOSSES IN THE PROPOSED CONVERTER

Type of loss	Element	Value (W)
Switches conduction losses (W) $R_{ds}.f_{sw}.\int_T I_s^2 dt$	S_1	4.5
	S_2	1.1
Switching losses (W)	S_1	2
	S_2	2.1
Diodes conduction losses (W) , $I_{ave}.V_F$	D_1	2
	D_2	2.3
	D_3	1.2
	D_4	0.4
Other Losses (Gate driver, Core losses, …)	-	2

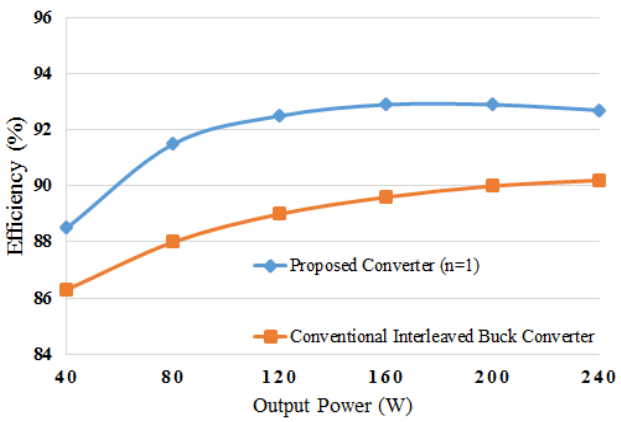


Fig. 11. Efficiency comparison between the proposed converter and a conventional interleaved buck converter.

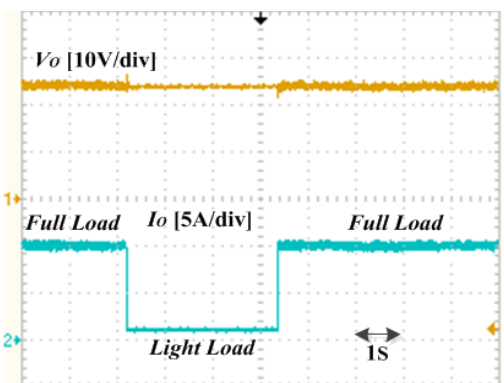


Fig. 12. Dynamic response of the proposed converter (n=1).

with the PWM controller of Fig. 7 is illustrated in Fig. 12 when the load is changed from a full load to a light load and vice versa. This confirms the proper operation of the PWM controller.

V. CONCLUSION

In this paper, an interleaved converter has been proposed that has the advantages of low switch voltage stress, low output current ripple, low switching losses, and an improved step-

down conversion ratio, which makes it a good candidate for high input voltage, low output current ripple and non-isolated step-down converters. All of these benefits are obtained without any additional stress on the components. Experimental results based on a 200 V/ 24 V–10A prototype verify the theoretical analysis. According to the efficiency curves, the proposed converter has a better efficiency in comparison to the regular interleaved buck converter.

REFERENCES

[1] M. Bendali, C. Larouci, T. Azib, C. Marchand, and G. Coquery, "Design methodology of an interleaved buck converter for onboard automotive application, multi-objective optimisation under multi-physic constraints," *IET Electr. Syst. Transp*., Vol. 5, No. 2, pp. 53-60, Nov. 2015.

[2] Y. Zhang, X.T. Sun, Y. F. Wang, and H. J. Shao, "Transformerless three-level DC-DC buck converter with a high step-down conversion ratio," *J. Power Electron.*, Vol. 13, No. 1, pp. 70-76, Jan. 2013.

[3] M. Pahlevaninezhad, J. Drobnik, P. K. Jain, and A. Bakhshai, "A load adaptive control approach for a zero-voltage-switching DC/DC converter used for electric vehicles," *IEEE Trans. Ind. Electron*., Vol. 59, No. 2, pp. 920-933, Feb. 2012.

[4] S. Kai, Z. Li, X. Yan, and J. M. Guerrero, "A distributed control strategy based on DC bus signaling for modular photovoltaic generation systems with battery energy storage," *IEEE Trans. Power Electron*., Vol. 26, No. 10, pp. 3032-3045, Oct. 2011.

[5] M. Esteki, E. Adib, H. Farzanehfard and S. A. Arshadi, "Auxiliary circuit for zero-voltage-transition interleaved pulse-width modulation buck converter," *IET Power Electron*., Vol. 9, No. 3, pp. 568-575, Mar. 2016.

[6] F. Marvi, E. Adib and H. Farzanehfard, "Efficient ZVS synchronous buck converter with extended duty cycle and low-current ripple," *IEEE Trans. Ind. Electron*., Vol. 63, No. 9, pp. 5403-5409, Sep. 2016.

[7] Q. Luo, B. Zhu, W. Lu, and L. Zhou, "High step-down multiple-output LED driver with the current auto-balance characteristic," *J. Power Electron.*, Vol. 12, No. 4, pp. 519-527, Jul. 2012.

[8] K. Yao, Y. Mao, M. Xu, and F. C. Lee, "Tapped-inductor buck converter for high-step-down DC-DC conversion," *IEEE Trans. Power Electron*., Vol. 20, No. 4, pp. 775-780, Jul. 2005.

[9] K. Yao, Y. Qiu, M. Xu, and F. C. Lee, "A novel winding-coupled buck converter for high-frequency, high-step-down DC-DC conversion," *IEEE Trans. Power Electron*., Vol. 20, No. 5, pp. 1017-1024, Sep. 2005.

[10] P. Xu, J. Wei, and F. C. Lee, "Multiphase coupled-buck converter-a novel high efficient 12 V voltage regulator module," *IEEE Trans. Power Electron*., Vol. 18, No. 1, pp. 74-82, Jan. 2003.

[11] R. J. Wai and J. J. Liaw, "High-efficiency coupled-inductor-based step-down converter," *IEEE Trans. Power Electron*., Vol. 31, No. 6, pp. 4265-4279, Jun. 2016.

[12] X. Song, C. W. Siu, C. T. Siew, and C. K. Tse, "A family of exponential step-down switched-capacitor converters and their applications in two stage converters," *IEEE Trans. Power Electron*., Vol. 29, No. 4, pp. 1870-1880, Apr. 2014.

[13] M. Esteki, B. Poorali, E. Adib, and H. Farzanehfard, "Interleaved buck converter with continuous input current, extremely low output current ripple, low switching losses, and improved step-down conversion ratio," *IEEE Trans. Ind. Electron*., Vol. 62, No. 8, pp. 4769-4776, Aug. 2015.

[14] I.-O. Lee, S.-Y. Cho, and G.-W. Moon, "Interleaved buck converter having low switching losses and improved step-down conversion ratio," *IEEE Trans. Power Electron*., Vol. 27, No. 8, pp. 3664–3675, Aug. 2012.

[15] K. I. Hwu, W. Z. Jiang and P. Y. Wu, "An expandable four-phase interleaved high step-down converter with low switch voltage stress and automatic uniform current sharing," *IEEE Trans. Ind. Electron*., Vol. 63, No. 10, pp. 6064-6072, Oct. 2016.

[16] C. F. Chuang, C. T. Pan, and H. C. Cheng, "A novel transformer-less interleaved four-phase step-down DC converter with low switch voltage stress and automatic uniform current sharing characteristics," *IEEE Trans. Power Electron*., Vol. 31, No. 1, Jan. 2015.

[17] C. T. Pan, C. F. Chuang, and C. C. Chu, "A novel transformerless interleaved high step-down conversion ratio DC-DC converter with low switch voltage stress," *IEEE Trans. Ind. Electron*., Vol. 61, No. 10, pp. 5290-5299, Oct. 2014.

[18] M. Esteki, B. Poorali, E. Adib, and H. Farzanehfard, "High step-down interleaved buck converter with low voltage stress," *IET Power Electron*., Vol. 8, No. 12, pp. 2352-2360, Dec. 2015.

[19] J. H. Park and B. H. Cho, "Nonisolation soft-switching buck converter with tapped-inductor for wide-input extreme step-down applications," *IEEE Trans. Circuits Syst. I: Reg. Papers*, Vol. 54, No. 8, pp. 1809-1818, Aug. 2007.

[20] M. R. Yazdani, H. Farzanehfard, and J. Faiz, "Classification and comparison of EMI mitigation techniques in switching power converters – A review," *J. Power Electron.*, Vol. 11, No. 5, pp. 767-777, Sep. 2011.

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