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A Single-phase Buck-boost AC-AC Converter with Three Legs

Min Zhou*, Yao Sun*, Mei Su*, Xing Li, Fulin Liu* and Yonglu Liu†**

Abstract – This paper proposes a single-phase buck-boost AC-AC converter. It consists of three legs with six switching units (each unit is composed of an active switch and a diode) and its input and output ports share a common ground. It can provide buck-boost voltage operation and immune from shoot-through problem. Since only two switching units are involved in the current paths, the conduction losses are low, which improves the system efficiency. The operation principle of the proposed circuit is firstly presented, and then, various operation conditions are introduced to achieve different output voltages with step-changed frequencies. Additionally, the parameters design and comparative analysis of the power losses are also given. Finally, experimental results verify the correctness of the proposed converter.

Keywords: Buck-boost operation, High efficiency, Single-phase AC-AC converter, Step-changed frequency

1. Introduction

Single-phase AC-AC converters are widely used in AC power supplies, induction motor driving and dynamic voltage restorers (DVRs) [1]. The basic AC-AC converters derivated from buck [2-3], boost [2, 4], and buck-boost topologies [2, 5-7], have the benefits of simple circuit configuration, ease of control, small size, low cost and high efficiency. However, they can only provide a unipolar output voltage and fail to regulate the output voltage frequency.

Matrix converters (MCs) [8-20] can output variable voltages and frequencies with the advantages of compact structure and high reliability. However, they have not been widely used because of limited voltage gain (the voltage transfer ratio is either less than one [11-13] or more than one [14]), complicated modulation strategies [15-16], complex commutation and a large number of switches. Addressing the limited voltage gain, an over-modulation technique is employed in [16] and a Z-source MC is proposed in [19]. And the commutation problem is also solved by switching cell structure with split wound coupled inductor [20], or soft commutation strategies [21]. However, those solutions mentioned above will increase the volume, costs, the control complexity or power losses.

Alternatively, AC-DC-AC converters, which perform frequency conversion with a dc bus [22-29], are widely used in industry due to the simplicity and relatively low cost. And various circuit topologies have been proposed for different applications [26, 30-35]. Generally, a diode rectifier is used as the front stage to reduce the control complexity and the cost [22, 33-35]. However, the input currents are uncontrollable, which are undesired for many applications. To achieve the sinusoidal current as well as low cost, a three-leg converter is proposed in [23] by sharing a leg between the rectifier and inverter. It has the highlights of smaller number of switches and lower power losses. However, the three-leg configuration may be only suitable for the situations that the grid and load frequencies are identical (e.g., UPSs) [23-28]. Moreover, all of them are with bulky intermediate capacitors, which increase the volume and reduce the reliability [29]. A current source type AC-AC converter with six switches is proposed in [30], as shown in Fig. 1. It can provide buck-boost voltage operation with step-changed frequencies, and only a small inductor has been used. What's more, it has no short-circuit problem. However, the high conduction power losses is significant because there are always three switching units (each unit is composed of an active switch and a diode) contained in the current paths.

To overcome the drawback of the converter in [30], a

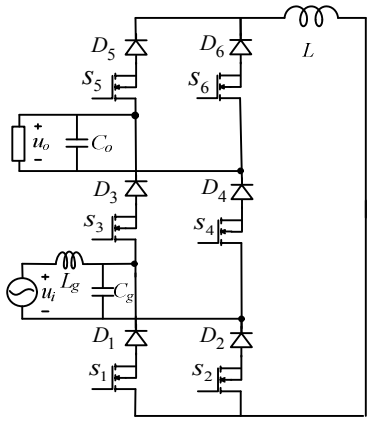

Fig. 1. Single-phase buck-boost AC-AC converter proposed in [30]

† Corresponding Author: Dept. of Electrical Engineering, Central South University, China. (liuyonglu@csu.edu.cn)
* Dept. of Electrical Engineering, Central South University, China
** Dept. of Electrical and Electronic Engineering, Hunan University, China.
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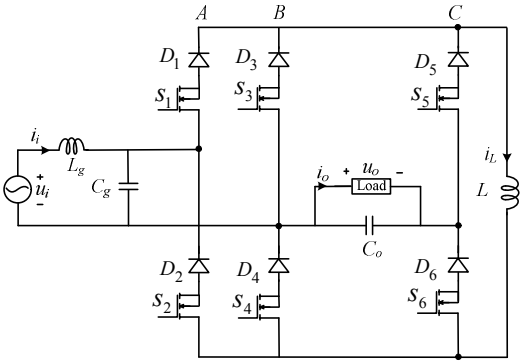


Fig. 2 Proposed single-phase buck-boost AC-AC converter

single-phase buck-boost AC-AC converter with common ground between the input and output ports is proposed, as shown in Fig. 2. It consists of three legs, an intermediate inductor, an input filter, and an output filter. Apparently, the proposed converter employs the same number of components as the existing circuit shown in Fig. 1. It also possesses all the functions that the converter shown in Fig. 1 has. The highlight of the proposed converter is that only two switching units are involved in the current conducting loops. Therefore, lower conduction losses are achieved, which improves the conversion efficiency.

The rest of the paper is arranged as follows: Section 2 introduces the circuit configuration of the proposed converter; Section 3 presents the operation principle with various switching strategies; Section 4 gives a comparative analysis of the power losses between the converters in this paper and [30]. Experimental results are provided in Section 5. Finally, Section 6 gives the conclusion.

2. Circuit Configuration

Fig. 2 shows the circuit configuration of the proposed single-phase AC-AC converter. It consists of three legs (A, B, C), an intermediate inductor L, input filters (L_g, C_g), and an output filter C_o. legs A and B constitute the rectifier and legs B and C form the inverter. Consequently, leg B is shared. Each leg is composed of two switching units. And the switching unit can be realized by a RB-IGBT or the series combination of a MOSFET and a fast recovery diode. The latter will be adapted in this paper for the purpose of high efficiency.

3. Operating Condition

This section is to introduce the circuit operation conditions. The intermediate inductor current is controlled to be rectified sinusoidal shape in this study. Assumes that the grid voltage is pure sinusoidal, all the active and passive components are ideal, and the switching voltage ripples are negligible in each switching period.

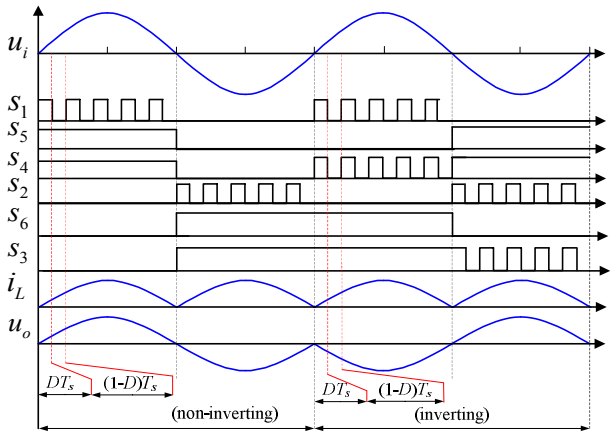


Fig. 3. Switching sequences and key waveforms for non-inverting and inverting buck-boost operations

3.1 Case I: 50 Hz (same frequency, f_o=f_{in}) operation

In this operation case, the input frequency f_{in} and the output frequency f_o are the same. There exist two specific operation modes: non-inverting buck-boost operation mode and inverting buck-boost operation mode. The related switching strategies and key waveforms are shown in Fig. 3, where T_s is the switching period. The detailed analysis is as follows.

1) For non-inverting buck-boost operation mode: During the positive half line cycle (u_i>0), only switch S_1 is driven by the PWM signal with a duty ratio D, switches S_2, S_3, and S_6 are kept being off, and switches S_4 and S_5 are kept being on.

During DT_s interval, the switch S_1 is turned-on. The switching state and current path are shown in Fig. 4(a). Although S_5 is also turned on, it won't conduct as a reverse-biased voltage (u_i+u_o) is imposed on D_5. The energy is transferred from the grid to the intermediate inductor and the dynamic differential equation of inductor L is

$$L\frac{di_L}{dt} = u_i \tag{1}$$

During (1-D) T_s interval, the switch S_1 is turned-off. The switching state and the current path are shown in Fig. 4(b). Note that no overlap time (avoiding the open-circuit of the intermediate inductor current) is needed as S_5 is always turned on. The energy stored in the intermediate inductor L is released to the load. Applying Kirchhoff voltage laws (KVL) yields

$$L\frac{di_L}{dt} = -u_o \tag{2}$$

Based on the volt-second balance principle, (1), and (2), the voltage gain is derived as

$$\frac{u_o}{u_i}=\frac{D}{1-D} \tag{3}$$

From (3), the proposed converter can both buck and boost the input voltage.

During the negative half line cycle ($u_i<0$), only switch S_2 is driven by the PWM signal with a duty ratio D, switches S_1, S_4, and S_5 are kept being off, and switches S_3 and S_6 are kept being on. States 3 and 4, as shown in Figs. (c) and (d), are used and the operation principle can be similarly analyzed.

2) For inverting buck-boost operation mode: During the positive half line cycle ($u_i>0$), switches S_1 and S_4 are driven by the PWM signal with the duty ratio D, switches S_2 and S_5 are kept being off, and switches S_3 and S_6 are kept being on. During DT_s interval, switches S_1 and S_4 are turned-on. Although S_3 (S_6) is also turned-on, it won't conduct as a reverse-biased voltage u_i ($|u_o|$) is imposed on D_3 (D_6). Then the current path is shown in Fig. 4(e). During $(1\text{-}D)T_s$ interval, switches S_1 and S_4 are both turned-off, then switches S_3 and S_6 conduct the current i_L, as shown in Fig. 4(d).

During the negative half line cycle ($u_i<0$), switches S_2 and S_3 are driven by PWM signals with the same duty ratio D, switches S_1 and S_6 are kept being off, and switches S_4 and S_5 are kept being on. States 2 and 6, as shown in Figs. (b) and (f), are used and the operation principle can be similarly analyzed. It can be found that although the switching states are different, the current paths in state 5 (state 6) and state 1 (state 3) are the same.

The charging and discharging operation of the inductor L is same as the non-inverting buck-boost operation mode. Based on the volt-sec principle, the voltage gain of the proposed converter for inverting buck-boost operation mode can be described as

$$\frac{u_o}{u_i}=\frac{-D}{1-D} \tag{4}$$

From (4), the voltage gain of this mode is $-D/(1-D)$, which is same as that in the non-inverting buck-boost operation mode. The sign "-" means that the output voltage u_o is out of phase with the input voltage u_i.

3.2 Case II: 25 Hz (step-down frequency, $f_o = f_{in}/2$) operation

In this operation case, the output frequency f_o is half of the input frequency f_{in}. The related switching strategies and key waveforms are shown in Fig. 5. As seen, the system operates in non-inverting operation mode for one line cycle (0.02s) and then inverting operation mode for the next one, and so on. When operating under the non-inverting operation mode, states 1, 2, 3, and 4 are adopted. When operating under the inverting operation mode, states 2, 4, 5, and 6 are adopted. The operation principles in this case are identical to those in the Case I. The voltage gain of the step-down frequency operation is $D/(1-D)$ for non-inverting operation mode and $-D/(1-D)$ for inverting operation mode, which is also the same as that in the Case I

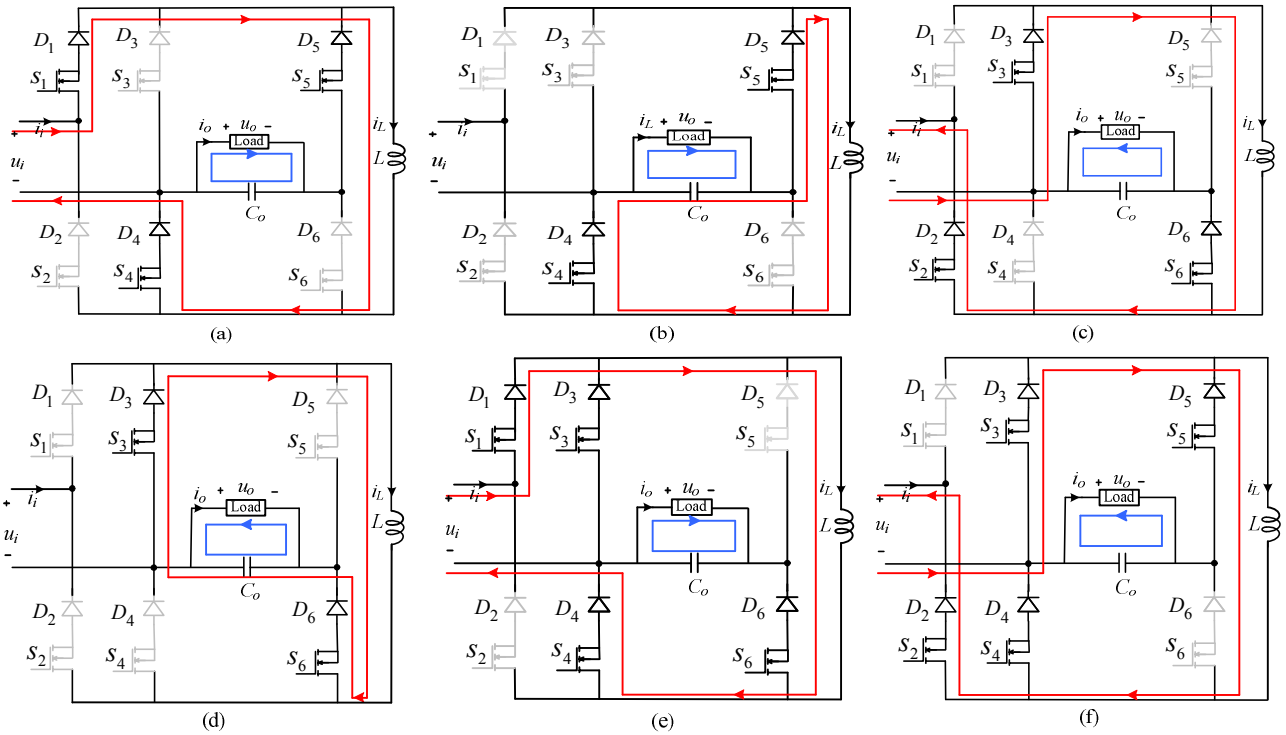


Fig. 4 Switching states and current paths: (a) State 1. (b) State 2. (c) State 3. (d) State 4. (e) State 5. (f) State

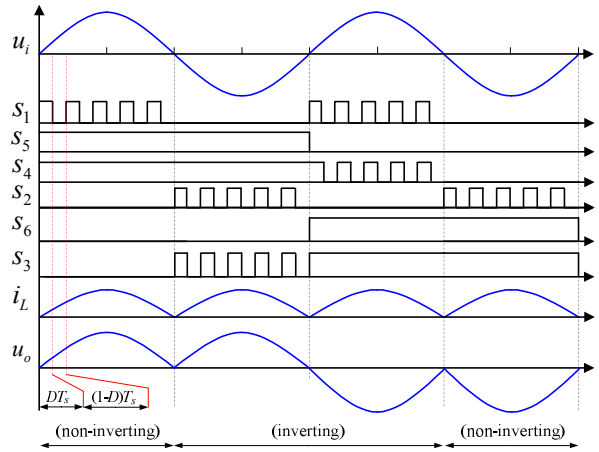


Fig. 5. Switching sequence and key waveforms for step-down frequency operation

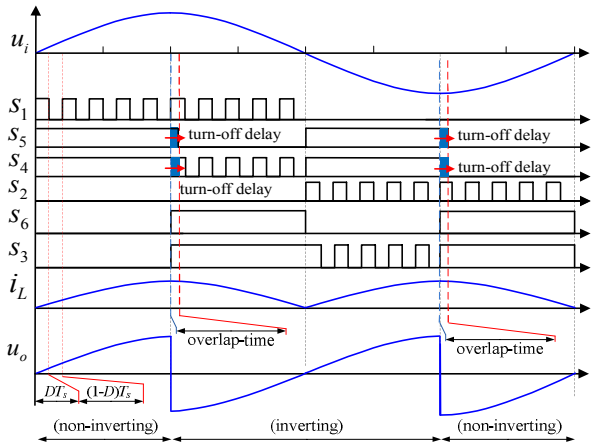


Fig. 6. Switching sequence and key waveforms for step-up frequency operation

(see (3) and (4)). For other step-down frequency operation cases, similar results can be obtained.

3.3 Case III: 100 Hz (step-up frequency, f_o=2 f_{in}) operation

In this operation case, the output frequency f_o is twice the input frequency f_{in}. The related switching strategies and key waveforms are shown in Fig. 6. As seen, the system operates under non-inverting operation mode and inverting operation mode alternately. The operation modes change at the positive or negative peak grid voltage. The operation principles in this case are also identical to those in the Case I. The voltage gain is D/(1-D) for non-inverting operation mode and -D/(1-D) for inverting operation mode.

As can be seen from Fig. 3, Fig. 5 and Fig. 6 that the non-inverting operation mode and the inverting operation mode alternate at the zero-crossing of the intermediate inductor current for Cases I and II. However, that is invalid for Case III. So, a overlap-time is added to avoid open circuit problem, as shown in Fig. 6. It can be found that the proposed converter can achieve the same functions that the one proposed in [30] possesses. However, one less switching unit is involved in its current paths. So less conduction power losses are caused, which will be introduced in the following.

4. Losses Analysis and Comparison

A detailed losses analysis of the proposed AC-AC converter is done in this section. It is used to guide the design of the heat sink and evaluate the system efficiency. A comparison with the converter proposed in [30] is also given. Since the power losses of passive components are negligible compared with those of the semiconductors. The losses analysis will mainly focus on conduction losses and switching losses of semiconductor devices. Take the Case III as an example, the power losses of the converter is analyzed. Power losses in other operation cases can be similarly analyzed.

4.1 Voltage stresses

The peak voltage stresses of the switches S_1-S_6 and the blocking voltage of D_1-D_6 are given below,

$$\begin{cases} V_{Sx,peak} = V_{Dy,peak} = U_i + U_o \\ x = 1,2 \\ y = 5,6 \end{cases} \tag{5}$$

$$\begin{cases} V_{Sx,peak} = U_o \\ x = 3,4,5,6 \end{cases} \tag{6}$$

$$\begin{cases} V_{Dy,peak} = U_i \\ y = 1,2,3,4 \end{cases} \tag{7}$$

where $V_{Sx,peak}$ (x=1, 2, 3, 4, 5, 6) is the voltage stress of switch S_x, $V_{Dy,peak}$ (y=1, 2, 3, 4, 5, 6) is the voltage stress of diode D_y, U_i and U_o are the peak values of the input voltage and output voltage.

4.2 Current stresses

The peak current stresses of the switches S_1-S_6 are equal to the maximum value of intermediate inductor current i_L. Assume i_L is controlled to be rectified sinusoidal shape, and given as (ignoring current ripple),

$$i_L = i_L^* = I_L \left|\sin(\omega t)\right| \tag{8}$$

where $I_L = 2P_o/((1\text{-D})U_o)$.

The average current $I_{sx,avg}$ flowing through switches S_x is

$$\begin{cases} I_{Sx,avg} = \dfrac{1}{2\pi}\int_0^{\pi} DI_L \sin(\omega t)dt = \dfrac{DI_L}{\pi} \\ x = 1,2 \end{cases} \tag{9}$$

$$\begin{cases} I_{Sx,avg} = \dfrac{1}{2\pi}\int_0^{\pi} I_L \sin(\omega t)dt = \dfrac{I_L}{\pi} \\ x = 3,4 \end{cases} \tag{10}$$

$$\begin{cases} I_{Sx,avg} = \dfrac{1}{2\pi}\int_0^{\pi} (1-D) I_L \sin(\omega t)dt = \dfrac{(1-D)I_L}{\pi} \\ x = 5,6 \end{cases} \tag{11}$$

The root-mean-square (RMS) current $I_{sx,rms}$ flowing through switches S_x is as follows,

$$\begin{cases} I_{Sx,rms} = \dfrac{1}{2\pi}\sqrt{\int_0^{\pi} (DI_L \sin(\omega t))^2} = \dfrac{DI_L}{2} \\ x = 1,2 \end{cases} \tag{12}$$

$$\begin{cases} I_{Sx,rms} = \dfrac{1}{2\pi}\sqrt{\int_0^{\pi} (I_L \sin(\omega t))^2} = \dfrac{I_L}{2} \\ x = 3,4 \end{cases} \tag{13}$$

$$\begin{cases} I_{Sx,rms} = \dfrac{1}{2\pi}\sqrt{\int_0^{\pi} ((1-D)I_L \sin(\omega t))^2 dt} = \dfrac{(1-D)I_L}{2} \\ x = 5,6 \end{cases} \tag{14}$$

Since D_x is in series with switches S_x, respectively. the current stress of D_x is equal to that of switch S_x.

The voltage and current stresses of semiconductor devices in this paper and [30] are summarized in Table 1.

As can be seen from Table 1, the maximum voltage stresses of switches in this paper and in [30] are both (U_i+U_o). And the maximum RMS currents pass through switches in both two converters are (I_L/2). However, the average/RMS currents of S_1, S_2, S_5, S_6, D_1, D_2, D_5, and D_6 in this paper are smaller than those in [30]. Table 1 will be used to guide the selection of appropriate semiconductors and estimate the power losses of the system.

Table 1. Switch stresses

Switches	Voltage stress		Current stress			
	This paper	[17]	This paper		[17]	
			Average	RMS	Average	RMS
S_1, D_1	U_i+U_o, U_i	U_i, U_i	$\frac{DI_L}{\pi}$	$\frac{DI_L}{2}$	$\frac{I_L}{\pi}$	$\frac{I_L}{2}$
S_2, D_2	U_i+U_o, U_i	U_i, U_i				
S_3, D_3	U_o, U_i	U_i+U_o, U_i+U_o	$\frac{I_L}{\pi}$	$\frac{I_L}{2}$		
S_4, D_4	U_o, U_i	U_i+U_o, U_i+U_o				
S_5, D_5	U_o, U_i+U_o	U_o, U_o	$\frac{(1-D)I_L}{\pi}$	$\frac{(1-D)I_L}{2}$		
S_6, D_6	U_o, U_i+U_o	U_o, U_o				

4.3 Conduction losses

According to Fig. 4, it is clearly that the intermediate inductor current always flows through two active switches and two diodes. Therefore, the average conduction losses of the proposed converter are relatively easy to be estimated.

According to [36, 37], the conduction losses are related to the voltage drop across the device and the current flowing through it. Then, the conduction losses of a MOSFET (P_{c_m}) and a diode (P_{c_d}) can be respectively evaluated by

$$P_{c\_m} = \frac{1}{T}\int_0^T R_{m\_on} i_m^2 dt \tag{15}$$

$$P_{c\_d} = \frac{1}{T}\int_0^T (V_{F0} i_d + R_F i_d^2) dt \tag{16}$$

where T is the period of the integrated function, i_m is the flowing current of the MOSFET, R_{m_on} is the turn-on resistance, i_d is the current through the diode, and V_{F0} and R_F represent on-state zero-current voltage and on-state resistance of the diode.

Then the total conduction losses are

$$\begin{aligned} P_c &= 2(P_{c\_m} + P_{c\_d}) \\ &= 2\frac{1}{T}\int_0^T (V_{F0} i_L + (R_{m\_on} + R_F) i_L^2) dt \\ &= (R_{m\_on} + R_F) I_L^2 + \frac{4V_{F0}}{\pi} I_L \end{aligned} \tag{17}$$

On the other hand, there are three active switches and three external diodes contained in the current paths of the converter proposed in [30]. Then its total conduction losses are

$$P_{c1} = 3(P_{c\_m} + P_{c\_d}) = \frac{3}{2}(R_{m\_on} + R_F) I_L^2 + \frac{6V_{F0}}{\pi} I_L \tag{18}$$

From (17) and (18), it can be seen that the conduction losses of the proposed converter are 1/2 times lower than those in [30].

4.4 Switching losses

In the proposed AC-AC converter, only an active switch S_1 (S_2) and two diodes D_1 and D_5 (D_2 and D_6) work at high frequency during the positive half cycle (negative half cycle) under non-inverting buck-boost operation mode. Two active switches S_1 and S_4 (S_2 and S_3) and four diodes D_1, D_3, D_4, and D_6 (D_2, D_3, D_4 and D_5) operate at high frequency during the positive half cycle (negative half cycle) under inverting buck-boost operation mode. Note that in the positive half cycle (negative half cycle) there are no reverse recovery losses happened to D_1 (D_2) under non-

inverting buck-boost operation mode due to a negative reverse voltage. Similar conditions happen to D_1 and D_4 (D_2 and D_3) under inverting buck-boost operation mode. Therefore, only one active switch S_1 (S_2) and one diode D_5 (D_6) produce switching losses during the positive half cycle (negative half cycle) under non-inverting buck-boost operation mode. And two active switches S_1 and S_4 (S_2 and S_3) and diodes D_3 and D_6 (D_4 and D_5) cause switching losses during the positive half cycle (negative half cycle) under inverting buck-boost operation mode.

The lossing energy is assumed proportional to the conducting current and the blocking voltage at the moment of a switching event [37]. For a MOSFET, its switching losses can be formulated as

$$P_{s\_m} = \frac{f_s}{T}\int_0^T (\tfrac{1}{2} i_m v_m (t_{off} + t_{on}) + \tfrac{1}{2} C_{oss} v_m^2) dt \tag{19}$$

where f_s is the switching frequency, C_{oss} is the output capacitor of the MOSFET, t_{on} and t_{off} are turn-on and turn-off times

For diodes, the switching losses is typically caused by the reverse recovery mechanism, which only occurs during turn-off, and can be expressed as [37],

$$P_{s\_d} = \frac{f_s}{T}\int_0^T Q_{rr} u_f dt \tag{20}$$

where Q_{rr} and u_f are the reverse recovery charge and the reverse voltage of the diode.

Then the switching losses of the proposed converters in this paper and [30] over one line cycle are listed as Table 2.

According to Table 2, the total switching losses of the converter can be expressed as

$$P_{total} = \sum_{i=1}^{6} (P_{s_i} + P_{D_i}) \tag{21}$$

4.5 Discussion

Considering the system parameters listed in Table 3, the adopted MOSFET and diode are IPW60R099P6 and DSEI60-06A, respectively. According to the datasheets, for the MOSFET, t_{on}=30 ns, t_{off} =55 ns, R_{m_on}=0.099 Ω, C_{oss}=140 pF; for the diode, Q_{rr}=1.5 μC, V_{F0}=1.13 V, and R_F =0.0047Ω. The losses distribution and conversion efficiencies of the converters in this paper and [30] are depicted in Fig. 7.

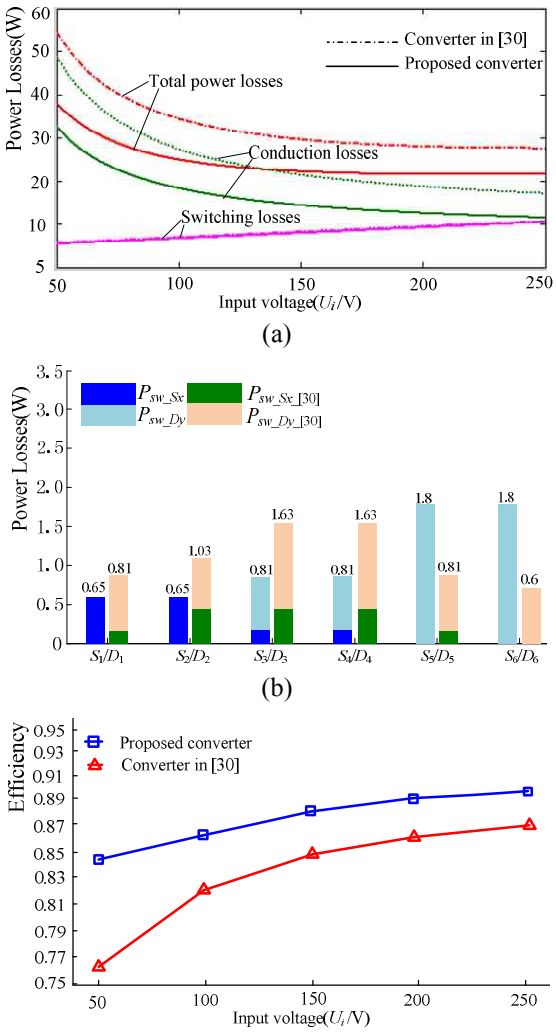


Fig. 7. Losses and efficiencies of the proposed converter and converter in [30]: (a) Power losses. (b) Switching losses distributions when U_i=100V. (c) Efficiencies versus input voltage

Table 2. Switching losses

Switch, diode	Switching losses	
	This paper	[30]
S_1, D_1	$\frac{1}{8} f_s \left[(2U_i + U_o) I_L (t_{on} + t_{off}) + \frac{1}{2} C_{oss} (2U_i^2 + 2U_i U_o + U_o^2)\right]$, 0	$\frac{1}{8} f_s \left[U_i I_L (t_{on} + t_{off}) + \frac{1}{2} C_{oss} U_i^2\right]$, $\frac{1}{2\pi} f_s Q_{rr} U_i$
S_2, D_2	$\frac{1}{8} f_s \left[(2U_i + U_o) I_L (t_{on} + t_{off}) + \frac{1}{2} C_{oss} (2U_i^2 + 2U_i U_o + U_o^2)\right]$, 0	$\frac{1}{8} f_s \left[(U_i + U_o) I_L (t_{on} + t_{off}) + \frac{1}{2} C_{oss} (U_i^2 + U_o^2)\right]$, $\frac{1}{2\pi} f_s Q_{rr} U_i$
S_3, D_3	$\frac{1}{8} f_s \left[U_o I_L (t_{on} + t_{off}) + \frac{1}{2} C_{oss} U_o^2\right]$, $\frac{1}{2\pi} f_s Q_{rr} U_i$	$\frac{1}{8} f_s \left[(U_i + U_o) I_L (t_{on} + t_{off}) + \frac{1}{2} C_{oss} (U_i + U_o)^2\right]$, $\frac{1}{2\pi} f_s Q_{rr} (U_i + U_o)$
S_4, D_4	$\frac{1}{8} f_s \left[U_o I_L (t_{on} + t_{off}) + \frac{1}{2} C_{oss} U_o^2\right]$, $\frac{1}{2\pi} f_s Q_{rr} U_i$	$\frac{1}{8} f_s \left[(U_i + U_o) I_L (t_{on} + t_{off}) + \frac{1}{2} C_{oss} (U_i + U_o)^2\right]$, $\frac{1}{2\pi} f_s Q_{rr} (U_i + U_o)$
S_5, D_5	0, $\frac{1}{2\pi} f_s Q_{rr} (U_i + 2U_o)$	$\frac{1}{8} f_s \left[U_o I_L (t_{on} + t_{off}) + \frac{1}{2} C_{oss} U_o^2\right]$, $\frac{1}{2\pi} f_s Q_{rr} U_o$
S_6, D_6	0, $\frac{1}{2\pi} f_s Q_{rr} (U_i + 2U_o)$	0, $\frac{1}{2\pi} f_s Q_{rr} U_o$

It can be seen from Fig.7(a) that the switching losses of the two converters are nearly the same. However, the losses distributions are different, as shown in Fig. 7(b), which should be paid attention when doing thermal design.

On the other hand, the conduction losses of the proposed converter are 1/2 times lower than those of the converter in [30], which can be identified easily from both Fig. 7(a) and formulas (17), (18).

Therefore, take both the switching losses and the conduction losses into consideration, the converter in this paper has a higher efficiency than the converter in [30], as shown in Fig. 7(c). But the difference becomes smaller with increasing the input voltage.

5. Experimental Results

A prototype for the proposed converter was built in lab as shown in Fig. 8 for experimental verification. The setup includes: a main circuit board, a drive board, a auxiliary power supply and a control board. The control board of the converter was realized by a combination of digital signal processor TMS320F28335 and field programmable gate array FPGA EP2C8T144C8N.

The experimental parameters are listed in Table 3. And four experimental results, as shown in Figs 9-12, were conducted.

Fig. 9 shows the experimental results with the same source and load frequencies (50 Hz) under non-inverting mode. Fig. 9(a) shows the waveforms under non-inverting buck operation mode (U_o=100V<U_i=110$\sqrt{2}$ V) and Fig. 9(b) shows the waveforms under non-inverting boost operation mode (U_o=100V>U_i=60$\sqrt{2}$ V). From top to bottom, input voltage/current and output voltage/current

Table 3. Parameters used in analysis and experiment

Parameters	Symbol	Value
Output power	P_o	200W
Amplitude of the output voltage	U_o	100V
Amplitude of input phase voltage	U_i	50~250V
Source angular frequency	ω	314rad/s
Input filters	L_g/C_g	100μH/10μF
Intermediate filter inductor	L	800μH
Output filters	C_o	10μF
Load	R	25Ω
Switching frequency	f_s	25kHz

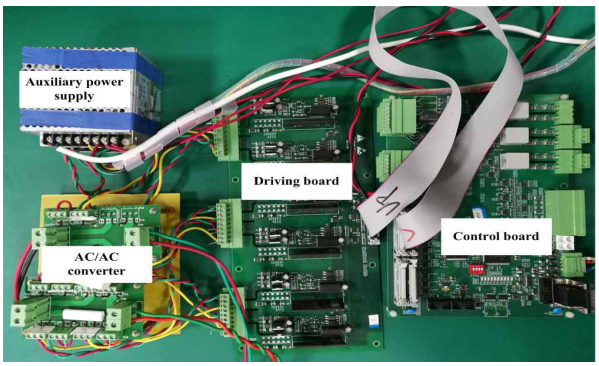
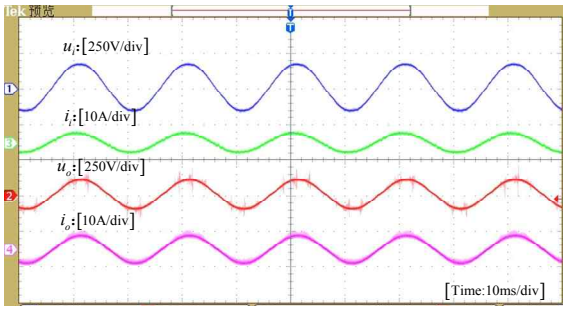
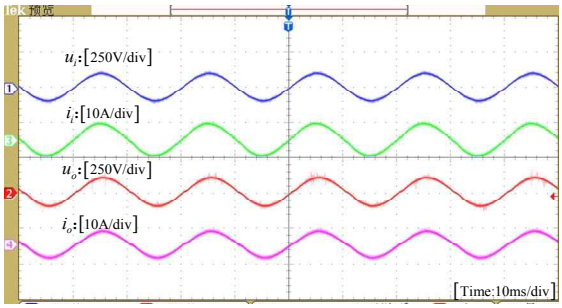


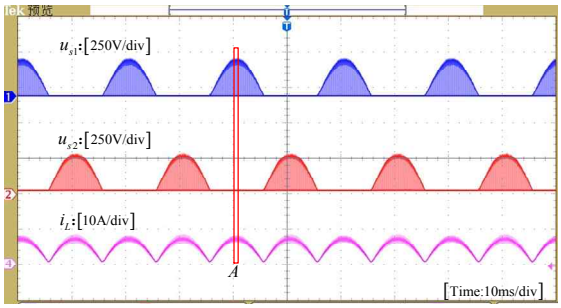
Fig. 8. Experimental setup for the converter



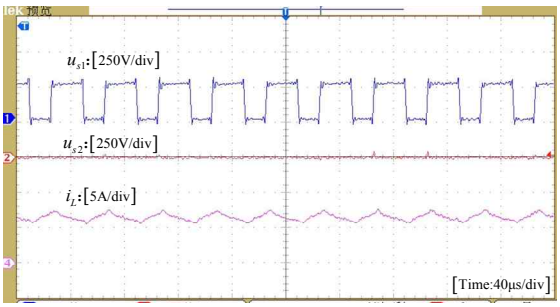
(a)



(b)



(c)



(d)

Fig. 9. Experimental waveforms under non-inverting buck-boost mode operations for U_o =100V and f_o =50 Hz. (a) Buck operation when U_i=110$\sqrt{2}$ V. (b) Boost operation when U_i=60$\sqrt{2}$ V. (c) Switches voltage and intermediate inductor current under non-inverting buck operation mode. (d) Zoom-in waveforms of point A

are illustrated. In both cases the output voltages are in phase with the input voltages. Fig. 9(c) shows the voltages between the source and drain of switches S_1 and S_2, and intermediate inductor current under non-inverting buck operation mode. And the zoom-in waveforms of point A is given in Fig. 9(d).

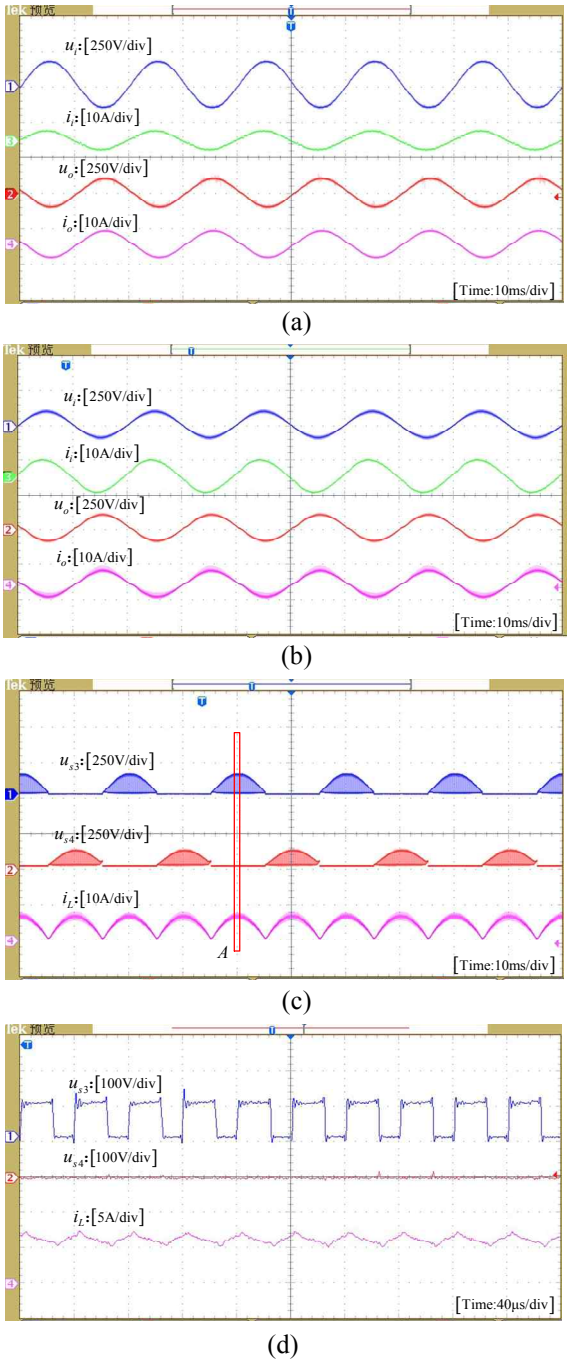


Fig. 10. Experimental waveforms under inverting buck-boost mode operations for U_o =100V and f_o =50 Hz. (a) Buck operation when U_i =110$\sqrt{2}$ V. (b) Boost operation when U_i=60$\sqrt{2}$ V. (c) Switches voltage and intermediate inductor current under inverting buck operation mode. (d) Zoom-in waveforms of point A

As seen, the intermediate inductor current is rectified sinusoidal shape as expected. In the first half line cycle, S_1 is driven by the PWM signal and S_2 is kept off. And in the next half line cycle S_2 is driven by the PWM signal and S_1 is kept off. The experimental waveforms are consistent with analysis in Fig. 3.

The experimental waveforms with the same source and load frequencies (50 Hz) under inverting mode are shown in Fig. 10. The waveforms under this mode is similarly to those under non-inverting mode, expect that the input/ output voltages are out of phase.

In this mode, as analyzed in Fig. 3, switches S_1 and S_4 operate at high frequency in one half line cycle and switches S_2 and S_3 operate at high frequency in the next half line cycle. The voltages between the source and drain of switches S_3 and S_4 are shown in Fig. 10(c) and (d).

Fig. 11 shows the experimental results with a step-down frequency (25 Hz) output voltage. The waveforms in Fig. 11(a) are input voltage/current, output voltage and intermediate current under the buck operation mode. And Fig. 11(b) shows the waveforms under the boost operation mode. As seen, in both cases the output voltages are in phase with the input voltages for one line cycle (0.02 s) and out of phase with the input voltage for the next one, and so on.

Fig. 12 shows the experimental results with a step-up frequency (100 Hz) output voltage. Fig. 12(a)/Fig. 12(b)

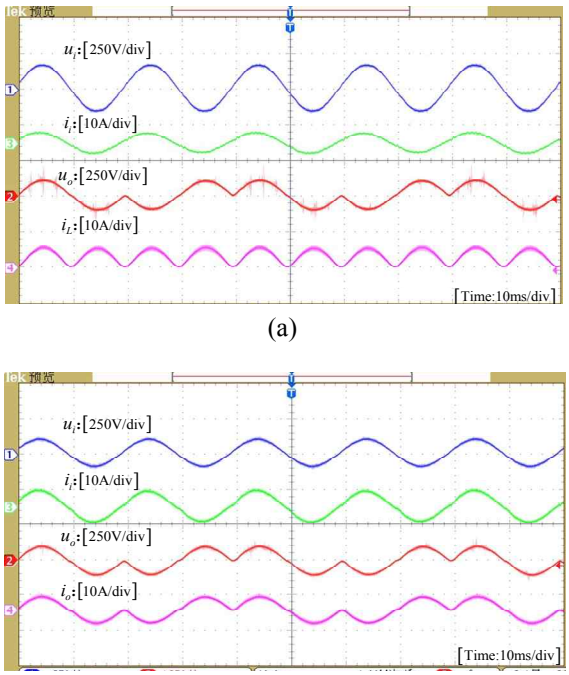


Fig. 11. Experimental waveforms under step-down frequency and buck-boost mode operations for U_o =100 V and f_o=25 Hz .(a) Buck operation when U_i =110$\sqrt{2}$ V. (b) Boost operation when U_i =60$\sqrt{2}$ V

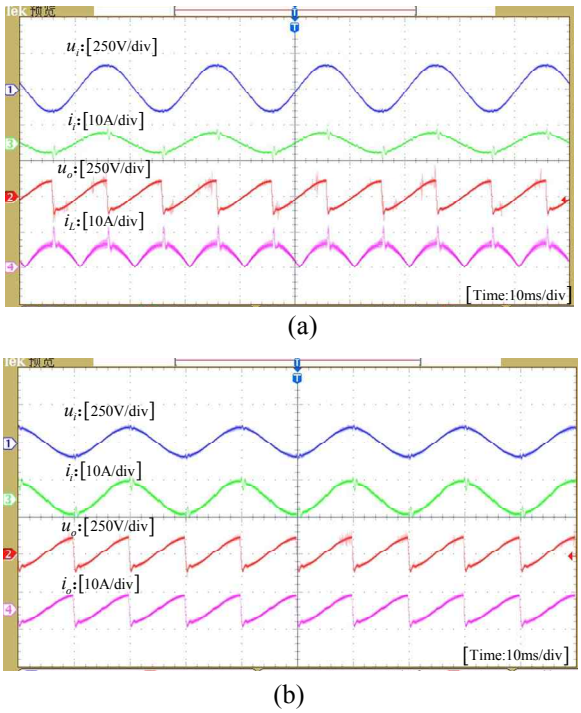


Fig. 12. Experimental waveforms converter under step-up frequency and buck-boost mode operations for U_o =100V and f_o =100 Hz: (a) Buck operation when U_i =110 $\sqrt{2}$ V. (b) Boost operation when U_i = 60 $\sqrt{2}$ V.

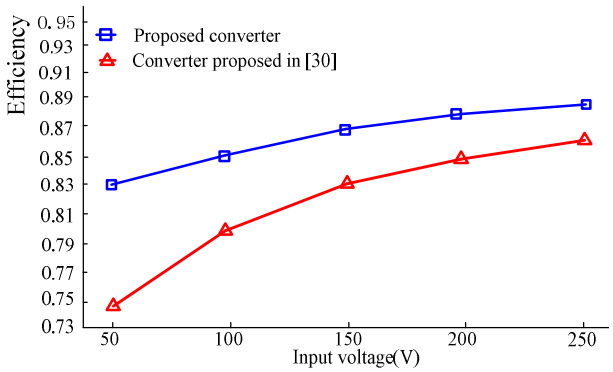


Fig. 13. Measured efficiencies versus input voltage of the proposed converter and converter in [30]

shows the waveforms under the buck operation mode/ under the boost operation mode. In order to get a step-up frequency output voltage, the converter has to change the direction of the output voltage at the peak value. Then, the output capacitor releases its energy to the inductor quickly and then absorbs the same energy back. Therefore, a spike current happened, as shown in Fig. 12(a).

Fig. 13 shows the measured efficiency curves of the converters in this paper and in [30]. It can be found that the proposed converter always has a higher efficiency compared with the converter in [30], due to its low conduction losses. The experimental efficiencies are slightly smaller than those obtained by theoretical calculation, since the power losses of the passive components are included.

6. Conclusion

A single-phase buck-boost AC-AC converter with six active switches is proposed in this paper. It can both buck and boost the input voltage, which enhances the scope of the output voltage. Besides, it is immune from shoot-through problem of voltage source, even in the case that all switches are turned on simultaneously. The highlight is the smaller power losses compared with the existing converter, which improves the system efficiency. A detailed analysis of the proposed circuit and various operation conditions was introduced. A laboratory prototype was built to verify the theoretical analysis. The proposed converter can server as DVRs to protect the sensitive loads from voltage disturbances, for instance, voltage sag and swell. And it can also be suitable for applications where both output voltage and frequency regulations are needed, such as induction heating, speed control of a fan or a pump, induction motor driving and so on.

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Min Zhou was born in Hunan, China, in 1993. He received the B.S. degree in Automation, in 2016 from Xiangtan University, Xiangtan, China. He is currently working toward the M.S. degree in electrical engineering, Central South University, Changsha, China. His research interests include matrix converter and ac/ac converters.

Yao Sun (M'13) was born in Hunan, china, in 1981. He received the B.S. degree in Automation, in 2004, M.S. and Ph.D. degrees in electric engineering, in 2007 and 2010 respectively, all from the School of Information Science and Engineering, Central South University. He has been an associate professor with the School of Information Science and Engineering, Central South University, China. His research interests include matrix converter, micro-grid and wind energy conversion system.

Mei Su was born in Hunan, China, in 1967. She received the B.S. degree in Automation, in 1989, M.S. and Ph.D. degrees in electric engineering, in 1992 and 2005 respectively, all from the School of Information Science and Engineering, Central South University. Since 2006, She has been a Professor with the School of Information Science and Engineering, Central South University. Her research interests include matrix converter, adjustable speed drives, and wind energy conversion system.

Xing Li was born in Hunan, China, in 1988. She received the B.S. degree in Automation, in 1989, M.S. and Ph.D. degrees in electric engineering, in 2009 and 2014 respectively, all from the School of Information Science and Engineering, Central South University. She is currently an Assistant Professor with the College of Electrical and Information Engineering, Hunan University, China. Her research interests include power electronic converter and wind energy conversion system.

Fulin Liu was born in Shandong, China, in 1994. He received the B.S. degree in electronic engineering from Central South University, Changsha, China, in 2016, where he is currently working toward the M.S. degree. His research interests include matrix converter and dc/dc converters.

Yonglu Liu (S'16) was born in Chongqing, China, in 1989. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Central South University, Changsha, China, in 2012, 2015, and 2017 respectively. He has been an Associate Professor with the School of Information Science and Engineering, Central South University, China. His research interests include power electronics and renewable energy power conversion systems.