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고정 샘플링 주파수에서의 모듈형 멀티레벨 컨버터 레벨 선택 알고리즘

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Level Selection Algorithm with Fixed Sampling Frequency for Modular Multilevel Converter

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Abstract

This study uses a level selection algorithm with fixed sampling frequency for modular multilevel converter (MMC) systems. Theoretically, the proposed method increases the level infinitely while the sampling time remains the same. The proposed method called cluster stream buffer (CSB) consists of several clusters, wherein each cluster is composed of 32 submodules that depend on the level of the submodules in the MMC system. To increase the level of the MMC system, additional clusters are used, and the sampling time between clusters is determined from the sampling time between levels needed for utilizing the entire level from the MMC system. This method is crucial in the control of MMC-type HVDC systems because it improves scalability and precision.

Key words: NLC, Cluster stream buffer, VSC-HVDC, Switching time

1. Introduction

Modular multilevel converter (MMC) is an emerging and highly attractive topology for medium-voltage (MV) and high-voltage applications. Fig.1 shows the basic structure of the MMC system. Due to the modular structure of several cascaded submodules (SM), series connection of power-electronic devices is avoided. Thus, MMC system offers three distinctive features mentioned below which cannot be obtained from the classical two-level VSC topology, [1]-[4].

- The series connection of the arm inductor to the distributed energy storage capacitors greatly reduces the possibility of fault occurring inside or outside of the converter system.
- Lower switching frequencies (less than 3 times the fundamental frequency) make the overall converter losses closer to the thyristor technology.
- The output voltage is smooth and nearly ideal sinusoidal, which means only small or even no filters are required.

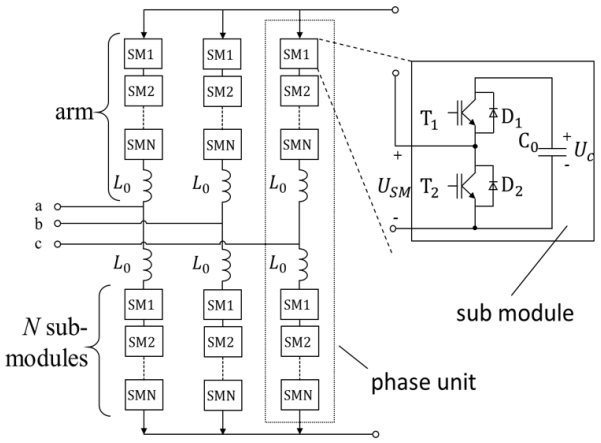

Fig. 1. Basic structure of MMC.

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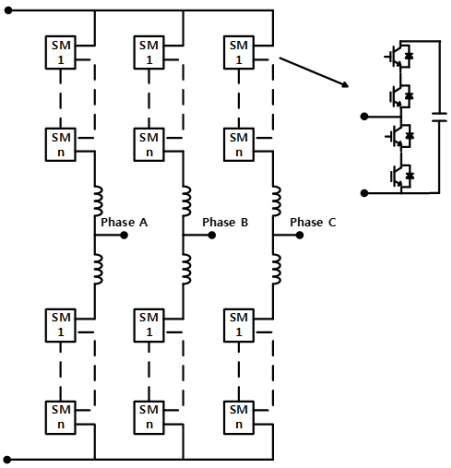


Fig. 2. ABB'S Group Module based MMC.

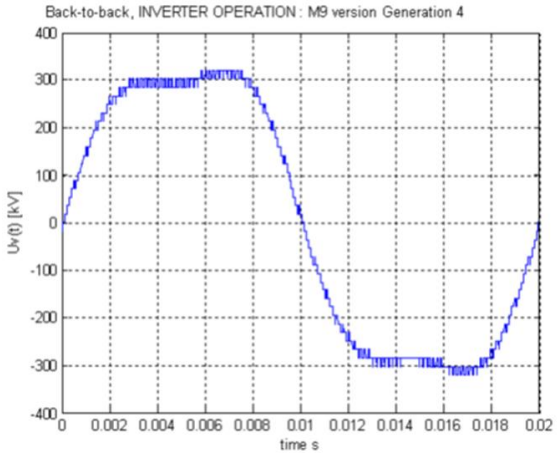


Fig. 3. Pole voltage of ABB's MMC using group module topology.

So far, the Pulse Width Modulation(PWM) scheme and space-vector modulation scheme have been utilized in MMC system[4]. However, the high switching frequency in the above mentioned modulation schemes lead to high switching losses and hence may not be suitable to very high power applications[5].

An improved version of selective harmonic elimination (SHE) method which is referred as active-harmonic-elimination method (AHEM) is proposed in [6]-[9] in order to reduce the switching losses. However, the large DC bus voltage in HVDC ransmission applications mainly determine the number of SMs of the converter to be large. Hence, due to the large number of SMs a large amount of switching angles of SHE method needs to be computed and the complexity of the numerical algorithm increases and puts a limitation to open-loop or low-bandwidth applications [10].

As a result, another two low-switching frequency modulation methods are mainly adopted : nearest vector control (NVC) and nearest level control (NLC). The NVC and NLC are the same in essence and can be realized online with high dynamic performance. The need for a program to realize the numerical algorithm capable of determining the closest vector makes the implementation of NVC method difficult. On the other hand, the NLC method become more suitable as the number of submodules in the MMC system increases. However, despite the simplicity and suitability of NLC method for converters with a high number of levels, the technical issue of MMC type HVDC system with NLC sorting algorithm is that the sampling time should gradually increases as the level goes up[13]. For example, a 500[kV] HVDC system with more than 251 levels (250 submodules) requires at least $33us$ sampling time to utilize all the 251 levels (250 submodules). This makes the sampling time of the controller to be at least $33us$ which becomes even higher if the MMC system use more than 250 submodules.

To solve this issues, some improved implementation methods have been proposed. First, ABB proposed a group module based MMC structure shown in Fig. 2 and its pole voltage is shown in Fig. 3. This method works in such a way that several serially connected submodules within a group module is activated like one submodule. However, in this system, a higher electric stress on the serial connected IGBTs occur due to the high harmonics level. As a result an additional snubber circuit is used in order to reduce di/dt of the IGBTs. In addition, the redundancy or margin of the number of IGBT must be increased. A group sorting algorithm and distributed control method for Modular multilevel converters are discussed in [11] and [12].

This paper deals with the NLC implementation method of the "Cluster Stream Buffer" which uses grouping and controlling the submodules, based on the time division method. This method doses not need to increase the sampling time of the phase controller of HVDC system despite the increase of the number of submodules. This can improve the scalability of the system which makes it easy to increase the HVDC capacity while the sampling time is the same. Finally, a time-domain simulation model with 325 SMs per arm is implemented in MATLAB/Simulink to validate the performance of the proposed NLC

modulation scheme using the "Cluster Stream Buffer" in MMC system.

2. Basic Structure and Operation Principle of MMC

2.1 Basic Structure

A three-phase MMC system is composed of six arms in which each arm contains N submodules connected in series with arm inductor, L_o. The upper and lower arm ofa single leg of MMC system makes a phase unit. A half bridge SM circuit is shown on the right side of Fig. 1. The SM output voltage, v_{SM}, is determined based on the switching states of the upper and lower IGBTs of the submodules. SM voltage, v_{SM}, becomes the capacitor voltage, v_c, when the upper and lower IGBTs are switched on and switched off, respectively. On the other hand, if the upper and lower IGBTs are switched off and switched on respectively, the SM voltage become zero. This means each SM has two states in normal operations: inserted ($v_{SM}=v_c$) or bypassed ($v_{SM}=0$).

2.2 Operation Principle

A single phase equivalent circuit of MMC system is shown in Fig. 4. In Fig. 4, the arm inductor and resistor are represented by L_o and R_o respectively. The total dc bus voltage of the MMC system and the converter output voltage of phase x are represented by V_{dc} and $v_{xs}(x=a,b,c)$, respectively. The line current of the phase is denoted by $i_{xs}(x=a,b,c)$ where x represents the three phases of the MMC system. The arm voltages generated by the cascaded SMs are expressed as v_{xu} and v_{xl} where the subscripts u and l denote the upper and lower arms, respectively. The arm currents i_{xu} and i_{xl} in Fig. 4 can be expressed by (1) and (2).

$$i_{xu}=i_{xo}+\frac{i_{xs}}{2} \tag{1}$$

$$i_{xu}=i_{xo}-\frac{i_{xs}}{2} \tag{2}$$

where i_{xo} is the inner circulating current of phase x, which flows through both the upper and lower arms and is given by:

$$i_{xo}=\frac{(i_{xu}+i_{xl})}{2} \tag{3}$$

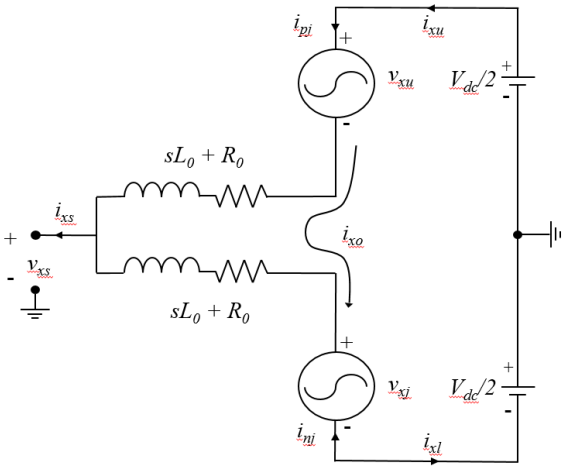


Fig. 4. Single-phase equivalent circuit of MMC.

According to [9], the MMC can be characterized by the following equations:

$$v_{xs}=e_{xs}-R_0*\frac{i_{xs}}{2}-\frac{L_0}{2}*\frac{di_{xs}}{dt} \quad ,(x=a,b,c) \tag{4}$$

$$L_0\frac{di_{xo}}{dt}+R_0i_{xo}=\frac{V_{dc}}{2}-\frac{(v_{xu}+v_{xl})}{2} \quad ,(x=a,b,c) \tag{5}$$

where e_{xs} in (4) is the inner emf generated in phase x and is expressed as:

$$e_{xs}=\frac{(v_{xl}-v_{xu})}{2} \tag{6}$$

From the relation in (4), considering v_{xs} as the ac grid network voltage, the line current i_{xs} can be regulated by manipulating the control variable e_{xs}. The vector control algorithm in the synchronous rotating reference frame can be applied to the MMC system in a similar way to AC motor drive application. The inner dynamic performance of the MMC which characterizes the relation between the inner unbalance voltage(v_{xo}) and the leg current(i_{xo}) is given by (5) and it is redefined as (7):

$$v_{xo}=L_0\frac{di_{xo}}{dt}+R_0i_{xo}=\frac{[V_{dc}-(v_{xu}+v_{xl})]}{2} \tag{7}$$

where v_{xo} is phase x inner unbalance voltage.

The unbalanced voltage, v_{xo} can be manipulated in order to regulate the difference current as per (7). The upper and lower arm current references can be derived by taking (6) and (7) into consideration and are given by (8) and (9).

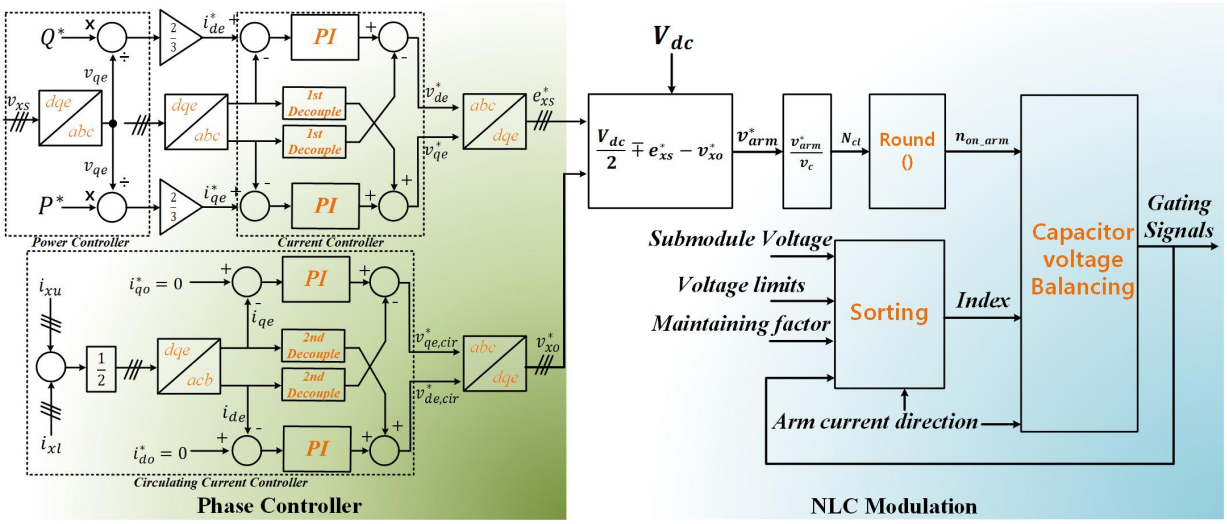


Fig. 5. MMC Control Diagram with NLC Modulation.

$$v_{xu\_ref} = \frac{V_{dc}}{2} - e_{xs}^{*} - v_{xo}^{*} \tag{8}$$

$$v_{xl\_ref} = \frac{V_{dc}}{2} + e_{xs}^{*} - v_{xo}^{*} \tag{9}$$

As it is seen in (8) and (9), to determine the upper and lower arm reference voltages, the same voltage v_{xo} is subtracted from both upper and lower arm voltages. The ac side is not affected by subtracting the same voltage from upper and lower arm reference according to (4) and (6). As shown in Fig.5, the e_{xs}^{*} and v_{xo}^{*} are generated by the current controller and the circulating current suppressing controller of the MMC system, respectively.

2.3 NLC method reviews

A specific modulation scheme is used to implement the reference voltages v_{xu_ref} and v_{xl_ref}. In multilevel converter system, three low-switching frequency modulation algorithms are used: selective harmonic elimination (SHE)[6], [7], [14]; nearest vector control (NVC); and nearest level control (NLC). However, in SHE method a large amount of switching angles is needed to be computed offline and stored in tables. So implementing SHE-based method of HVDC with a high number of submodules is complex and difficult. Relatively, the NLC modulation is easier to be implemented for HVDC system. Due to the conceptual implementation simplicity of the NLC method, the aim is to use it in converters with a high number of levels [9]. If the HVDC system has a sufficiently large number of submodules, a relatively low harmonic amplitude and THD could be achieved by using NLC modulation.

Fig. 5 shows the control diagram of the NLC modulation method. It is important to mention that in digital-signal-processing systems, the uniform sampling frequency f_s of the reference voltage, v_{ref}, must be taken into account. When a uniform sampling method is applied to control a system with large number of SMs, a high enough sampling frequency is needed to ensure that the resulting voltage level utilizes all SMs. In case of small sampling interval, every SM of Fig. 6 generates one voltage level and hence each voltage step is v_c. So using a smaller sampling frequency reduces the level of the output voltage to produce the exact output voltage as shown in Fig 6. But as shown in Fig. 7, the first and third voltage steps are $2v_c$ in case of large sampling interval. The voltage reference shown in Fig. 6 and Fig. 7, v_{ref} is a staircase waveform with the sampling interval $T_s = 1/f_s$ instead of the sinusoidal waveform(blue line in Fig. 6 and Fig 7). The closest voltage level is determined by dividing the sampled reference voltage, v_{ref} by the value of the capacitor voltage.(here, v_c is considered to be a constant which is V_{dc} divided by total number of submodules). Finally, the closest voltage level is used to determine the number of submodules to be turn on. The round(x) function is used to determine the number of the turn-on submodules in one arm. The function returns the nearest integer of the input number(e.g., round(3.4) = 3, round(3.6) = 4). In each arm, the total number of SMs to be switched on, n_{on_arm}, is calculated.

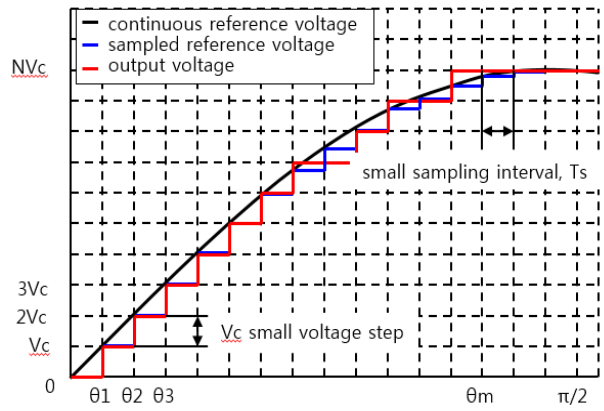


Fig. 6. Output voltage of NLC with small sampling interval.

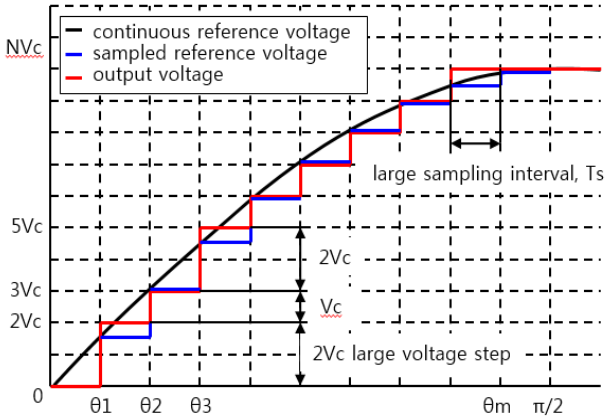


Fig. 7. Output voltage of NLC with large sampling interval.

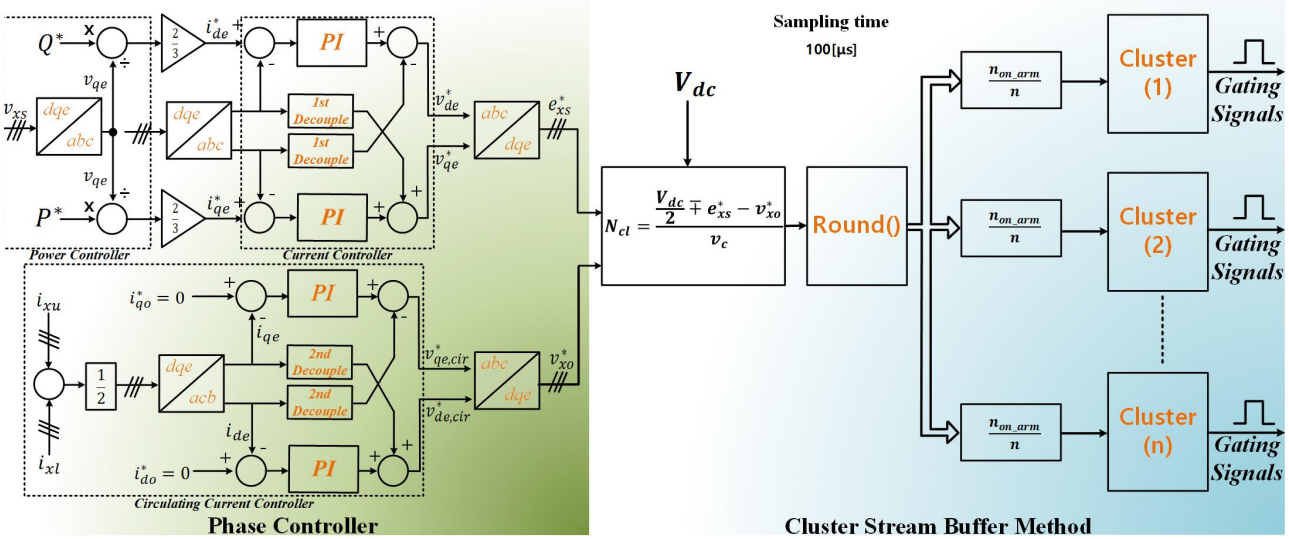


Fig. 8. Actual implementation of the proposed "Cluster stream buffer" method for MMC.

3. Proposed NLC Method: Cluster Stream Buffer Method

3.1 Cluster Stream Buffer Method

Fig. 8 shows the actual implementation of the cluster stream buffer method, which shows that the switching level is commanded in the phase controller with the fixed sampling time of the MMC based VSC-HVDC system using NLC modulation. As shown in Fig. 9, the proposed cluster stream buffer method arranges the MMC system as a combinations of clusters, where each cluster is composed of 32 submodules, and the number of the cluster increases as the submodule level (or voltage level) increases. The advantages of the proposed method is to ensure the scalability of the MMC system while keeping the sampling time constant, and improve the precision of the control system in the MMC HVDC system.

Unlike the group module approach used by ABB, which switches the series connection of the IGBT devices simultaneously, the proposed algorithm switches the cluster connection of the IGBT devices one by one. The individual switching of the IGBTs reduce the harmonic content of the converter system which have a significant effect specially in the high level MMC system. Hence, this method greatly improves the reliability of the IGBT modules of MMC system. In addition, due to the one by one switching of the IGBTs, the stress level on the IGBT during switching become smaller, which results in a smaller harmonic. This features give an advantage by avoiding the need of additional snubber circuit. As shown in Fig. 8, the current controller and the circulating current controller generate the three phase inner emf (e_{xs}) and the inner unbalance voltage, v_{xo}, respectively. The inner emf and the inner unbalance

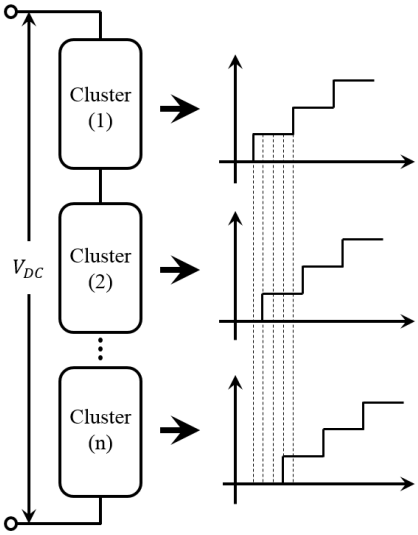


Fig. 9. Cluster module based MMC arm.

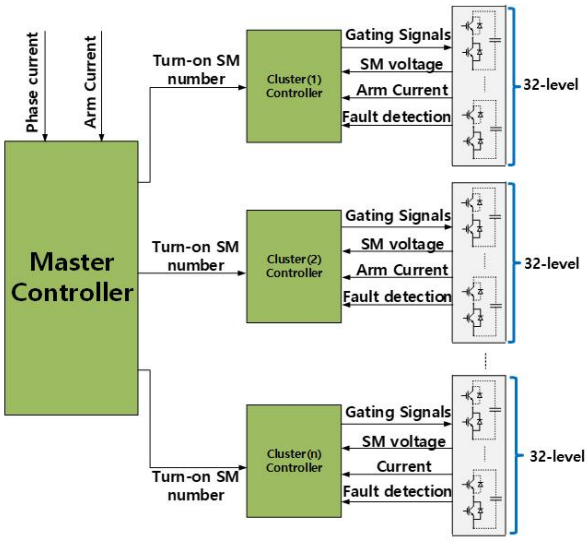


Fig. 10. Cluster module based MMC controller H/W structure.

voltage along with V_{dc} are used to determine the total number of the submodule to be turn on, N_d , for each arm of the MMC system. The total number of the submodules that need to be turned on, N_d, is divided by the total number of clusters ,n, and the result is transmitted to each cluster controller.

Fig. 10 shows the simple H/W block diagram of the cluster stream buffer control method. Each cluster controller corresponds to one cluster. This controller includes voltage measurement of each submodule, the generation of the gating signal for IGBT, emergency signal related to the failure of the submodule, as well as the current measurement of each arm for the sorting algorithm operation within each cluster. The cluster units shown in Fig. 9 and Fig. 10 are made of 32 levels for the simplicity of the system.

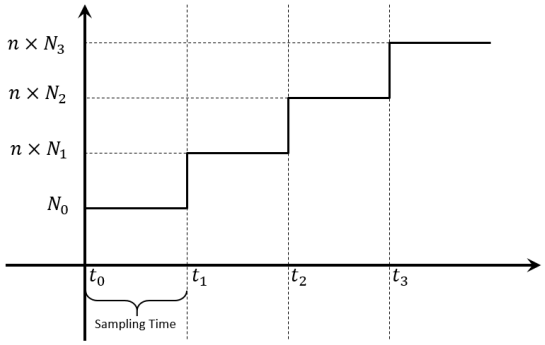


Fig. 11. Output voltage level of MMC based VSC-HVDC without cluster stream buffer method.

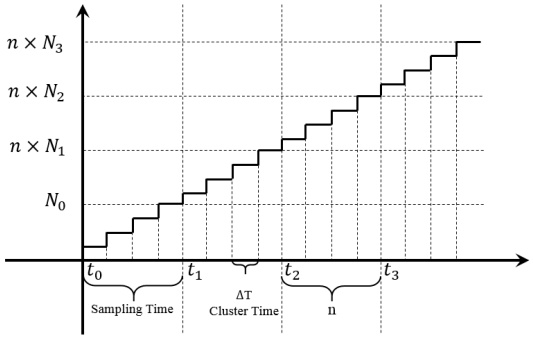
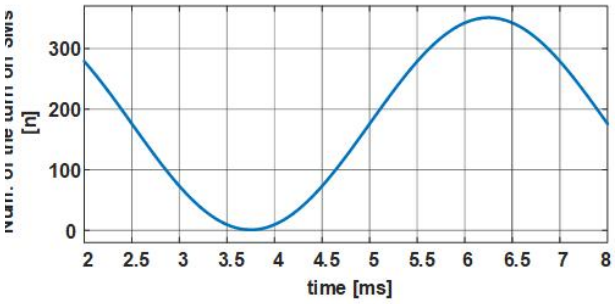


Fig. 12. Output voltage level of MMC based VSC-HVDC using cluster stream buffer method.

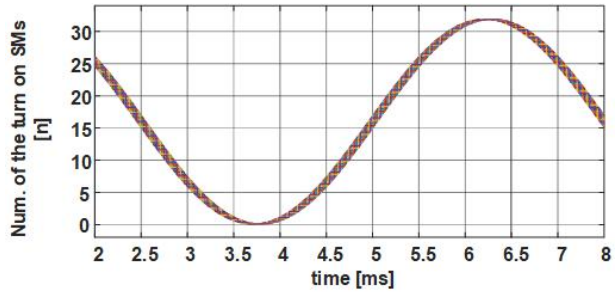
The total submodules of the system are divided into several clusters based on the system frequency. And the time delay of the sub-modules is switched in the same order as Cluster 1, Cluster 2, and Cluster (n) as shown in Fig. 10. The number of IGBTs in a cluster can be chosen to be 16, 32 or 64. However, selecting 16 IGBTs in a cluster needs many cluster controllers while expanding the MMC system to a higher level and selecting 64 IGBTs in a cluster causes a reduction in the reliability and the control resolution of the system. Therefore, in order to optimize both the number of controller and reliability of the system, this paper organizes each cluster to have 32 IGBTS. Then, the output voltage of the MMC based VSC-HVDC system using the proposed method has a much higher level as shown in Fig. 12 than that of the conventional method shown in Fig. 11.

3.2 Simulation and review

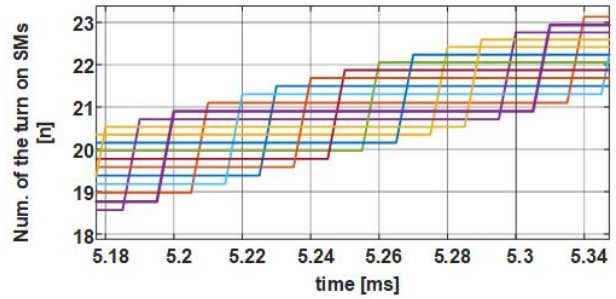
The simulation of the cluster stream buffer method is implemented using MATLAB/Simulink platform. The model used in the simulation is composed of 11 cluster and each of the cluster has 32 submodules, which results a total of 352 submodules in one arm



(a) The output of the NLC method



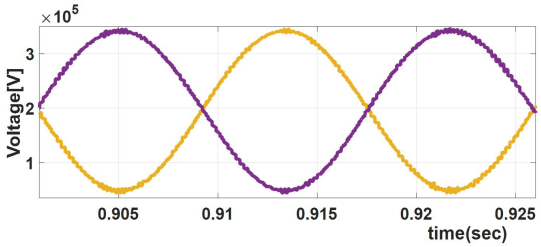
(b) Output of the cluster stream buffer method with 11-cluster



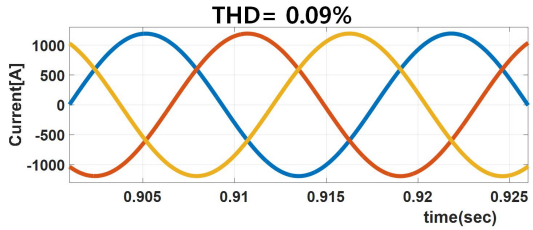
(C) Enlarged waveform of Fig. 13(b)

Fig. 13. Simulation result of the proposed algorithm: Cluster stream buffer.

of the MMC system. Fig. 13 shows the simulation result of the proposed cluster stream buffer method. The total number of the turn on submodules in the arm of MMC system determined by the combined operation of the current controller, circulating current controller and NLC modulation method is shown in Fig. 13(a). The number of the turn on submodules in each cluster are generated and shown in Fig 13(b). The summation of the number of turn on submodules given in Fig 13(b). makes the total number of the turn on submodules as shown in Fig. 13(a). Since the proposed algorithm equally divides the total number of turn-on signals depending on the magnitude of the submodule voltages, every cluster is well balanced signals as shown in Fig 13(c). The performance of the proposed algorithm compared with the conventional method with respect to the THD of the output voltage is presented by the matlab

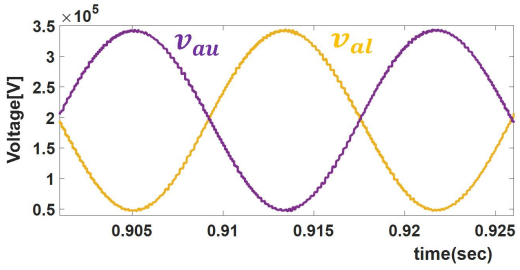


(a)

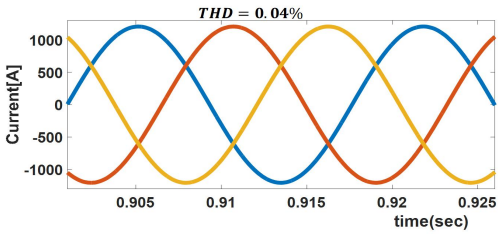


(b)

Fig. 14. Simulation result of conventional method. (a) Upper and lower arm voltages, (b) Three phase output current.



(a)



(b)

Fig. 15. Simulation result of proposed method. (a) Upper and lower arm voltages, (b) Three phase output current.

simulation result presented in Fig. 14. As it is seen from Fig. 15, the proposed algorithm improved the level of arm voltages of the MMC system and hence the THD of the output current waveform become smaller than that of the conventional method shown in Fig. 14. The parameters used in the simulation are listed in Table I.

4. Conclusion

In this paper, a new switching topology for easily expanding the MMC capacity to several levels while maintaining fixed sampling time is presented and

TABLE I
SIMULATION PARAMETER OF GRID CONNECTED MMC SYSTEM

Parameters	Value
DC-link voltage	400[KV]
SM capacitance	4500[mF]
Arm inductor	15[mH]
No. of SM per arm	352
Sampling Frequency	10[KHz]
Grid Voltage	115[KV]
Rated Power	400[MW]

validated. An explanation to the difference in the harmonics of the converter output voltages during group module and cluster approach was given. The proposed algorithm provided several advantages compared to the classical group module approach. Even if, a number of IGBTs are connected in series, the number of switching IGBT in the proposed method is one. Due to the one by one switching of the IGBTs, the stress level on the IGBT during switching become smaller, which results in a smaller harmonic. As a result, in the proposed method, there is no need of using additional snubber circuit and hence there is no unnecessary losses. By using the proposed method, Cluster Stream Buffer method, it is possible to extend the HVDC system to hundreds of levels without altering the sampling time of the phase controller. This will avoid the complexity that occurs during the expansion of the MMC system. Simulation results are given to validate the performance of the method.

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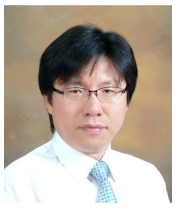

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