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Design and Control of a Bidirectional Power Conversion System with 3-level T-type Inverter for Energy Storage Systems

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Abstract – In this paper, the design process and the control method of the power conversion system (PCS) that consists of a bidirectional DC-DC converter and a 3-level T-type inverter for an energy storage system is presented. Especially the design method of the output LCL filter for a 3-lvel T-type inverter without complex mathematical process are proposed. The validity of the control method and design process in this paper are verified through simulation and experimental analysis.

Keywords: Energy storage system (ESS), Multi-level inverter, 3-level T-type Inverter, Grid-connected inverter, bidirectional inverter

1. Introduction

A power conversion system (PCS) for an energy storage system (ESS) requires high-quality output currents. Therefore, the volume of the output low pass filter (LPF) should be bulky or switching frequency of the grid-connected inverter should be increased. However, the bulky LPF causes a decrease in power density. On the other hand, an increased switching frequency causes an increase in switching loss of the power semiconductor. Therefore, a 3-level inverter such as a neutral point clamped (NPC) inverter, a flying capacitor inverter, and a T-type inverter has the advantages over a 2-level inverter in terms of high quality of output currents [1-4].

Although the conduction loss increases in a 3-level inverter due to the additional neutral-point-switches, it has been applied to high-voltage grid-connected systems such as those used in wind-power generation. The main reason is that the number of output voltage levels in the 3-level inverter is more than that of the 2-level inverter. Therefore, a 3-level inverter has a low electromagnetic interference (EMI), a small volume of the output filter size, a low switching loss, and a low THD of the output voltage compared to a 2-level inverter [1-4]. Considering these factors, a low-voltage and low-power PCS for an ESS with a 3-level inverter is investigated in this study.

The control methods for the charging and discharging operations of the PCS are presented in this paper. In addition, a design process of the output LCL filter for the 3-level inverter is suggested. Previous studies have not considered the optimal design method of the output filter for a 3-level inverter seriously [5-9]. Therefore, this paper describes a method to reduce the size of the output filter in detail.

Finally, control methods of the PCS for the ESS with the 3-level inverter and the design process of the LCL filter are verified by simulation and experimental analysis.

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2. Control Systems of PCS for ESS

The target system in this study is a 5-kW PCS consisting of the 3-level inverter and the bidirectional buck-boost converter as shown in Fig. 1. In case of the 3-level inverter, various topologies can be applied, such as a NPC inverter, a flying capacitor inverter, and a T-type inverter. Among them, the 3-level inverter is advantageous in terms of loss because the number of power semiconductor devices or passive components is small than the others [1]. Therefore, the 3-level T-type inverter is used in the target system.

The control targets of the bidirectional buck-boost converter and the 3-level inverter according to the operation modes of the ESS are listed in Table 1. The ESS operates in charging mode during daytime and discharging mode at night. Therefore, the PCS can be driven by the control methods listed in Table 1, regardless of the transfer time due to the operation mode change of the ESS.

The configurations of the controllers for both the modes are shown in Fig. 2. In the charging mode, the controller of bidirectional buck-boost converter in Fig. 2(a) controls the battery current and voltage. On the other hand, the controller of the 3-level T-type grid-connected inverter in Fig. 2(b) controls the grid currents and the DC-link voltage.

Table 1. Control targets of the PCS

Operation mode	DC-DC converter	3-level inverter
Charging	Battery voltage Battery current	DC-link voltage Grid current
Discharging	DC-link voltage	Grid current

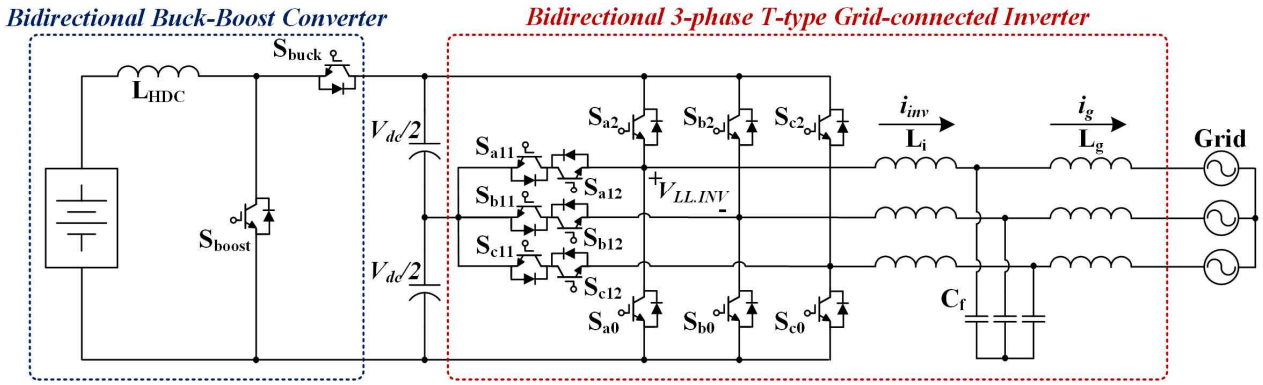
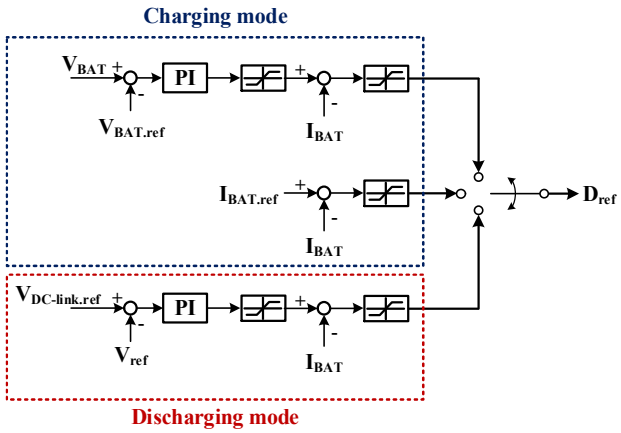
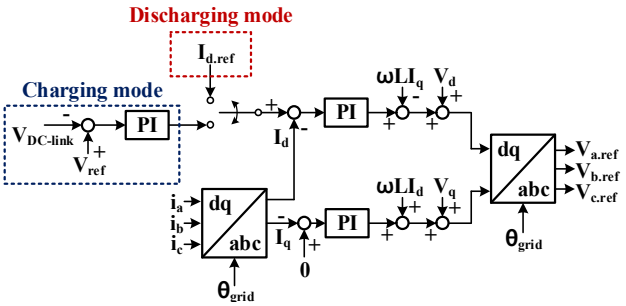


Fig. 1. Configuration of PCS for ESS



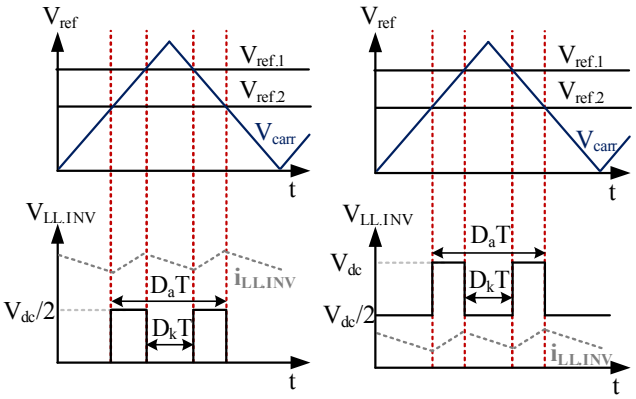
(a) Controller of buck-boost converter



(b) Controller of grid-connected inverter

Fig. 2. Configuration of PCS controller

In case of the discharging mode, the bidirectional buck-boost converter controls the DC-link voltage and the 3-level T-type grid-connected inverter controls the grid currents. It is to be noted that the controllers of the inverters shown in Fig. 2(b) require a feedforward because large grid currents are injected into the DC-link without it. In addition, a balancing algorithm is required for the DC-link. In case of the 3-level T-type inverter, neutral point switches cause unbalance of the separated DC-link voltages, as shown in Fig. 1. This unbalancing problem can be solved by adding an offset voltage to the reference voltage of inverters. For example, when the high-side DC-link voltage is higher than that of the low-side, a positive



(a) $0<V_{g.LL}<0.5V_{dc}$ (b) $0.5V_{dc}<V_{g.LL}<V_{dc}$

Fig. 3. Line-to-line voltages of the 3-level T-type inverter

offset voltage is added to the low-side reference voltage. As a result, the low-side voltage increases and the high-side voltage decreases. Using this method, controllers of the inverter in Fig. 2 and 3 perform DC-link balancing control [1, 10, 11].

3. Design of LCL Filter for 3-level T-type Inverter

As mentioned in the previous section, the output filter of a 3-level T-type inverter can be designed to be smaller than that of a 2-level inverter. However, previous studies are not serious considered about the optimal design process of an LCL filter. Therefore, the design process of an LCL filter for a 3-level T-type inverter is suggested in this section.

3.1. Output characteristics of 3-level T-type inverter

In order to derive an optimal design process of the LCL filter, an analysis of the output current and voltage of the 3-level T-type inverter is required. First, characteristics of the output voltage by conditions of duty (D_a), the DC-link voltage (V_{dc}), the inverter output line-to-line current ($i_{LL.P}$) and the grid line-to-line voltage ($V_{g.LL}$) should be analyzed.

Fig. 3 shows line-to-line voltage of 3-level T-type inverter ($V_{LL.INV}$) by reference voltages (V_{ref1} and V_{ref2}). In this figure, the D_a is on-duty period by V_{ref1}.

The magnitude of the output line-to-line voltage in the D_k is the same with the off-duty (1-D_a) period because of V_{ref2}. The phase difference between V_{ref1} and V_{ref2} is always $2\pi/3$, since the reference voltages are balanced 3-phase voltages. The conditions that the output current ripple ($i_{LL.INV}$) is maximum value is when the current increase time and the current decrease time is the same [12]. These conditions are presented in Eq. (1) and in this equation, m_a is the amplitude modulation index. In Eq. (1), when the values of ωt are 0.7401π or -0.1638π, the current ripple of $i_{LL.P}$ is the maximum value. Therefore, the amplitude of V_{ref1} is $0.729m_a$, V_{ref2} is $0.229m_a$ and the other is $-0.957m_a$ (V_{ref3}).

$$V_{ref1} - V_{ref2} = m_a\left[\sin(\omega t+\phi) - \sin(\omega t+\phi-\frac{2}{3}\pi)\right] = 0.5 \quad (1)$$

Fig. 4 shows inverter phase voltage of 3-phase T-type inverters (V_{INV}). In this figure, the influence of V_{ref3} can be ignored in the phase ripple current because the m_a of V_{ref3} is relatively close to 1 than V_{ref1} and V_{ref2} as derived by Eq. (1).

Eqs. (2)-(4) show the relationship between voltage and ripple current in Fig. 4(a). In these formulae, $\Delta i_{P.inc}$ is infinitesimal changes of increasing output phase current in each section in Fig. 4(a). The decrease ripple current within $(1\text{-}D_a)T$ and D_kT is represented by the increase ripple current ($\Delta i_{P.inc}$) using the ratio of D_a, D_k, and reference voltages (V_{ref1} and V_{ref2}).

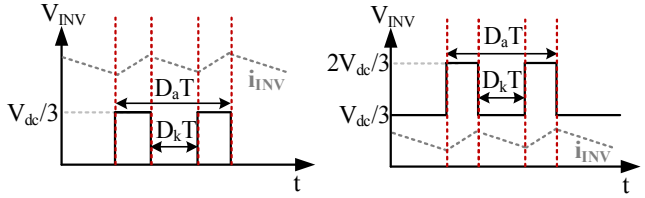
$$V_g = L_{eq}\frac{0.458\Delta i_{P.inc}}{(1-D_a)}f_s \quad (2)$$

$$V_g = -L_{eq}\frac{2\Delta i_{P.inc}}{(D_a-D_k)}f_s + \frac{V_{dc}}{3} \quad (3)$$

$$V_g = L_{eq}\frac{0.542\Delta i_{P.inc}}{(D_k)}f_s \quad (4)$$

In the condition of Fig. 4(b), the equations of $\Delta i_{P.inc}$ is presented in Eqs. (5)-(7).

$$V_g = L_{eq}\frac{0.458\Delta i_{P.inc}}{(1-D_a)}f_s + \frac{V_{dc}}{3} \quad (5)$$



(a) $0<V_g<0.5V_{dc}$ (b) $0.5V_{dc}<V_g<V_{dc}$

Fig. 4. Phase voltages of the 3-level T-type inverter

$$V_g = -L_{eq}\frac{2\Delta i_{P.inc}}{(D_a-D_k)}f_s + \frac{2V_{dc}}{3} \quad (6)$$

$$V_g = L_{eq}\frac{0.542\Delta i_{P.inc}}{(D_k)}f_s + \frac{V_{dc}}{3} \quad (7)$$

Using Eqs. (2)-(7), the maximum ripple of i_{INV} ($\Delta i_{p.max}$) in Fig. 4 can be derived as Eq. (8).

$$\Delta i_{p.\max} = \frac{V_{dc}}{18L_{eq}f_s} \quad (8)$$

Based on this analysis, the optimal design process of the LCL filter for a 3-level T-type inverter can be derived. The derived $\Delta i_{p.max}$ is equivalent to current ripples of filter inductors. By this result, optimal parameters of inductors in the LCL filter are calculated.

3.2. LCL filter design for 3-level T-type grid-connected inverter

First of all, the inverter-side inductor (L_i) can be derived by (8). It can be designed by using allowable maximum current ripple of inverter-side current ($\Delta i_{INV.max}$) at the switching frequency (f_s) as shown in (9).

The filter capacitor (C_f) can be calculated by a rated power of the single phase (P_{rate}) and a ratio of allowable reactive power (β) at the fundamental frequency of the grid (f_{grid}) as depicted in Eq. (10).

$$L_i = \frac{V_{dc}}{18\Delta i_{INV.\max}f_s} \quad (9)$$

$$C_f = \beta\frac{P_{rate}}{2\pi f_{grid}V_{g.rate}^{\ 2}} \quad (10)$$

$$\alpha\Delta i_{\mathrm{INV.max}} = \left|\frac{1}{1+C_fL_is^2}\right|\Delta i_{\mathrm{INV.max}} \quad (11)$$

$$L_g = \frac{1+\alpha}{\alpha C_f(2\pi f_s)^2} \quad (12)$$

Finally, the grid-side inductor (L_g) can be calculated from the short circuit model in the high-frequency band shown in Fig. 5. In this figure, α is the ratio of the inverter-side to the grid-side current, and $i_{INV.h}$ is the high-order

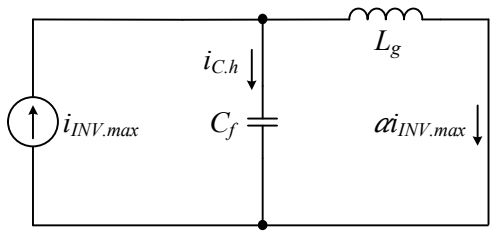


Fig. 5. Equivalent single-phase short circuit model in high-frequency band

harmonic ripple current of the inverter-side current that is calculated by (10). The relationship between the grid-side and the inverter-side ripple current is shown in Eq. (11). Using (11), L_g can be designed as shown in Eq. (12). Using these results, it is possible to design the LCL filter for the 3-level T-type inverter.

4. Simulation and Experimental Results

In order to verify the design and control method, simulation and experiment of the PCS with the 3-level T-type inverter are performed. The specifications and results of the design are shown in Table 2 and 3 respectively. The LCL filter in Table 3 is designed to satisfy the standards for harmonic currents (IEEE-519 standard).

Table 2. Specification of the PCS

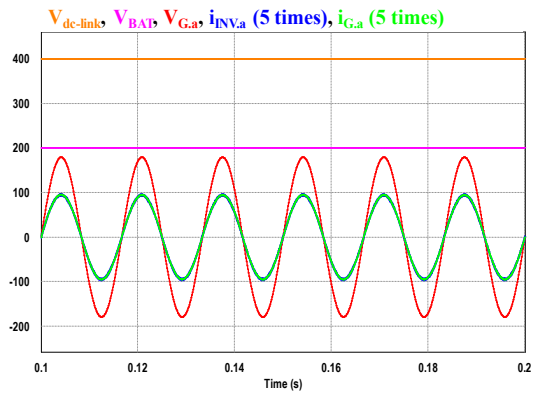
Parameter	Specification
Rated power	5 kW
Grid voltage	220 $V_{rms.LL}$
Grid frequency	60 Hz
DC-link voltage	400 V_{dc}
Switching frequency	30 kHz

Table 3. Design result of the LCL filter

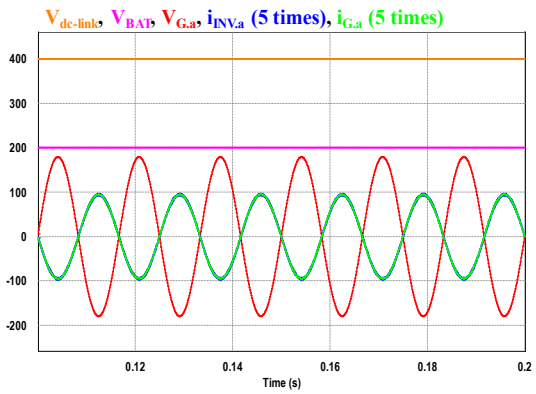
Parameter	Specification
Inverter-side inductor	0.60 mH
Grid-side inductor	0.46 mH
Filter capacitor	1.50 uF

4.1. Simulation results

Simulation results are shown in Fig. 6 applied the control method in Table 1. Fig. 6 (a) shows the results of the discharging mode. In this mode, the grid currents and the DC-link voltage are controlled by the 3-level T-type inverter and the bidirectional buck-boost converter respectively. The simulation results of the charging mode are shown in Fig. 6 (b). In this scenario, the 3-level T-type inverter controls both the grid-current and the DC-link voltage and the bidirectional buck-boost converter controls the input current and voltage of the battery. As can be seen, the PCS operates properly both in the charging and discharging modes. These results show that the present control method can be applied in the PCS for ESS with the 3-level T-type inverter. In order to verify the design process of the LCL filter, the maximum values of the inverter-side and grid-side currents are also analyzed through the simulation as shown in Fig. 7. Fig. 7(a) and

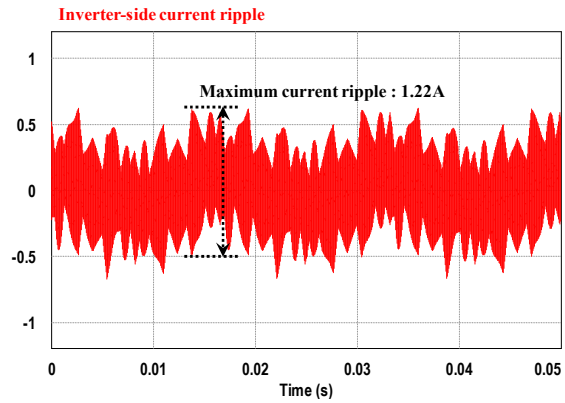


(a) Simulation waveforms in discharging mode

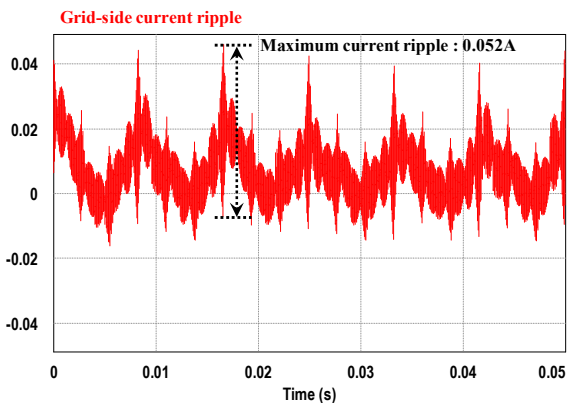


(b) Simulation waveforms in charging mode

Fig. 6. Simulation results of PCS with designed LCL filter



(a) Simulation waveforms of inverter-side current ripple



(b) Simulation waveforms of grid-side current ripple

Fig. 7. Simulation results of LCL filter currents

(b) are the inverter-side and grid-side current ripple with the maximum value of 1.22 A and 0.052 A, respectively. On the other hand, values of calculation results using the analysis results are 1.23 A and 0.051 A, respectively. There are errors associated with both the simulation and experimental results because the resonance between the inductors and the capacitor in the designed LCL filter is not considered. In addition, the design process of the LCL filter in this paper is carried out under the condition that the inverter-side and grid-side both have the maximum values of ripple currents. However, the error is negligible because it is very small as compared to fundamental currents. Therefore, the present design process is reliable and simulation results show that it can be applied to design the LCL filter for the 3-level inverter.

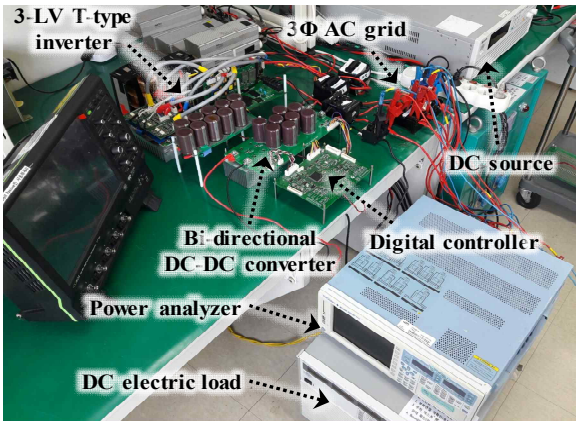
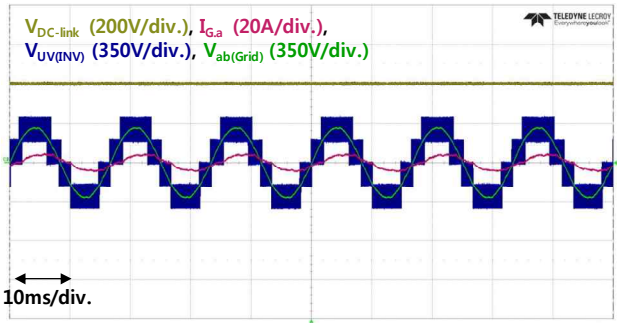


Fig. 8. 5kW prototype of the PCS with 3-level T-type inverter and experimental environment

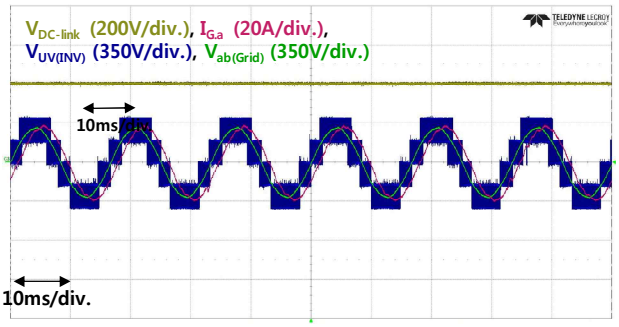
4.2 Experimental results

A 5-kW PCS prototype for the ESS is designed by the proposed design process and controlled by the present control scheme. The prototype and experimental environment are shown in Fig. 8. Experimental conditions are the same as in the previous section.

Fig. 9 and 10 is the experimental results of the 3-level T-type inverter in the light load (1 kW) and the full load (5 kW) and Fig. 11 shows the results of the total PCS for ESS applying the bidirectional buck-boost converter in charging and discharging mode at 5 kW. As can be seen, the PCS using the present control method operates properly under both the charging and discharging modes in the designed load region. In addition, average values of THD of output currents are 2.8% and 2.9% in the charging and discharging mode respectively that satisfy the standard of harmonic currents (IEEE-519 standard). The experimental results show that the control methods and the process of the LCL filter presented in this paper are reasonable to be applied in the PCS with 3-level T-type inverters for ESS.

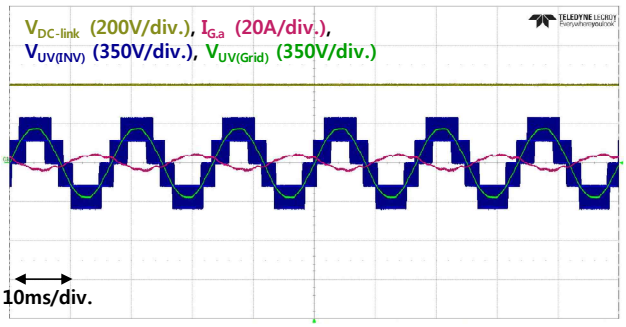


(a) Experimental waveforms in discharging mode (1 kW)

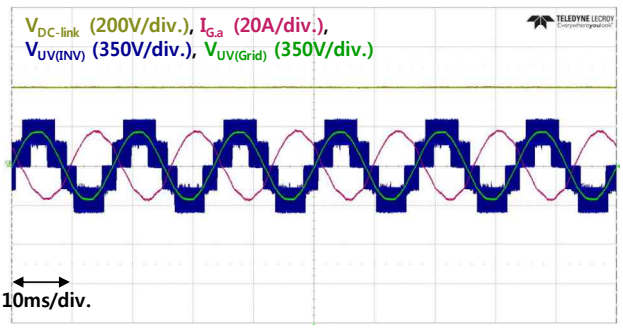


(b) Experimental waveforms in discharging mode (5 kW)

Fig. 9. Experimental results of the 3-level T-type inverter in discharging mode

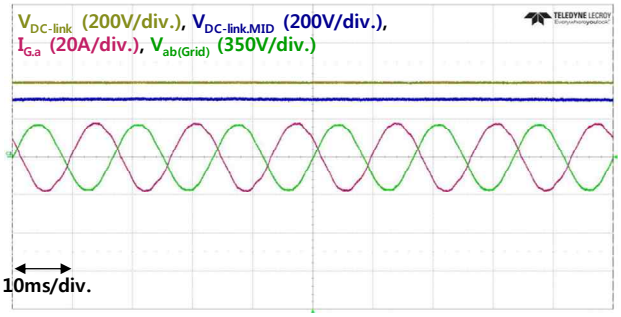


(a) Experimental waveforms in charging mode (1 kW)

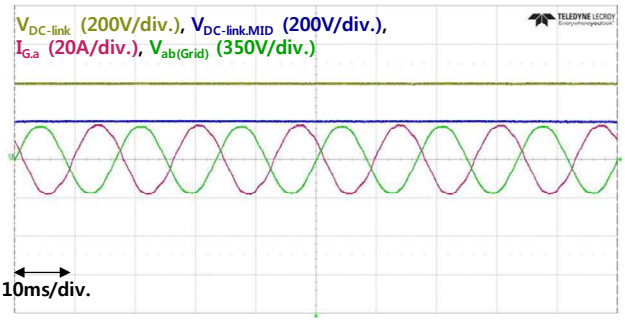


(b) Experimental waveforms in charging mode (5 kW)

Fig. 10. Experimental results of the 3-level T-type inverter in charging mode



(a) Experimental waveforms in discharging mode (5kW)



(b) Experimental waveforms in charging mode (5kW)

Fig. 11. Experimental results of the PCS

5. Conclusion

In this paper, the control method of the PCS with 3-level T-type inverters for ESS and the design process of the LCL filter are presented without involving complex mathematics. Furthermore, the validity of the control method and the design process of the PCS for the ESS are verified through simulation and experimental results. Therefore, the present control method and the design process can be applied to the actual design of the PCS with the 3-level T-type inverter for ESS.

Acknowledgements

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References

[1] C. Y. Oh, "Design and Control of Energy Storage Systems based on 3-Level T-Type Inverters," Ph.D. dissertation, Dept. Elect. Comput. Eng., Sungkyun-kwan Univ., Suwon, Korea, 2016.

[2] B. Ren, X. Sun, S. An, X. Cao, Q. Zhang "Analysis and Design of an LCL Filter for the Three-level Grid Connected Inverter," *2012 IEEE 7th Int. Power Electron. and Motion Cont. Conf.*, Harbin, China, pp. 317-318, Jun. 2012.

[3] P. Alemi, "Analysis and Control of Grid-Connected Three-Level T-type Converters," Ph.D dissertation, Dept. Elect. Eng., Yeungnam Univ., Gyeongsan, 2014.

[4] H. M. Ahn, C. Y. Oh, E. S. Jang, and B. K. Lee, "Design of Output Filter for Grid Connected 3-level T-type Inverter," *2016 Power Electronics Annual Conference*, Buan, Korea, pp.317-318, Jul. 2016.

[5] T. C. Wang, Z. Ye, G. Sinha, and X. Yuan, "Output Filter Design for a Grid-interconnected Three-Phase Inverter," *PESC 2003*, Acapulco, Mexico, Jun. 2003.

[6] Q. Liu, L. Peng, Y. Kang, S. Tang, Deliang Wu, and Y. Qui, "A Novel Design and Optimization Method of an LCL Filter for a Shunt Active Power Filter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 4000-4010, Aug. 2014.

[7] P. Channegowda and V. John, "Filter Optimization for Grid Interactive Voltage Source Inverters," *IEEE Trans. Ind. Electron*., vol. 57, no. 12, pp. 4106-4114, Dec. 2010.

[8] H. M. Ahn, C. Y. Oh, W. Y. Sung, J. H. Ahn, and B.K. Lee, "Analysis and design of LCL filter with passive damping circuits for three-phase grid-connected inverters," *J. Elect. Eng. Tech.*, vol. 12, no. 1, pp. 217-224, Jan. 2017.

[9] S. Lim, and J. Choi, "LCL Filter Design for Grid Connected NPC Type Three-Level Inverter," *IJRER*, vol. 5, no. 1, pp. 45~53, 2015.

[10] C. Xia, X. Gu, T. Shi and Y. Yan, "Neutral-point potential balancing of three-level inverters in direct-driven wind energy conversion system," *IEEE Trans. Energy Convers.*, vol. 26, no. 1, pp. 18-19, Mar. 2011.

[11] J. Shen, S. Schrüder, and R. Roesner, "A neutral point balancing controller for three-level inverter with full power-factor range and low distortion," *In IEEE Energy Conversion Congr. and Expo.*, pp. 3419-3426, 2011.

[12] *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems,* IEEE standard 519-192, 10, May 1992.

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