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3-Level T-type Inverter Operation Method Using Level Change

Tae-Hun Kim* and Woo-Cheol Lee†

Abstract – In this study, a selective inverter operation between a 2-level voltage source converter (VSC) and a 3-level T-type VSC (3LT VSC) is proposed to improve the efficiency of a 3LT VSC. The 3LT VSC topology, except for its neutral-point switches, has similar operations as that of the 2-level VSC. If an operation mode is changed according to efficiency, the efficiency can be improved because efficiencies of each methods are depending on current and MI (Modulation Index). The proposed method calculates the power losses of the two topologies and operates as the having lower losses. To calculate the losses, the switching and conduction losses based on the operation mode of each topology were analyzed. The controller determined the operation mode of the 2- or 3-level VSC based on the power loss calculated during every cycle. The validity of the proposed control scheme was investigated through simulation and experiments. The waveform and average efficiency of each method were compared.

Keywords: T-type, inverter, 3-level, Loss, Efficiency

1. Introduction

A 2-level voltage source converter (VSC) is used for many systems because of its simple configuration and the ensured reliability [1]. However, the 2-level VSC has limit to improve the efficiency and performance. Recently, multilevel inverters are being researched to overcome the limitations of the 2-level VSC.

Multilevel inverters have several advantages as compared to 2-level VSC. Both reduce switching and harmonic losses and generate high quality output voltage because the switching voltage of the switch is half the DC-link voltage [2, 3]. Multilevel inverters such as the neutral-point-clamped (NPC), active NPC (ANPC) and H-bridge have advantages in terms of medium voltage [4-6]. However, these topologies have the disadvantage of high conduction losses because of their increased number of semiconductors. Thus, they are not ideal for low voltage applications. Therefore, a 3-level T-type VSC (3LT VSC) has been proposed to apply the conventional 3-level inverter to a low-voltage application [7]. The 3LT VSC has the advantage of low conduction losses as a result of a decrease in the number of switches and isolated gate drivers compared to conventional multilevel topologies such as NPC. The multi-level inverter has a disadvantage of increasing the number of devices, and various studies have been carried out to overcome this disadvantage. Studies to improve the efficiency of the T-type VSC include research on new devices, efficient PWM and operating methods, optimization designs, and so on [8-10]. Previous studies have shown that the 3LT VSC has low switching loss characteristics and achieves high efficiency compared to the 2-level VSC in low voltage conditions and when the switching frequency is higher than 10 kHz [10, 11].

The 3LT VSC has characteristics analogous to the conventional 2-level VSC. The 3LT VSC is composed of the same circuit as the 2-level VSC with an additional two neutral point switches. Therefore, the 3LT VSC can operate in the same manner as a 2-level VSC depending on the situation. The 3LT VSC efficiency depends on the amplitude modulation index (MI) if the switching frequency and DC-link voltage are the same. If the MI is small (i.e., close to zero), the efficiency of the 3LT VSC decreases as a result of the increase in conduction losses. Specifically, conduction losses depend on the turn-on ratio of the neutral point switches and on the MI. However, as previously mentioned, the 2-level VSC does not have neutral-point switches. Therefore, the 2-level VSC has higher efficiency than the 3LT VSC at a low MI. If the 3LT VSC operation mode is changed to that of a 2-level VSC at a low MI, the efficiency of the 3LT VSC will be the same as that of the 2-level VSC. By contrast, the 3LT VSC will have higher efficiency than that of the 2-level VSC at a high MI. If the average loss in a 60 Hz period is calculated and compared, the operation mode can be changed to another more efficient operation mode. Therefore, the system can achieve the efficiency of a 2-level or a 3LT VSC [12, 13].

In this study, a mode transition scheme for optimal efficiency is proposed. If operation mode is changed according to efficiency, the efficiency can be improved because efficiencies of each method are depending on current and MI. The proposed method calculates the power losses of the two topologies and operates as the having

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lower losses. The controller performs a loss calculation and a comparison at each control period 10 and 15 kHz. If the loss calculation of the 3LT VSC result in a lower value than that of the 2-level VSC, the 3LT VSC operation is selected; otherwise, the 2-level VSC operation is selected. Therefore, in a 60 Hz period, the 3LT and 2-level VSC operation regions exist, and the average efficiency will be higher than that of the individual operation method. The proposed method is verified by means of a power sim (PSIM) simulation and experiments. The waveform and average efficiency of each method were compared.

2. Operation Characteristics and Power Loss

The switching and conduction losses can be derived from the DC-link voltage (V_{dc}), output voltage (V_{xn}), and inductor current (i_{xL}). The operation period is divided into four areas, as shown in Fig. 1. In each area, the operation modes and the switching and conduction losses are analyzed.

2.1 2-level VSC

A 2-level VSC circuit is shown in Fig. 2 [14, 15]. In all areas, the switch S_{x_H} operates as the complementary switch to the S_{x_L} switch shown in Fig. 2. In areas 1 and 4, the switching loss in one switching cycle includes the turn-

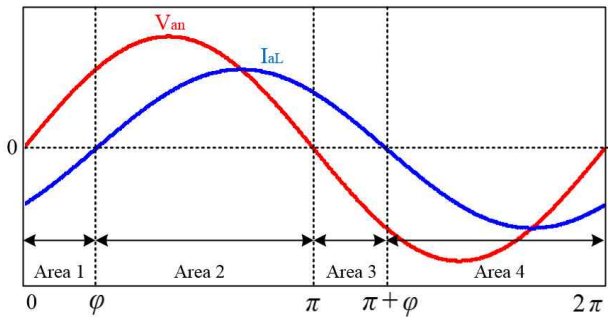

Fig. 1. Operation areas based on phase angle of output voltage and inductor current in A-phase

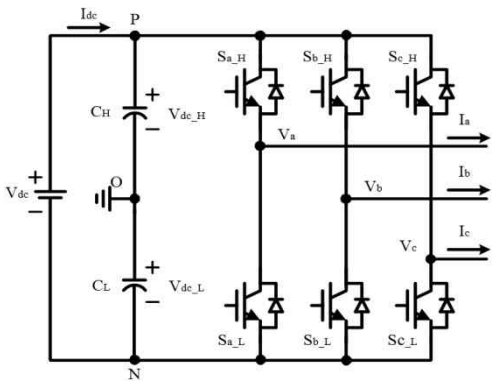

Fig. 2. 3-phase 2-level VSC circuit

on loss (P_{xon2}) and turn-off loss (P_{xoff2}) of S_{x_H}. A diode reverse-recovery loss (P_{xrr2}) of S_{x_L} also occurred. The switching losses can be expressed as:

$$P_{xon2} = \frac{V_{dc}}{V_{data}} A|i_{xL}| \quad (1)$$

$$P_{xoff2} = \frac{V_{dc}}{V_{data}} B|i_{xL}| \quad (2)$$

$$P_{xrr2} = \frac{V_{dc}}{V_{data}} C|i_{xL}| \quad (3)$$

where the inductor instantaneous current i_{xL} is:

$$i_{xL} = I_{xL} \sin(\omega t + \varphi) \quad (4)$$

where V_{dc} is the DC-link voltage and V_{data} is the reference switching voltage in the datasheet. The switching voltage in the 2-level VSC is the same as V_{dc}. A and B are the constants obtained from the insulated gate bipolar mode transistor (IGBT) switching energy losses as functions of the collector current, and C is the constant obtained from the diode reverse-recovery energy losses as a function of the collector current in the datasheet. In addition, φ is the phase delay between the output voltage V_{xn} and inductor current i_{xL}.

The diode conduction loss (P_{xd}) of the IGBT and the transistor conduction loss (P_{xtr}) of the IGBT are expressed as:

$$P_{xtr} = (V_{c0} + R_s |i_{xL}|)|i_{xL}| \quad (5)$$

$$P_{xd} = (V_{d0} + R_d |i_{xL}|)|i_{xL}| \quad (6)$$

where V_{tr0} and V_{d0} are the on-state saturation voltage between the collector and emitter of the IGBT when the IGBT is turned on but when no current exists. R_{tr} and R_d are the on-state resistances, which are obtained from the I_c-V_{ce} characteristics of the IGBT and antiparallel diode in the datasheet.

The conduction loss in one control period is changed depending on the duty ratio. In area 1, if S_{x_H} is in the on-state, the current i_{xL} flows through the diode of S_{x_H} and diode conduction loss occurred based on the turn-on ratio. Reverse- recovery energy loss occurred during switching times. The turn-on ratio of S_{x_H} is the duty ratio expressed as:

$$D_2 = \frac{1}{2} + \frac{|V_{xn} \sin(\omega t)|}{2V_{dc}} \quad (7)$$

Therefore, the turn-on ratio varies depending on the output voltage. When conduction losses are calculated, the turn-on ratio of each switch must be considered. When S_{a_H} is turned off and S_{a_L} is in the on-state, the current i_{aL} will flow through the transistor of S_{a_L}. During switching time,

Table 1. 2-level VSC switching and conduction losses

Area	Loss	Switches	Loss equation
1	P_{xsw2}	D_{a_H}, S_{a_L}	$P_{xrr2} + P_{xon2} + P_{xoff2}$
	P_{xcon2}	D_{a_H}, S_{a_L}	$D_2 P_{xd} + (1\text{-}D_2) P_{xtr} + (d/2)(P_{xd} - P_{xtr})$
2	P_{xsw2}	S_{a_H}, D_{a_L}	$P_{xon2} + P_{xoff2} + P_{xrr2}$
	P_{xcon2}	S_{a_H}, D_{a_L}	$D_2 P_{xtr} + (1\text{-}D_2) P_{xd} + (d/2)(P_{xd} - P_{xtr})$
3	P_{xsw2}	S_{a_H}, D_{a_L}	$P_{xon2} + P_{xoff2} + P_{xrr2}$
	P_{xcon2}	S_{a_H}, D_{a_L}	$(1\text{-}D_2) P_{xtr} + D_2 P_{xd} + (d/2)(P_{xd} - P_{xtr})$
4	P_{xsw2}	D_{a_H}, S_{a_L}	$P_{xrr2} + P_{xon2} + P_{xoff2}$
	P_{xcon2}	D_{a_H}, S_{a_L}	$(1\text{-}D_2) P_{xd} + D_2 P_{xtr} + (d/2)(P_{xd} - P_{xtr})$

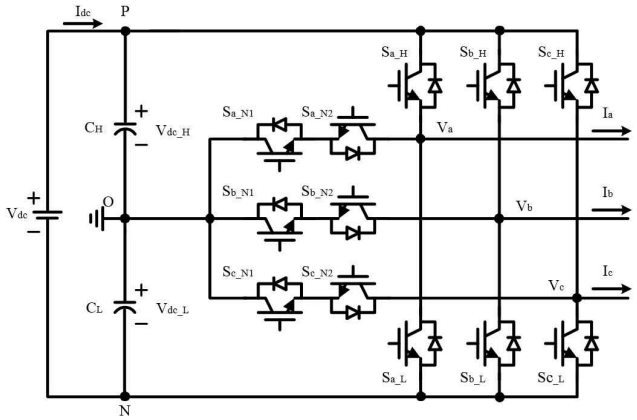

Fig. 3. 3LT VSC circuit

turn-on and turn-off losses (P_{xon2}, P_{xoff2}) occurred in S_{x_L}. The turn-on ratio of S_{a_L} will be $(1 - D_2)$.

The operating switches and loss equations for all areas are listed in Table 1.

In Table 1, P_{xsw2} denotes the switching loss and P_{xcon2} denotes the conduction loss of a 2-level VSC. P_{xsw2} employs the same equation for each area because the current flows through one IGBT transistor and one IGBT antiparallel diode. However, P_{xcon2} uses a different equation for each area because the conduction loss must consider the turn-on ratio. The 2-level VSC total loss is expressed as:

$$P_{x2} = P_{xsw2} + P_{xcon2} \tag{8}$$

2.2 3-level T-type VSC

The 3LT VSC is shown in Fig. 3. S_{x_H} and S_{x_N2}, as well as S_{x_N1} and S_{x_L}, perform complementary switching operations. In single cycle, the output voltage of the 3LT VSC ranges from zero to $V_{dc}/2$ or from - $V_{dc}/2$ to zero. Because of the decrease in the turn on/off voltage of the switch, the switching losses and harmonics are reduced. Therefore, the 3LT VSC IGBT turn-on and turn-off loss (P_{xon2}, P_{xoff2}), as well as the diode reverse recovery loss (P_{xrr3}), are expressed, respectively, as:

$$P_{xon3} = \frac{V_{dc}/2}{V_{data}} A\left|i_{xL}\right| \tag{9}$$

Table 2. 3LT VSC switching and conduction losses

Area	Loss	Switches	Loss equation
1	P_{xsw3}	D_{x_H}, S_{x_N2}	$P_{xrr3} + P_{xon3} + P_{xoff3}$
	P_{xcon3}	D_{x_H}, D_{x_N1}, S_{x_N2}	$D_3 P_{xd} + (1 - D_3) P_{xd} + (1\text{-}D_3) P_{xtr} + (d/2)(P_{xd} - P_{xtr})$
2	P_{xsw3}	S_{x_H}, D_{x_N2}	$P_{xon3} + P_{xoff3} + P_{xrr3}$
	P_{xcon3}	S_{x_H}, S_{x_N1}, D_{x_N2}	$D_3 P_{xtr} + (1 - D_3) P_{xtr} + (1\text{-}D_3) P_{xd} + (d/2)(P_{xd} - P_{xtr})$
3	P_{xsw3}	S_{x_N1}, D_{x_L}	$P_{xon3} + P_{xoff3} + P_{xrr3}$
	P_{xcon3}	S_{x_N1}, D_{x_N2}, D_{x_L}	$(1 - D_3) P_{xtr} + (1 - D_3) P_{xd} + D_3 P_{xd} + (d/2)(P_{xd} - P_{xtr})$
4	P_{xsw3}	D_{x_N1}, S_{x_L}	$P_{xrr3} + P_{xon3} + P_{xoff3}$
	P_{xcon3}	D_{x_N1}, S_{x_N2}, S_{x_L}	$(1 - D_3) P_{xd} + (1\text{-}D_3) P_{xtr} + D_3 P_{xtr} + (d/2)(P_{xd} - P_{xtr})$

$$P_{xoff3} = \frac{V_{dc}/2}{V_{data}} B\left|i_{xL}\right| \tag{10}$$

$$P_{xrr3} = \frac{V_{dc}/2}{V_{data}} C\left|i_{xL}\right| \tag{11}$$

where $V_{dc}/2$ is the same as the switching voltage of the 3LT VSC.

When the current flows through the neutral point of the IGBT (S_{x_N1}, S_{x_N2}), the conduction losses will increase to twice that of the 2-level VSC because both transistor and diode conduction losses occur. Therefore, if the turn-on ratio of the S_{x_N1} and S_{x_N2} is sufficiently high, the 3LT VSC conduction loss will be higher than that of the 2-level VSC.

The 3LT VSC operation is divided based on the areas shown in Fig. 1. In areas 1 and 3, S_{a_N1} is in the on-state and S_{a_L} is in the off-state, and S_{a_H} and S_{a_N2} perform a complementary switching operation. In area 1 and in the S_{a_H} on-state, the current flows through the S_{a_H} diode and diode conduction loss occurred. In addition, at S_{a_H} switching time, a diode reverse-recovery loss occurred. In the S_{a_L} on-state, the current flows through the S_{a_L} transistor. Thus, a transistor conduction loss occurred. During switching time, S_{x_L} turn-on and turn-off loss occurred. The duty ratio is expressed as:

$$D_3 = \frac{\left|V_{xn}\sin(\omega t)\right|}{V_{dc}/2} \tag{12}$$

In the Area 1, 2, The D_3 becomes the duty of D_{x_H} and in other area The D_3 becomes the duty of D_{x_L} [16]. The operating switches and loss equations for all areas are listed in Table 2. As shown in Table 2, the 3LT VSC switching loss (P_{xsw3}) employs the same equation for each area because the current flows through one IGBT transistor and one IGBT antiparallel diode. The 3LT VSC conduction loss (P_{xcon3}) is the sum of three terms because two switches are present in the neutral point. Conduction losses are different based on the turn-on ratio of each switch. The 3LT VSC total loss is expressed as:

$$P_{x3} = P_{xsw3} + P_{xcon3} \tag{13}$$

3. Proposed Method

A mode transition scheme between the 2-level and 3LT VSC is proposed for optimal efficiency. Loss calculation results of (8) and (12) are compared to determine whether an inverter immediately yields high efficiency. Parameters that influence loss calculation results are the duty ratio (DC-link voltage, output voltage) and the inductor current. The proposed method achieves high efficiency compared with the 2-level or 3LT VSC.

3.1 Proposed method sequence

Fig. 4 is a block diagram of the proposed method sequence. The sequence is performed during every cycle from 10 to 15 kHz. After the parameter values (V_{xn}, V_{dc}, and i_{xL}) are measured, the operation area is divided according to V_{xn} and i_{xL}. The switching and conduction losses (P_{xsw2}, P_{xcon2}, P_{xsw3}, and P_{xcon3}) are calculated based on the loss equations given in Table 1 and Table 2. Then, P_{x2} and P_{x3} are compared. If the P_{x3} is less than P_{x2}, the 3LT VSC operation mode selected; otherwise, the 2-level VSC operation mode is selected.

3.2 Simulation results

To verify the proposed method, a PSIM simulation was performed. The calculation and inverter operation were performed using a dynamic linking library (DLL) function.

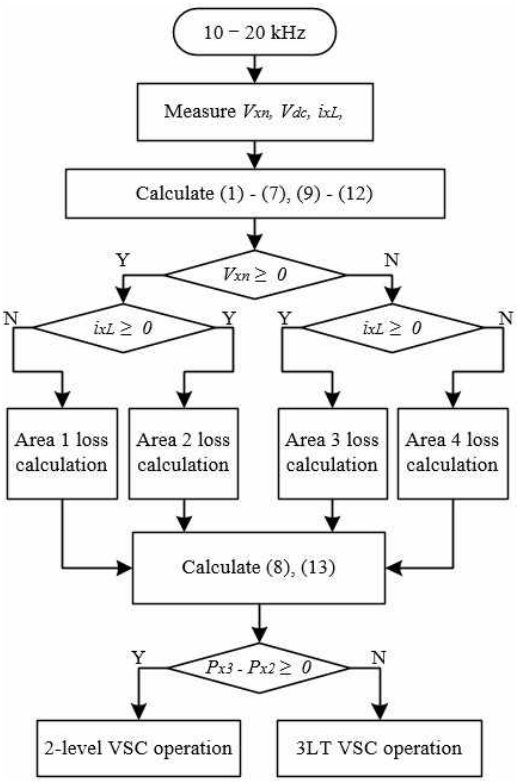

Fig. 4. Block diagram of proposed method sequence

The thermal module of the PSIM was used to confirm the results of the calculation. The parameters used in the simulation and experiment are shown in Table 3.

The PSIM simulation results are shown in Fig. 5. P_{x2} and P_{x3} are calculation results from (8) and (12). When (P_{x3} – P_{x2}) ≥ 0, the inverter operates as a 2-level VSC. When (P_{x3} – P_{x2}) < 0, the inverter operates as a 3LT VSC.

Fig. 6 shows the simulation results based on the conditions that DC-link voltage 700 V, output voltage 380 V, 6 kW resistor load. The proposed method achieved higher efficiency than did the individual operation methods.

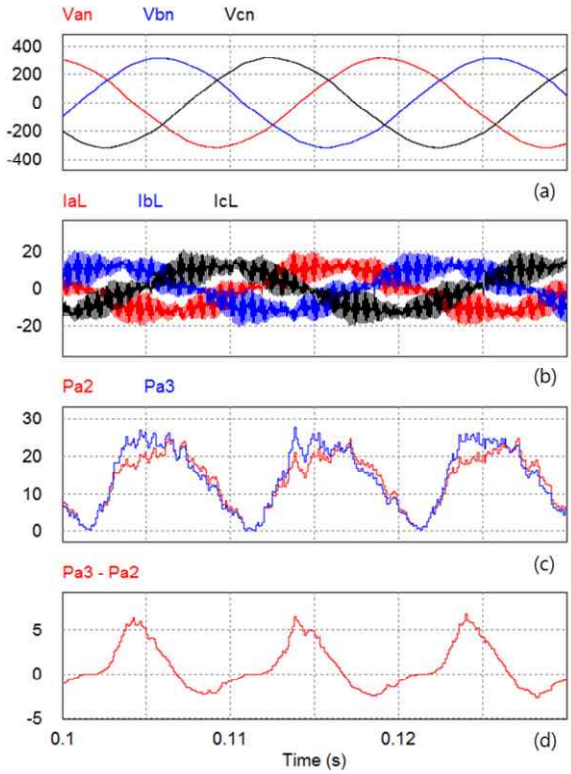

Fig. 5. Simulation waveform (f_s = 10 kHz, R_{load} = 48 Ω) : (a) output phase voltage V_{an}, V_{bn}, and V_{cn}, (b) inductor current i_{aL}, i_{bL}, and i_{cL}, (c) 2-level A-phase loss calculation P_{a2} and 3-level A-phase loss calculation P_{a3}, (d) P_{a3} - P_{a2}

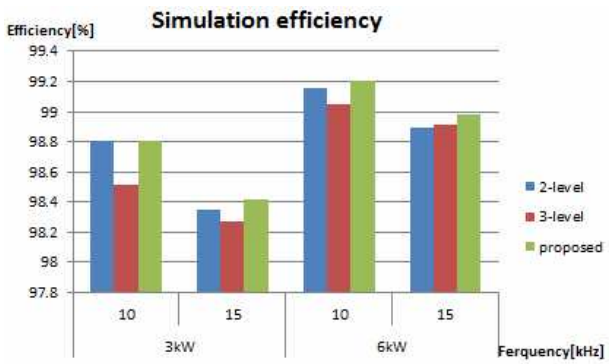

Fig. 6. Simulation efficiency with R load (3 kW, 6 kW)

The efficiency increased approximately 0.3% with the 10 kHz frequency and 1 kW resistor load.

4. Experimental results

Experimental conditions were the same as those listed in Table 3. To verify the proposed method the experiment was performed on some other conditions. First, the DC-link voltage is 700 V, output voltage is 380 V and R load.

Second, the DC-link voltage is 500 V, output voltage is 220 V and R load. Third, the DC-link voltage is 500 V, output voltage is 220 V and RL load that PF is 0.8. The prototype 3LT VSC consisted of a Vincotech 70-W212NMA300SC-M208P IGBT (1200V, 300A). A digital signal processor TMS320F28335 was used to implement the proposed control method.

4.1 Waveform comparison

Figs. 7 to 9 show experimental results. The DC-link voltage is 700 V, output voltage is 380 V. The control period was 10 kHz and the resistor load was 3 kW. Fig. 7 shows the 2-level VSC waveform. The inverter voltage fluctuation was equal to the DC-link voltage. In 2-level operating mode, the ripple current of the inductor is larger than in other operating modes. Fig. 8 shows the 3LT VSC waveform. The inverter voltage fluctuation was equal to half the DC-link voltage. In addition, Fig. 8 shows that the 3LT VSC current fluctuation was lower than that of the 2-level VSC. Fig. 9 shows the proposed method's operation waveform. The area marked with 2lv is 2-level operating area and 3lv is 3-level operating area. The operation area can be noticed by the inverter voltage waveform. An additional waveform, P_{a3}-P_{a2}, also exists. When (P_{a3}-P_{a2}) ≥ 0, the inverter operated as a 2-level VSC. When (P_{a3}-P_{a2}) < 0, the inverter operated as a 3LT VSC. Therefore, the 2-level VSC operation was performed at phase angles of approximately "0" and "π". Fig. 10 shows the experimental waveforms on condition of DC-link voltage 500 V, output voltage 220 V with 1 kW RL load. In conditions of 1 kW and 2 kW, the PF is close to 0.8.

Table 3. System parameter

Parameter	Value
DC-link voltage (V_{dc})	700, 500 [V]
Output voltage (V_{xl})	380, 220 [V]
Switching frequency (f_s)	10, 15 [kHz]
Resistor load (R_{load})	24, 48 [Ω]
Inductor load (L_{load})	48, 77 [mH]
Filter inductor (L_f)	1 [mH]
Filter capacitor (C_f)	100 [μF]

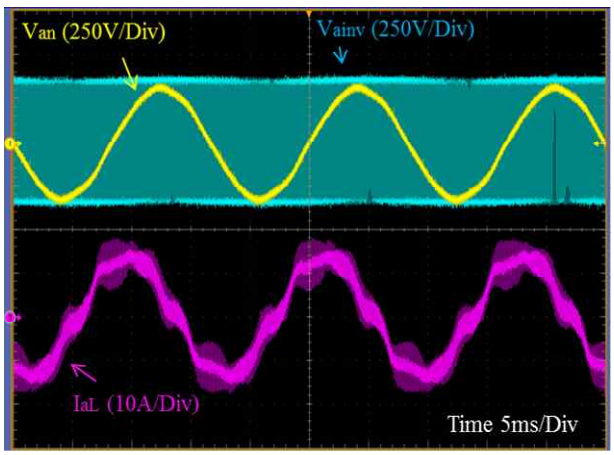

Fig. 7. 2-level operation mode waveform: Ch1 output voltage, V_{an} (250 V/div), Ch2 inverter voltage, V_{ainv} (250 V/div), Ch3 inductor current, i_{aL} (10 A/div)

4.1 Efficiency comparison

A HIOKI PW6001 power analyzer with a basic power

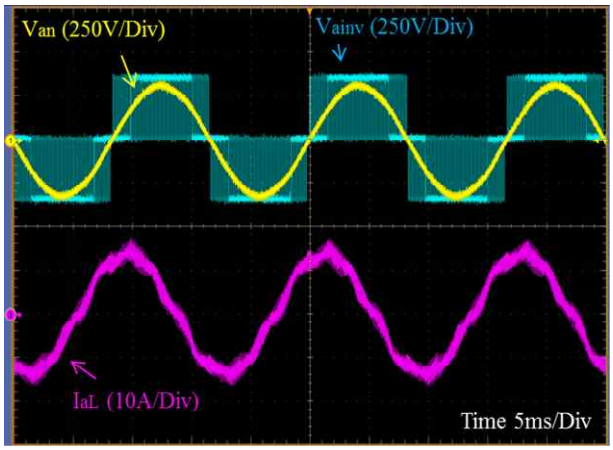

Fig. 8. 3-level operation mode waveform: Ch1 output voltage, V_{an} (250 V/div), Ch2 inverter voltage, V_{ainv} (250 V/div), Ch3 inductor current, i_{aL} (10 A/div)

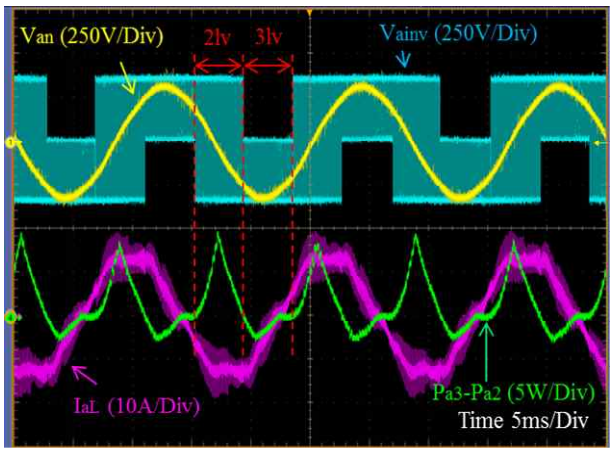

Fig. 9. Proposed method waveform: Ch1 output voltage, V_{an} (250 V/div), Ch2 inverter voltage, V_{ainv} (250 V/div), Ch3 inductor current, i_{aL} (10 A/div), Ch4 $P_{a3} - P_{a2}$ value (5 W/div)

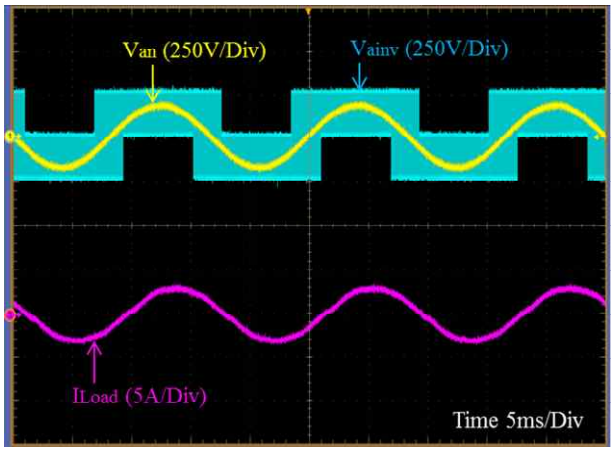

Fig. 10. Proposed method waveform with RL load: Ch1 output voltage, V_{an} (250 V/div), Ch2 inverter voltage, V_{ainv} (250 V/div), Ch3 load current, i_{Load} (10 A/div)

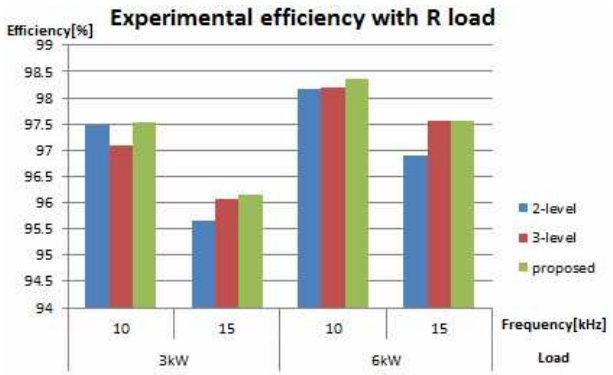

Fig. 11. Experiment efficiency with R load (3 kW, 6 kW)

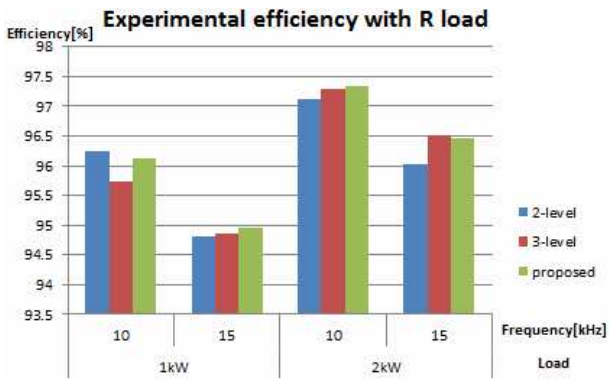

Fig. 12. Experiment efficiency with R load (1 kW, 2 kW)

accuracy of 0.02 % was used to measure the efficiency. Fig. 11 shows the experimental results on the first conditions as mentioned before same with Figs.7-9. Fig. 12 shows the experimental results on the second conditions. Comparing the 2-level and 3-level operating mode in terms of efficiency, the 3-level operation mode is more effective than the 2-level as the capacity and frequency increase.

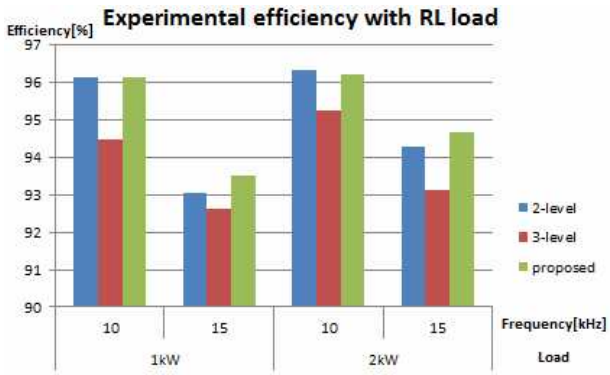

Fig. 13. Experiment efficiency with RL load (1 kW, 2 kW)

Because the switching losses are increased as the switching voltage and frequency are increase. Fig. 13 shows the experimental results on the conditions same with Fig. 10. It can be seen that the efficiency of each operation mode can be different depending on the phase on same condition. In Fig. 13, efficiency of 2-level is greater than 3-level.

The efficiency of proposed method is almost same or higher with an operation mode that has better efficiency. On condition of a 15 kHz frequency and a 2 kW RL load the efficiency was increased approximately 1.53 % than the 3-level, and 0.37 % than 2-level. On condition of a 15 kHz frequency and a 1 kW RL load the efficiency of proposed method was increased 0.91 % than 3-level and 0.46 % than 2-level. In these two cases the efficiency of 2, 3-level are worst but the increase rate of proposed method efficiency is best.

5. Conclusion

The 3LT VSC had the advantage of low switching loss because the switching voltage was the half the DC-link voltage. 3LT VSC has a disadvantage of large conduction loss due to two neutral switches. At a low output voltage, the 2-level mode is more advantageous in terms of efficiency than that of the 3-level mode. In this study, a mode transition scheme between a 2-level and a 3-level operation mode was proposed for optimal efficiency for 3LT VSC. In each control period, the proposed method performs calculation of losses and selects a better operation mode. The proposed mode transition scheme is more efficient when operating only in 3-level or 2-level under most conditions.

Acknowledgements

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