J Electr Eng Technol.2018; 13(1): 168-180
http://doi.org/10.5370/JEET.2018.13.1.168

ISSN(Print) 1975-0102
ISSN(Online) 2093-7423

An Adaptive Complementary Sliding-mode Control Strategy of Single-phase Voltage Source Inverters

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Abstract – In order to achieve the high quality output voltage of single-phase voltage source inverters, in this paper an Adaptive Complementary Sliding Mode Control (ACSMC) is proposed. Firstly, the dynamics model of the single-phase inverter with lumped uncertainty including parameter variations and external disturbances is derived. Then, the conventional Sliding Mode Control (SMC) and Complementary Sliding Mode Control (CSMC) are introduced separately. However, when system parameters vary or external disturbance occurs, the controlling performance such as tracking error, response speed et al. always could not satisfy the requirements based on the SMC and CSMC methods. Consequently, an ACSMC is developed. The ACSMC is composed of a CSMC term, a compensating control term and a filter parameters estimator. The compensating control term is applied to compensate for the system uncertainties, the filter parameters estimator is used for on-line *LC* parameter estimation by the proposed adaptive law. The adaptive law is derived using the Lyapunov theorem to guarantee the closed-loop stability. In order to decrease the control system cost, an inductor current estimator is developed. Finally, the effectiveness of the proposed controller is validated through Matlab/Simulink and experiments on a prototype single-phase inverter test bed with a TMS320LF28335 DSP. The simulation and experimental results show that compared to the conventional SMC and CSMC, the proposed ACSMC control strategy achieves more excellent performance such as fast transient response, small steady-state error, and low total harmonic distortion no matter under load step change, nonlinear load with inductor parameter variation or external disturbance.

Keywords: Adaptive complementary sliding-mode control, Single-phase voltage source inverter, Voltage control, Inductor current estimator

1. Introduction

In the last few decades, the use of voltage inverters has gained an increased presence in a wide range of applications such as Uninterruptible Power Supply (UPS), communication systems, medical equipment and data processing systems [1-3]. Characterized by switching, voltage inverters are inherently switching nonlinear systems. Conventional control approaches based on linear control techniques are found to be incapable of achieving the necessary regulation, dynamic response, and stability requirements needed for voltage inverters. In recent years, various control methods, such as deadbeat control, repetitive control, proportional-resonant control, adaptive control, feedback linearization control, sliding mode control etc., have been applied to inverter systems, and their feasibility has been studied [4-22]. However, these control methods still have more or less defects. Repetitive control meets the problems of slow dynamics, large memory requirement and poor performance to non-periodic disturbances. The Proportional- Resonant (PR) control gain is extremely small at the non-resonant frequency. In [23], a new sliding mode control scheme based on rotating sliding line has been proposed to improve dynamic response; its main defect is that the tracking errors still cannot converge to zero in finite time. In [24, 25] the sgn function is replaced by the saturation function to reduce the chattering of output voltage. However, the variable switching frequency operation problem still exists, and that makes it difficult to accurately design output filter parameters. Consequently, a fixed switching frequency sliding-mode control is widely applied in the field of inverter [26-29]. In [26], voltage feed-forward control method is applied to reduce steady-state error of the output voltage and the time of reaching sliding surface. In [27, 28], a PID sliding mode surface and an improved PID sliding mode surface is used to reduce steady-state error. In [29], an integral compensation term is added to terminal sliding mode control, which can reduce inverter steady-state error in certain degree.

In [30-32], a complementary sliding mode control method (CSMC) is proposed. Compared with the traditional sliding mode control in the above paper, the CSMC not only alleviates the chattering phenomena but

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Received: October 23, 2016; Accepted: August 23, 2017

also reduces steady-state error at least by 50%. The transient response of the tracking error during the reaching phase also can be improved greatly by two perpendicular sliding surfaces. Therefore, the CSMC has been widely used in many fields, such as atomic force microscopy, dual linear motor servo system, PMSM drive system, etc [33-35].

In this paper, the CSMC method is firstly applied to control the output voltage of a single-phase inverter for tracking voltage reference signal. However, like SMC, in practical applications, the exactly bound of the uncertainty is still hard to get in advance. Therefore, an Adaptive Complimentary Sliding Mode (ACSMC) is proposed for the inverter system. In the ACSMC, the *LC* parameters adaptive law is applied to estimate the uncertainty online and the estimated laws are derived from the Lyapunov theorem. Considering that the load current is unknown and inductor current avoiding over-current faults must be known, an inductor current estimator is adopted. Meanwhile, the global stability of the control system is proved by the Lyapunov stability theory. Simulations and experiments are implemented to investigate the effective-ness of the proposed control scheme.

The remaining part of this paper is organized as follows: Section 2 describes the model of the single-phase inverter. The design of the SMC and the CSMC controller are fully addressed in Section 3 and Section 4, respectively. Section 5 addresses the ACSMC, analyzes its stability, and gives an inductor current estimator. In Section 6, the simulation and experimental results are given to evaluate the performance of the control algorithm. Finally, conclusions are drawn in Section 7.

2. Modeling of the Inverter

The single-phase voltage source inverter with an *LC* filter is shown in Fig. 1, which is composed of a DC-link voltage(V_{dc}), a single-phase pulse width modulation (PWM) inverter (Q_1～Q_4), an output *LC* filter (*L* and *C*), a single-phase load R_L (e.g., linear or nonlinear load). Based on Fig. 1, the dynamic model for the inverter can be written as

$$K_m \ddot{X}_e = -X_e + u - L\frac{di_o}{dt} \tag{1}$$

where $X_e=u_o$, $K_m=LC$, $u=V_{dc}d$, d is control input duty ratio, $-1\le d\le 1$.

Defining the state variable $E=X_e-X_d$, where X_d is the reference for the output voltage and $X_d=V_m\sin(2\pi ft)$, so the Eq. (1) can be transformed to

$$K_m \ddot{E} = -X_e + u + W_c \tag{2}$$

where W_c is the disturbance term and defined as

$$W_c = -L\frac{di_o}{dt} - K_m \ddot{X}_d \tag{3}$$

3. Conventional Sliding Mode Control

Let us define a linear sliding surface as

$$S_{\mathrm{SMC}} = \dot{E} + \Lambda E, \quad \Lambda > 0 \tag{4}$$

where Λ is a positive quantity. Here, the reaching law is selected as

$$\dot{S}_{\mathrm{SMC}} = -\eta \,\mathrm{sgn}(S_{\mathrm{SMC}}), \quad \eta > 0 \tag{5}$$

where η is a positive value. If the disturbance term W_c is not considered, from (4) and (5), we can get

$$u_{\mathrm{SMC}} = X_e - \Lambda \hat{K}_m \dot{E} - \eta \,\mathrm{sgn}(S_{\mathrm{SMC}}) \tag{6}$$

where $\hat{K}_m$ is estimation of K_m. In order to alleviate the chattering caused by $\mathrm{sgn}(S_{\mathrm{SMC}})$, here a saturation function $sat(\cdot)$ is adopted to replace sgn function [36].

$$sat(\frac{\xi}{\Phi}) = \begin{cases} 1, \xi > \Phi \\ \dfrac{\xi}{\Phi}, |\xi| \le \Phi \\ -1, \xi < -\Phi \end{cases} \tag{7}$$

where Φ is a positive value, and named the boundary layer. So, the Eq. (6) can be rewritten as

$$u_{\mathrm{SMC}} = X_e - \Lambda \hat{K}_m \dot{E} - \eta\, sat(S_{\mathrm{SMC}}) \tag{8}$$

If $|S_{\mathrm{SMC}}| > \Phi$, we can get

$$K_m \dot{S}_{\mathrm{SMC}} S_{\mathrm{SMC}} = -\eta S_{\mathrm{SMC}} \mathrm{sgn}(S_{\mathrm{SMC}}) + S_{\mathrm{SMC}}(W_c + W_d) \tag{9}$$

where

$$W_d = (K_m - \hat{K}_m)\Lambda \dot{E} \tag{10}$$

and

$$|W_c + W_d| \le |W_c| + |W_d| \tag{11}$$

From (3), the following inequalities can be obtained

$$|W_c| \le L\left|\frac{di_o}{dt}\right| + K_m V_m \omega^2 \tag{12}$$

In accordance with the inverter characteristic, the capacitance, inductance, and instantaneous load current is bounded in a switching period. So, we can assume that $|W_c|$

$|W_d|$ are bounded and satisfy the follow inequality

$$|W_c|+|W_d|\le K_1 \tag{13}$$

where K_1 is the upper bound on (13).

Consequently, we get

$$K_m\dot{S}_{\mathrm{SMC}}S_{\mathrm{SMC}} \le |S_{\mathrm{SMC}}|(K_1-\eta) \tag{14}$$

From (14), the condition for quasi-sliding mode to exist is that $\eta > K_1$. When the system state stays inside the boundary layer, the tracking error meets [36]

$$|E|\le\frac{\Phi}{\Lambda} \tag{15}$$

4. Complementary Sliding Mode Control

In order to satisfy the design requirement in the CSMC, the generalized-sliding surface is defined as follows

$$S_e=\dot{E}+2\Lambda\mathrm{E}+\Lambda^2\int_0^t E(\tau)d\tau \tag{16}$$

Next, a second sliding surface named complementary sliding surface is designed as follows

$$S_{ce}=\dot{E}-\Lambda^2\int_0^t E(\tau)d\tau \tag{17}$$

From (16) and (17), we get

$$\dot{S}_{ce}+\Lambda(S_e+S_{ce})=\dot{S}_e \tag{18}$$

Consider the following Lyapunov function

$$V=\frac{1}{2}K_m(S_e^2+S_{ce}^2) \tag{19}$$

From (16) to (19), the time derivative of V is given by

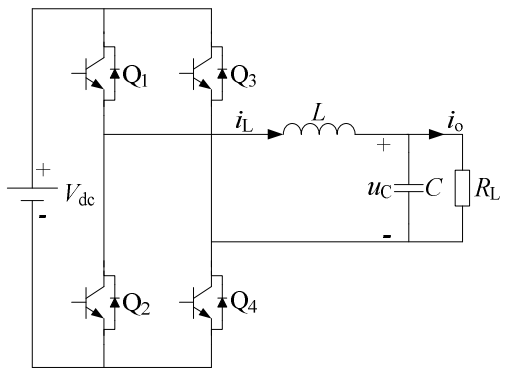


Fig. 1. Circuit diagram of single-phase voltage source full-bridge inverter

the following

$$\begin{aligned}\dot{V}&=K_m(S_e\dot{S}_e+S_{ce}\dot{S}_{ce})\\&=-\Lambda K_m(S_e+S_{ce})^2+(S_e+S_{ce})(K_m\dot{S}_e+\Lambda K_mS_e)\end{aligned} \tag{20}$$

Then, the complementary sliding mode controller can be designed by the following equation

$$\begin{aligned}u_{\mathrm{CSMC}}=X_e&-3\Lambda\hat{K}_m\dot{E}-3\hat{K}_m\Lambda^2E-\hat{K}_m\Lambda^3\int_0^t E(\tau)d\tau\\&-\varepsilon sat(S_e+S_{ce})\end{aligned} \tag{21}$$

When $|S_e+S_{ce}|>\Phi$, Substituting (21) into (20), (21) becomes

$$\dot{V}=-\Lambda K_m(S_e+S_{ce})^2-\varepsilon|S_e+S_{ce}|+(S_e+S_{ce})(W_c+W_{d2}) \tag{22}$$

where

$$W_{d2}=(K_m-\hat{K}_m)(3\Lambda\dot{E}+3\Lambda^2E+\Lambda^3\int_0^t E(\tau)d\tau) \tag{23}$$

As similar with the SMC, W_c+W_{d2} is bounded and satisfy the follow inequality

$$|W_c|+|W_{d2}|\le K_2 \tag{24}$$

So, (24) becomes

$$\dot{V}\le|S_e+S_{ce}|(K_2-\varepsilon) \tag{25}$$

From (25), the condition for quasi-sliding mode to exist is that $\varepsilon > K_2$. From (16) and (17), we can get

$$\frac{S_e+S_{ce}}{2}=\dot{E}+\Lambda\mathrm{E} \tag{26}$$

When the system state keeps inside the boundary layer the tracking error will meet [36]

$$|E|\le\frac{\Phi}{2\Lambda}\ \text{ And }\ |\dot{E}|\le\Phi \tag{27}$$

Comparing with the SMC, it can be known that the CSMC can reduce half of the tracking error with faster approaching speed. From the above mentioned theoretical analysis, it can be easily seen that the CSMC has lower tracking error and faster approaching speed than the SMC, but the switching gain is same as the SMC, namely $\varepsilon > K_2$. The Eq. (6) and Eq. (21) show that the upper bound η and ε have a significant effect on the control performance. However, W_c and $\hat{K}_m$ contain the uncertainties

including load current disturbance and inductance variations. Since $\hat{K}_m$ is difficult to measure and load current of W_c must be measured through current sensor in advance in practical applications. Though the value of the upper bound can be selected by the trial and error methods to reach the requirement of convergence of tracking error in the CSMC, this method has the shortcoming of time consuming and cannot provide enough robustness in practical applications. Therefore, an ACSMC is developed in the following sections to alleviate the aforementioned drawbacks.

5. Adaptive Complementary Sliding Mode Control

5.1 Adaptive complementary sliding mode control

To improve the control performance of the inverter system for the tracking of periodic-reference trajectories and high performance applications, the ACSMC is developed. The ACSMC mainly includes three parts: a CSMC control term, an estimator of $\hat{K}_m$ term, and a feed-forward term of $\hat{W}_c$. Firstly, the overall system control law is designed as follows

$$u_{\mathrm{ACSMC}} = X_e - 3\Lambda\hat{K}_m\dot{E} - 3\hat{K}_m\Lambda^2 E - \hat{K}_m\Lambda^3\int_0^t E(\tau)d\tau - \varphi sat(S_e + S_{ce})) - \hat{W}_c \tag{28}$$

where φ is a positive value.

Secondly, the adaptive learning algorithm is designed as follows

$$\dot{\hat{K}}_m = \gamma_1(S_e + S_{ce})(3\Lambda\dot{E} + 3\Lambda^2 E + \Lambda^3\int_0^t E(\tau)d\tau) \tag{29}$$

The feed-forward term $\hat{W}_c$ can be designed as

$$\hat{W}_c = -L\frac{di_L}{dt} - \hat{K}_m\ddot{X}_d \tag{30}$$

Choose the following Lyapunov function

$$V_2(t) = \frac{1}{2}K_m(S_e^2 + S_{ce}^2) + \frac{1}{2\gamma_1}\tilde{K}_m^2 \tag{31}$$

where $\tilde{K}_m = K_m - \hat{K}_m$ is defined as observational errors of K_m. Consider that K_m changes slowly, then the time derivative of V can be derived as

$$\begin{aligned}\dot{V}_2(t) = &-K_m\Lambda(S_e + S_{ce})^2 + \tilde{K}_m((3\Lambda\hat{K}_m\dot{E} + 3\hat{K}_m\Lambda^2 E \\ &+\hat{K}_m\Lambda^3\int_0^t E(\tau)d\tau)(S_e + S_{ce}) - \frac{1}{\gamma_1}\dot{\hat{K}}_m) \\ &+(S_e + S_{ce})(W_c - \hat{W}_c - \varphi sat(S_e + S_{ce}))\end{aligned} \tag{32}$$

Substituting (28), (29) and (30) into (32), then

$$\begin{aligned}\dot{V}_2(t) = &-K_m\Lambda(S_e + S_{ce})^2 + (S_e + S_{ce}) \\ &(LC\frac{d^2u_o}{dt^2} - \tilde{K}_m\ddot{X}_d - \varphi sat(S_e + S_{ce}))\end{aligned} \tag{33}$$

When $|S_e + S_{ce}| > \Phi$, the following result can be obtained

$$\dot{V}_2(t) \le |S_e + S_{ce}|(\left|LC\frac{d^2u_o}{dt^2}\right| + |\tilde{K}_m\ddot{X}_d| - \varphi) \tag{34}$$

If

$$\left|LC\frac{d^2u_o}{dt^2}\right| + |\tilde{K}_m\ddot{X}_d| \le \varphi \tag{35}$$

Then

$$\dot{V}_2(t) \le -|S_e + S_{ce}|(\varphi - \left|LC\frac{d^2u_o}{dt^2}\right| - |\tilde{K}_m\ddot{X}_d|) \le 0 \tag{36}$$

Since $V_2(t)$ is a negative semi-definite function, i.e., $V_2(t) \le V_2(0)$. It implies that S_e, S_{ce} and $\tilde{K}_m$ are bounded functions. Define the function

$$M(t) = |S_e + S_{ce}|(\varphi - \left|LC\frac{d^2u_o}{dt^2}\right| - |\tilde{K}_m\ddot{X}_d|) \ge 0 \tag{37}$$

and the integrate function $M(t)$ with respect to time

$$\int_0^t M(\tau)d\tau \le V_2(0) - V_2(t) \tag{38}$$

Because V_2 (0) is a bounded function and V_2 (t) is a non-increasing and bounded function, we can get

$$\lim_{t\to\infty}\int_0^t M(\tau)d\tau < \infty \tag{39}$$

The V_2 (t) is bounded, by the Barbalat's lemma, it can be shown that $\lim_{t\to\infty} M(t) = 0$. It can imply that S_e and S_{ce} will converge to zero as $t\to\infty$. Moreover, $\tilde{K}_m$ can be guaranteed to be bounded. As a result, the stable behavior for the inverter can be ensured. In above analysis, the load current i_o in Eq.(3) is replaced by the inductor current i_L in Eq.(25), the reason is that it will require additional current sensor to measure load current if adopting Eq.(3) and the inductor current i_L must be known for avoiding over-current faults in practice. In order to reduce the hardware cost, the inductor current i_L is obtained by the inductor current estimator introduced later in this paper. If $\hat{W}_c$ in Eq. (32) is substituted by the Eq. (3), the Eq. (33) will become

$$\dot{V}_2(t) = -K_m \Lambda (S_e + S_{ce})^2 + +(S_e + S_{ce}) \\ (-\tilde{K}_m \ddot{X}_d - \varphi sat(S_e + S_{ce})) \quad (40)$$

The Eq.(35) will also become

$$\left| \tilde{K}_m \ddot{X}_d \right| \le \varphi \quad (41)$$

Comparing with Eq.(41), the switching gain φ in Eq.(35) will be increased. However, for high frequency harmonics of the output voltage filtering requirements, L and C are usually designed as mH and μF, respectively. So, LC and $\tilde{K}_m$ are very small. According to (35), the switching gain φ can still be selected as smaller than SMC or CSMC, it means that ACSMC can further reduce the chattering. Hence, in Eq.(5) using the inductor current i_L instead of the load current i_o won't influence control effect. Meanwhile, the ACSMC has the same advantages properties such as half of the tracking error, fast dynamic response speed. The block diagram of the ACSMC control scheme is shown in Fig. 2. Here, the Eq. (18) and the Eq. (19) are used to calculate S_e and S_{ce}; the Eq. (29) and the Eq. (30) are used to calculate $\hat{K}_m$ and $\hat{W}_c$; the controlling signal of u_{ACSMC} is calculated by the Eq. (28).

5.2 Inductor current estimator

In this paper, an inductor current estimator is adopted. As shown in Fig. 1, we can get

$$L \frac{\mathrm{d}i_L}{\mathrm{d}t} = V_{dc} S - u_o \quad (42)$$

where, if Q_1, Q_4 are turned ON and Q_2, Q_3 are turned OFF, S=1, else S= -1.As shown in Eq. (40), the inductor current derivative $\mathrm{d}i_L/\mathrm{d}t$ is based on V_{dc}, S, and u_o, that means that the inductor current derivative $\mathrm{d}i_L/\mathrm{d}t$ can be estimated by the Eq. (42). If a high sampling frequency is considered, the inductor current derivative $\mathrm{d}i_L/\mathrm{d}t$ is replaced by a forward Euler approximation. That is to say, the derivative $\mathrm{d}i_L/\mathrm{d}t$ can be approximated as follows

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} \approx \frac{i_L(k) - i_L(k-1)}{T_s} \quad (43)$$

where T_s is the sampling period. From (42) and (43), we can get [37]

$$\begin{cases} i_L(k) = \dfrac{T_s}{L}(V_{dc} S(k) - u_o(k)) + i_L(k-1) \\ L \dfrac{\mathrm{d}i_L(k)}{\mathrm{d}t} \approx V_{dc} S(k) - u_o(k) \end{cases} \quad (44)$$

If the DC source voltage V_{dc} changes are very small, from (44) we can know that the inductor current is related with the switching status S, output voltage u_o. Thus, based on the discretized result in (44), the inductor current and the differentiation of inductor current can be estimated.

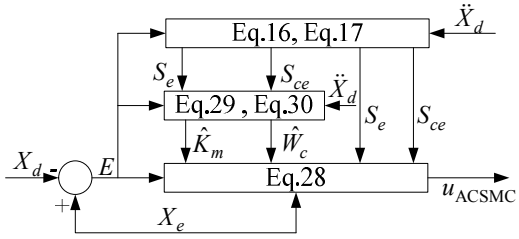


Fig. 2. Block diagram of the ACSMC control scheme

6. Simulation and Experimental Results

In this section, simulations and experiments are made, and various results are presented. To evaluate the effectiveness and feasibility of the ACSMC of inverters, comparative simulations and experiments between SMC, CSMC, and ACSMC are investigated. Simulations are carried out by MATLAB, and the system nominal parameters are given in Table 1.

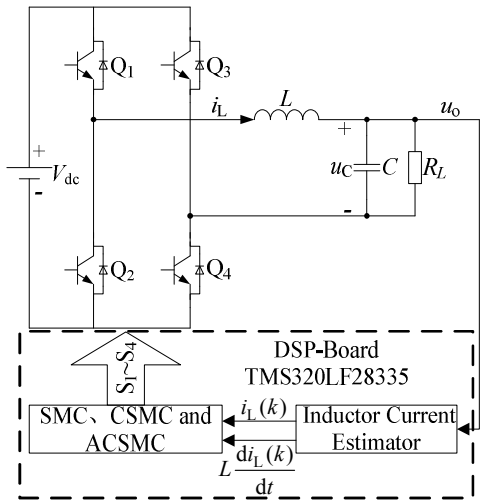
Fig. 3(a) illustrates the block diagram of a single-phase PWM inverter with an LC output filter, whereas Fig. 3(b) shows the photograph of the experimental setup employed to carry out the three control strategies. In the test bed, the current is measured by LA55-P current sensors; the voltage is measured by LV25-P voltage sensors. The sensed signals are then applied to the TMS320LF28335 DSP through its analog-to-digital converter. The proposed algorithm is verified through the resistive load, resistor inductance load and the nonlinear load with a diode rectifier. The nonlinear load circuit and the resistive-inductive load are shown in Fig. 4. Note that during simulation and the experiment, the

Table 1. System parameters of the inverter

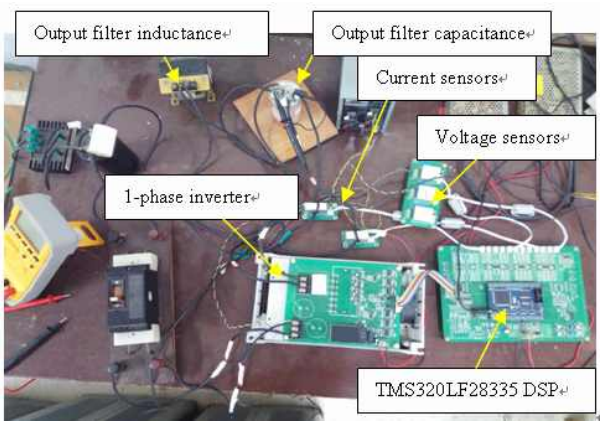
		Descriptions	Values
System Parameters	V_{dc}	dc-link voltage	150V
	f_s	Sampling frequency	18kHz
	f_{sw}	Switching frequency	18kHz
	f	Fundamental frequency	50Hz
	X_d	Reference Output voltage	$100\sin(2\pi ft)$
	L	Output filter inductance	6mH
	C	Output filter capacitance	20μF

Table 2. Control parameters

Descriptions	Values
Λ	2300
Φ	10000
η	9.5
ε	9.5
γ_1	2.3
φ	0.5



(a) Block diagram



(b) Experimental setup

Fig. 3. Single-phase PWM inverter with an *LC* output filter

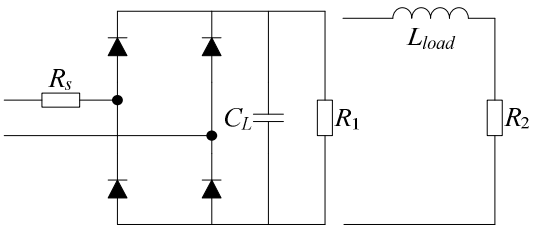
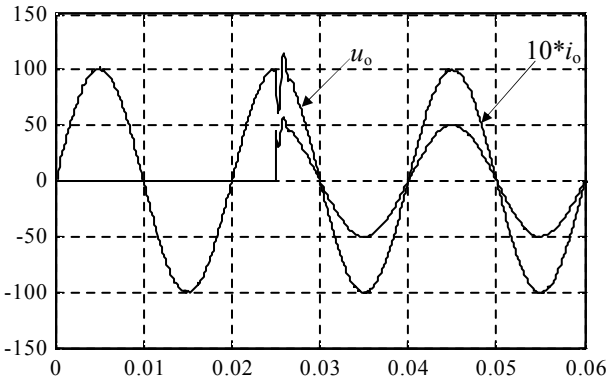


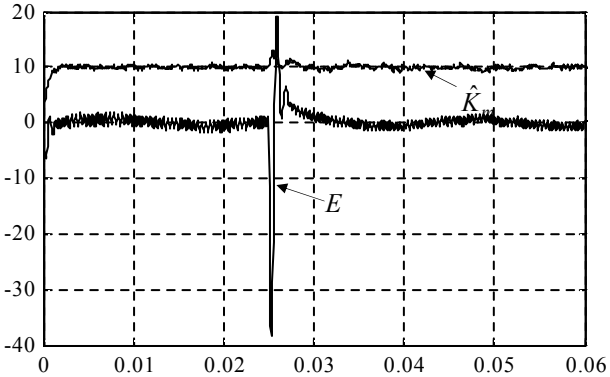
Fig. 4. Nonlinear load circuit with a diode rectifier and resistive-inductive load circuit (R_s=6.2Ω, C_L=220 μF, R_1=25Ω, R_2=19Ω and L_{load}=20mH)

control parameters are selected as Table 2.

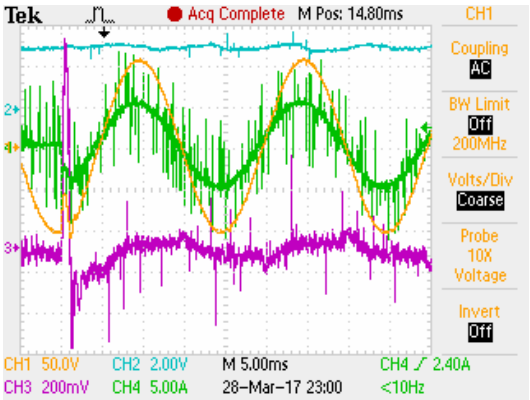
In practical applications, the filter inductance *L* has some uncertainties due to its nonlinear magnetic properties and the most common tolerance variation is within 10% [38, 39]. To further justify the system robustness under parameter variations, a ±16.67% reduction in *L* is assumed under all load conditions such as load step change, resistive-inductive load and nonlinear load. The load step change is carried out to verify the transient responses; On



(a) Load output voltages and Load output currents



(b) Load voltage error and $\hat{K}_m$ (*E*: 5.0V/div, $\hat{K}_m$:10^{-8}/div and 0.01s/div)

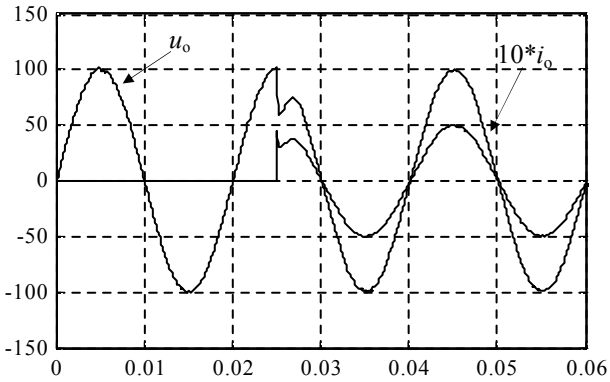


(c) Experimental results of ACSMC

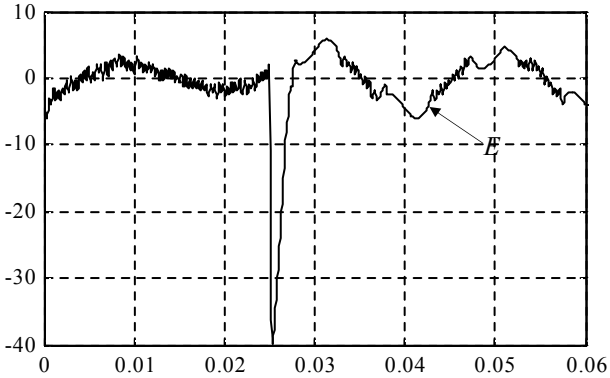
Fig. 5. Simulation and experimental results of the ACSMC scheme under load step change with −16.67% variations in *L*: (a) and (b) Simulation. (c) Experiment. (Ch1: u_o (50V/div), Ch2: $\hat{K}_m$ (0.67×10^{-7}/div), Ch3:*E* (5.0V/div) and Ch4:i_o (5A/div))

the other hand the resistive-inductive load and nonlinear load are carried out to verify the steady-state responses.

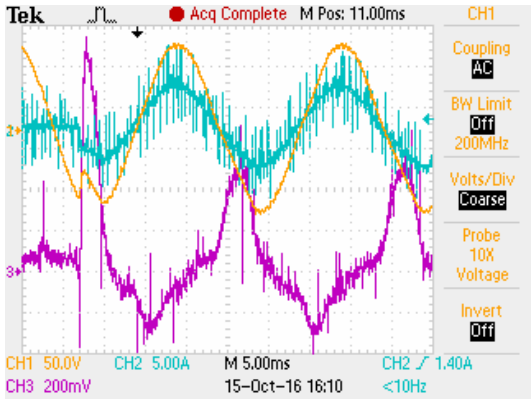
Fig. 5 shows the simulation and experimental results of the proposed ACSMC during the load step change. Fig. 6 and Fig. 7 present the comparative results obtained by employing the SMC and the CSMC and the CSMC under



(a) Load output voltages and Load output currents

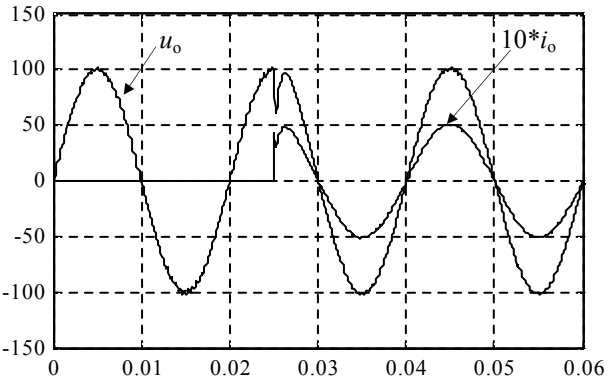


(b) Load voltage error E

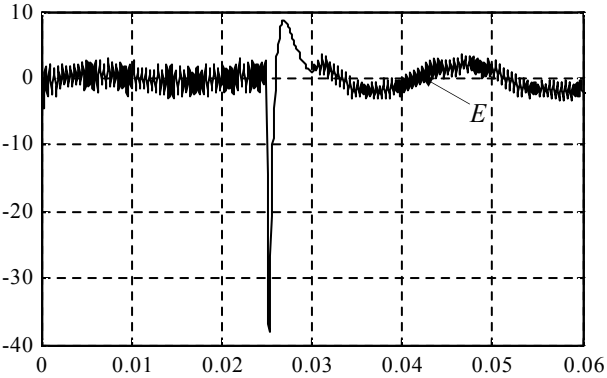


(c) Experimental results of SMC

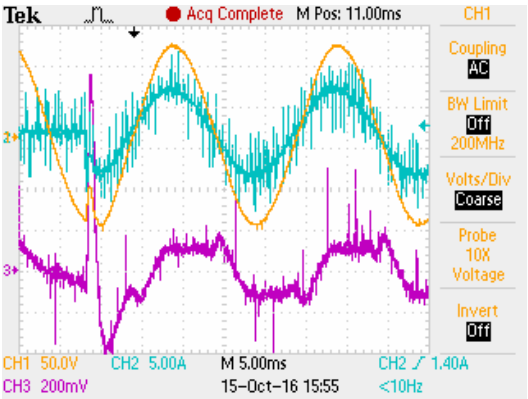
Fig. 6. Simulation and experimental results of the SMC scheme under load step change with −16.67% variations in L. (a) and (b) Simulation. (c) Experiment. (Ch1: u_o(50V/div), Ch2:i_o (5A/div) and Ch3: E(5.0V/div))



(a) Load output voltages and Load output currents



(b) Load voltage error E (E: 5.0V/div, and 20ms/div)



(c) Experimental results of CSMC

Fig. 7. Simulation and experimental results of the CSMC scheme under load step change with −16.67% variations in L. (a) and (b) Simulation. (c) and (d) Experiment. (Ch1: u_o(50V/div),Ch2:i_o (5A/div) and Ch3:E (5.0V/div))

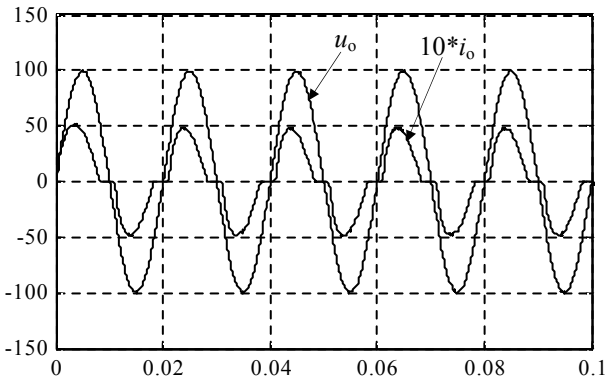
the same condition, respectively.

From Fig. 5(a), we can know that when the load is suddenly changed, the output voltage presents little distortion and returns to a steady-state condition in 1.9ms. At the same time, it has revealed a recovery time of 1.2 ms in a real experimental setup as shown in Fig. 5(c). Conversely, as shown in the simulation results in Fig. 6(a) and Fig. 7(a), the voltage tracking error E is larger, and its recovery times are 3.0ms and 2.2ms respectively. Moreover, Fig. 6(c) and Fig. 7(c) show a longer recovery time of 2.9ms and 1.9ms than that observed in Fig. 5(c). From Fig. 5, Fig. 6 and Fig. 7, we can know that tracking error of the ACSMC is smallest and the CSMC is about half of the SMC.

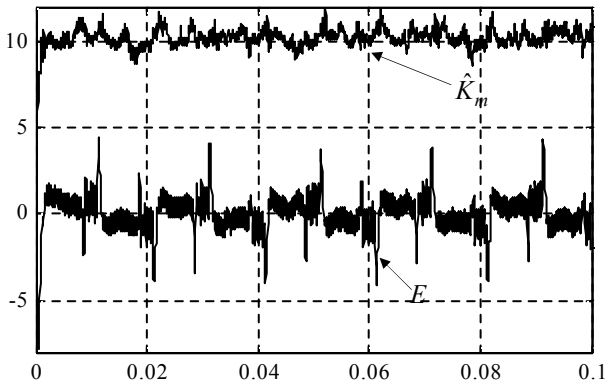
Meanwhile, when the filter inductance L is 5mH, 6mH and 7mH respectively, the THD values of the load output

Table 3. The simulated and measured THD(%) of output voltage for the resistive load case (R_L=20Ω)

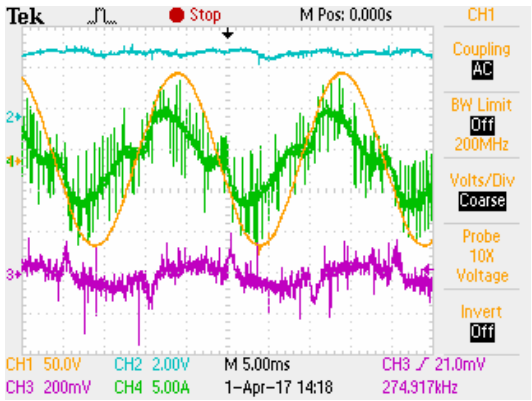
Parameters L	SMC		CSMC		ACSMC	
	Sim.	Exp.	Sim.	Exp.	Sim.	Exp.
5mH	3.57%	4.2%	2.31%	2.87%	0.64%	0.68%
6mH	2.38%	2.65%	1.16%	1.83%	0.42%	0.81%
7mH	4.91%	5.23%	2.69%	3.15%	0.51%	0.90%



(a) Load output voltages and Load output currents



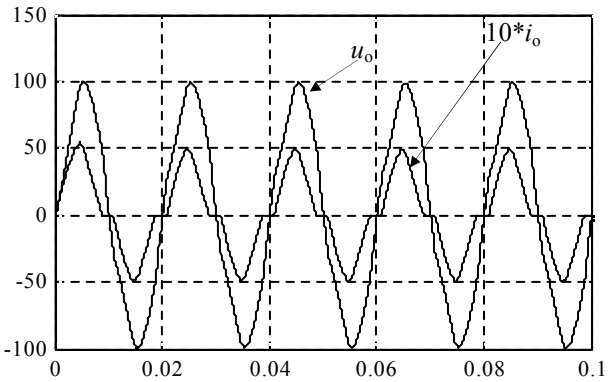
(b) Load voltage error and $\hat{K}_m$



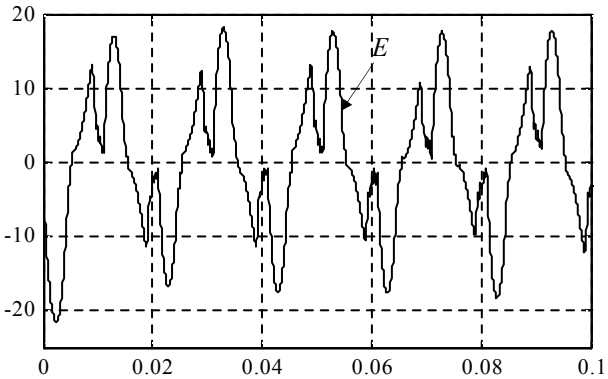
(c) Experimental results of ACSMC

Fig. 8. Simulation and experimental results of the ACSMC scheme under nonlinear load with −16.67% variations in L. (a) and (b) Simulation. (c) Experiment. (Ch1: u_o(50V/div), Ch2: $\hat{K}_m$ (0.67×10^{-7}/div), Ch3: E (5.0V/div) and Ch4:i_o (5A/div))

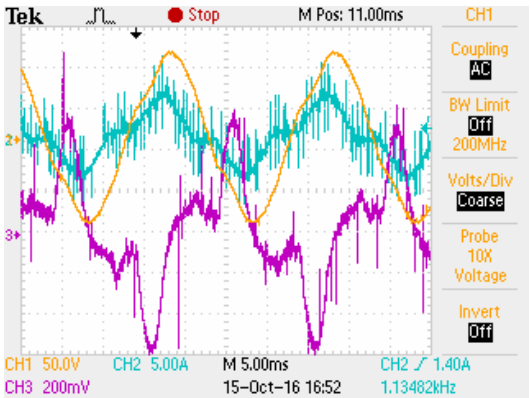
voltage at steady-state full-load operation are presented in Table 3. In this paper, the THD values of the output voltage are obtained by the WaveStar Software for the Tektronix oscilloscopes. From the given Table 3, it can be seen that the ACSMC attains lower THD. Furthermore, it can be observed from Table 3 that the ACSMC has better robustness in all schemes. Note that there is a discrepancy in the THD between the simulation and the experimental



(a) Load output voltages and Load output currents



(b) Load voltage error

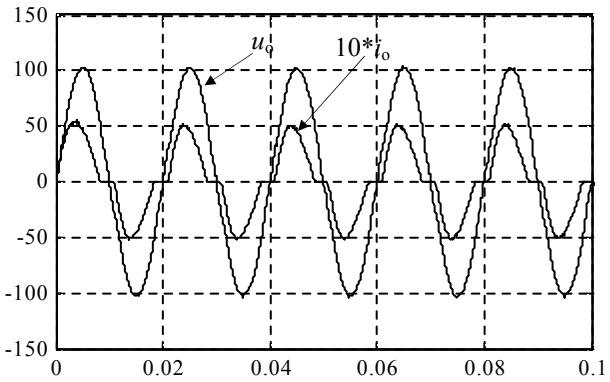


(c) Experimental results of SMC

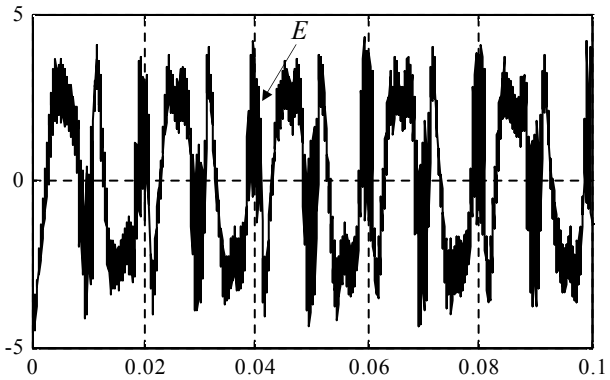
Fig. 9. Simulation and experimental results of the SMC scheme under nonlinear load with −16.67% variations in L. (a) and (b) Simulation. (c) Experiment. (Ch1: u_o(50V/div),Ch2:i_o (5A/div) and Ch3:E (5.0V/div))

results. The main reason for this difference comes from no-ideal effects such as additional distortion caused by noise disturbances in the practical system. This distortion is clearly seen on the experimental waveforms.

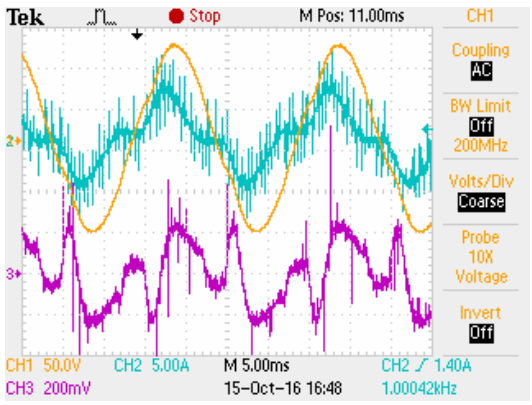
The simulation and experimental results under nonlinear load are in Fig. 8, 9 and 10. To this end, the THD values of the load voltage waveforms achieved with the proposed scheme are 1.17% for simulation and 1.52% for experiment, respectively. In the case of the SMC scheme, the corresponding THD values are 5.34% for simulation and 8.26%for experiment, respectively. In the case of the CSMC scheme, the corresponding load voltage THD values are 2.32% for simulation and 4.25% for experiment, respectively. The experimental results of each control method under resistor-inductor load are in Fig.11(a), Fig. 11 (b) and Fig. 11(c), and the THD values of output voltage



(a) Load output voltages and Load output currents

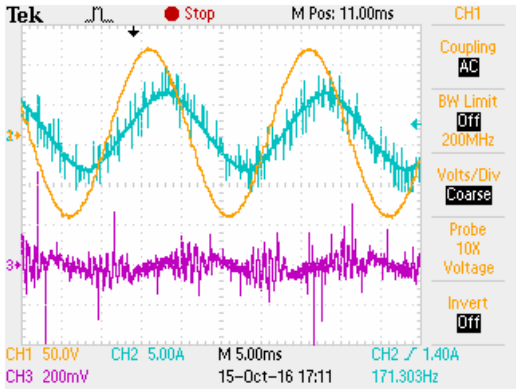


(b) Load voltage error

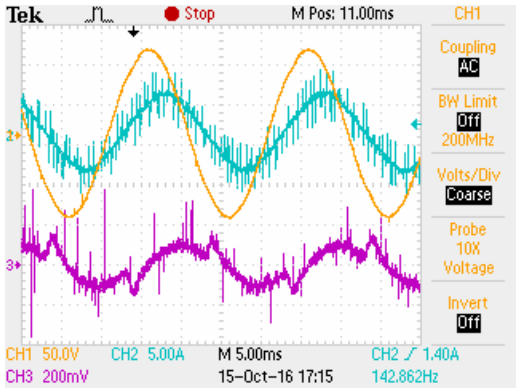


(c) Experimental results of CSMC

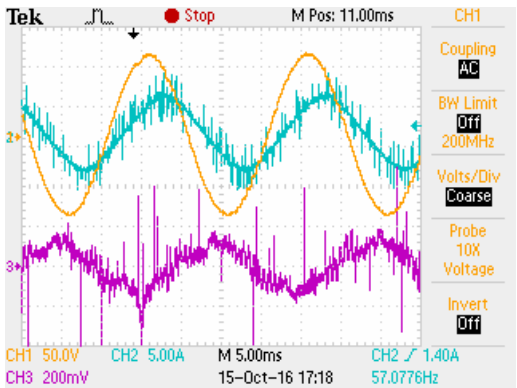
Fig. 10. Simulation and experimental results of the CSMC scheme under nonlinear load with −16.67% variations in *L*. (a) and (b) Simulation. (c) Experiment. (Ch1: u_o(50V/div), Ch2:i_o (5A/div) and Ch3: *E* (5.0V/div))



(a) Experimental results of ACSMC



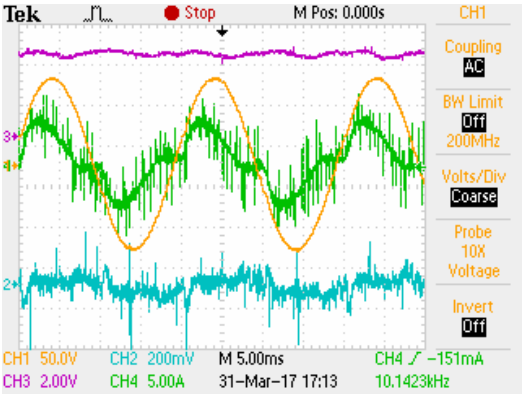
(b) Experimental results of CSMC



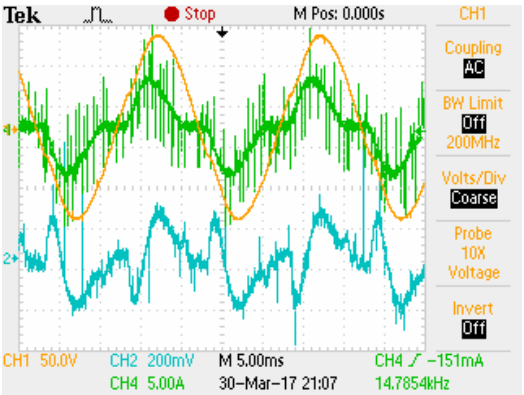
(c) Experimental results of SMC

Fig. 11. Experimental results of the ACSMC, CSMC and SMC scheme under resistor-inductor load with −16.67% variations in *L*. (Ch1: u_o (50V/div), Ch2: i_o (5A/div) and Ch3: *E* (5.0V/div))

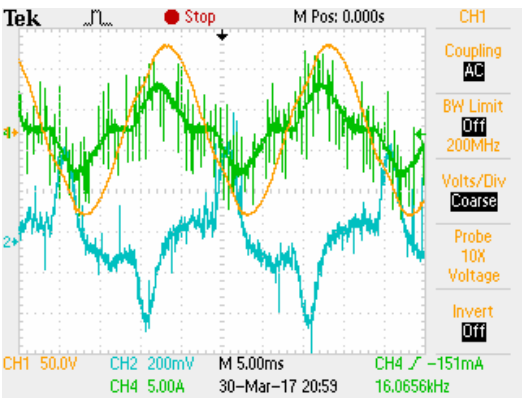
are 0.58%, 1.35% and 1.78%, respectively. In Fig. 8(c), Fig. 9(c) and Fig. 10(c), the average-absolute-error (*ABE*) values of output voltage are 1.61V, 7.95V and 4.05V, respectively. In Fig. 11(a), Fig. 11(b) and Fig. 11(c), the *ABE* values of output voltage are 1.21V, 4.12V and 2.21V respectively. Here, the *ABE* formulate is as following Eq. (45). When the load are the nonlinear load and the resistor-



(a) Experimental results of ACSMC



(b) Experimental results of CSMC

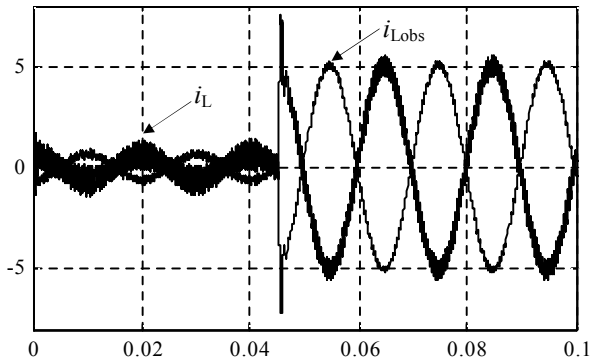


(c) Experimental results of SMC

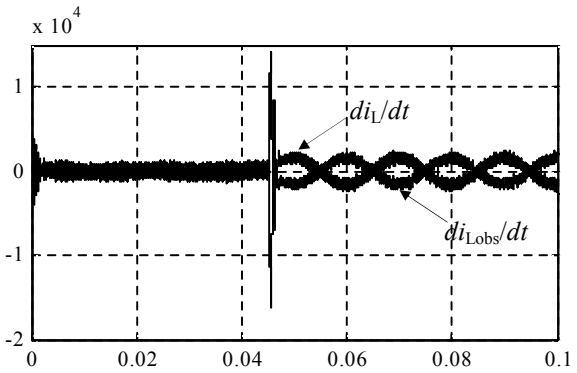
Fig. 12. Experimental results of the ACSMC, CSMC and SMC scheme under nonlinear load with 16.67% variations in L. (Ch1: u_o (50V/div), Ch2: E (5.0V/div), Ch3: $\hat{K}_m$ (0.67×10^{-7}/div) and Ch4:i_o (5A/div))

Table 4. The simulated and measured THD(%) of output voltage for the nonlinear load cases

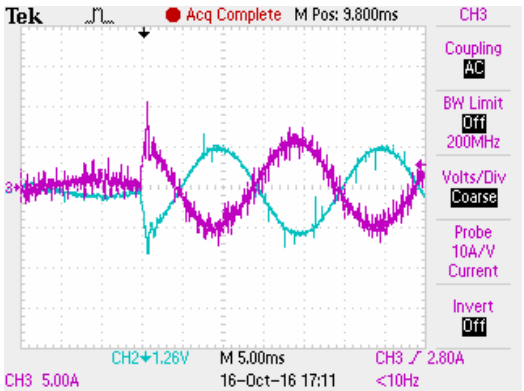
Parameters L	SMC		CSMC		ACSMC	
	Sim.	Exp.	Sim.	Exp.	Sim.	Exp.
5mH	5.34%	8.26%	2.32%	4.25%	1.17%	1.52%
6mH	2.38%	5.28%	1.51%	3.14%	1.02%	1.35%
7mH	4.91%	6.59%	2.47%	5.23%	1.12%	1.24%



(a)



(b)



(c) Experimental results

Fig. 13. Simulation and experimental results of the inductor current estimator under load step change. (a) and (b) Simulation. (c) Experiment. (CH2: reverse of estimated inductor current (5A/div), CH3: inductor current (5A/div))

inductor load, we can also know from the simulation and experiment that the tracking error in the ACSMC is much smaller than in the CSMC and the SMC. The *ABE* value of the CSMC is about half of the SMC's, which has verified the correctness of the inequality (15) and (27).

$$ABE(x) = \frac{1}{N}\sum_{n=1}^{N}|x(n)| \tag{45}$$

where x is the voltage control error (E), N is the total sampling instants.

When the filter inductance L is 5mH, 6mH and 7mH respectively, the THD values of the load output voltage at steady-state nonlinear load operation are presented in Table 4. Fig. 12 shows experimental results when the filter inductance L is selected as 7mH. Fig. 5(c), Fig. 8(c) and Fig. 12(c) provide experimental results of $\hat{K}_m$, and *ABE* values of $\hat{K}_m$ are 4.2×10^{-9}, 7.1×10^{-9} and 7.4×10^{-9}, it demonstrates that the Eq.(29) can estimate the parameter K_m efficiently.

It can be also observed from Table 4 that the ACSMC provides a better load voltage regulation in steady state compared with the SMC and the CSMC. It can be deduced from above results that the ACSMC has the strongest robustness against filter parameters perturbation in three methods. This was because that control parameters $\hat{K}_m$ don't match the actual parameters K_m, it will severely weaken the tracking performance of controllers. In Fig.13, it can be evidently seen that the inductor current estimator has a small estimation error and a good estimation performance can be guaranteed.

From above simulation and experimental results, it can be concluded that the ACSMC achieves better voltage tracking performance (i.e., fast response, smaller steady-state error and lower THD) under various types of loads (i.e., linear load, resistor-inductor load, and nonlinear load) than the CSMC and the SMC even though there exists uncertainties of inductor parameters.

7. Conclusion

This paper has proposed a complementary sliding mode voltage control strategy of a single-phase inverter. To resist the disturbance and inductor parametric change of the model in the inverter system, this paper proposes an adaptive complementary sliding mode voltage control strategy. The stability of three control systems is analyzed and proven through the Lyapunov stability theory and the *LC* parameters adaptive law is developed to increase the robust of system parameters. Meanwhile, an inductor current estimator is adopted in this paper.

To evaluate the validity of the proposed control algorithm, simulations and experiments have been carried out through MATLAB software and a prototype single-phase inverter test bed with a TMS320F28335DSP, respectively. Simulation and experimental results show that the ACSMC scheme revealed a better voltage tracking performance, such as lower THD, smaller steady-state error, and faster transient response than the SMC and the CSMC scheme under various load types even if there exist parameter variations, while it only needs one voltage sensor. Thus, the proposed control strategy is more attractive for fuel cell, and wind generation systems or the others.

Acknowledgements

This work was supported by the National Natural Science Foundation of China (Grant No. 51505360) and the Scientific Research Plan Projects of Shaanxi Education Department (Grant No. 15JK1120).

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