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Comparative Study on SVPWM Switching Sequences for VSIs

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Abstract – Paper presents a comparative study of space vector pulse width modulation (SVPWM) switching sequences for Voltage Source Inverters (VSIs). Various SVPWM switching sequences are studied for two and three level VSIs in linear modulation index region. The computations of dwell times are presented for two and three level VSIs based on space vector geometry in a synchronized and optimized manner. The existing SVPWM switching sequences are implemented using Matlab / Simulink and in an experimental setup for three phase two and three level VSIs. The simulation and experimental waveforms of conventional SVPWM (CSVPWM) and bus clamped SVPWM (BCSVPWM) are demonstrated for two and three level inverter respectively. The performance of different SVPWM switching sequences are evaluated and presented based on weighted voltage total harmonic distortion (THD).

Keywords: Voltage source inverter, Space vector pulse width modulation, Bus Clamping Strategies (BCS)

1. Introduction

Most VSIs form a major part in power electronic industry. The VSI approximates the output voltage through high frequency switching using the pulse width modulation (PWM) techniques. Various PWM strategies exist for VSI fed induction motor drives. The process of switching the electronic devices in a power electronic converter from one state to another is called modulation. The choice of a particular PWM depends on the permissible harmonic content in the output voltage waveform, dc bus utilization and minimum switching losses. The harmonics at the output of a voltage source inverter are also strongly influenced by the method of PWM [1-30]. Several PWM techniques have been reported for voltage source inverter fed electrical motor drives [1-8]. The carrier based PWM [18] and space vector PWM (SVPWM) are the two most recognized methods in the available modulation techniques. In carrier based PWM [1-2, 17-18], three modulating functions are compared against a common carrier to generate the gating signals for the devices in a three phase VSI. The modulating signals are continuous functions of time. The carrier based PWM techniques provides high waveform quality and operates at high switching frequency.

Compared to sine PWM, the distortion in line current is reduced by adding a third harmonic of amplitude 0.25 times the fundamental amplitude (THIPWM4) to the three-phase sinusoidal modulating signals [1, 19]. Both DC bus utilization and reduced harmonics are attained with conventional space vector PWM (CSVPWM) [1-5]. The SVPWM is evaluated as a better technique of PWM implementation as it has advantages over carrier based PWM in terms of good utilization of dc bus voltage, reduced switching frequency, low current ripple and good waveform quality [1-4]. Discontinuous PWM (DPWM) schemes involve modulating functions that are discontinuous functions of time. DPWM schemes are also known as bus-clamping PWM (BCPWM) methods [2-12, 14, 23-24].

The placement of zero vectors [20] gives an additional degree of freedom in SVPWM. Based on the position of zero vectors, numerous SVPWM strategies have been developed [2-12]. Synchronised SVPWM schemes have been mentioned in the literature [3-12]. The principle of SVPWM is based on the switching combination of inverter. are applied to the conventional and modified forms of space vector modulation, leading to the synchronized conventional space vector strategy.

The SVPWM strategies are broadly classified as conventional SVPWM (CSVPWM) strategy and Bus clamping SVPWM(BCSVPWM) strategy. The CSVPWM strategy is known as continuous SVPWM strategy and BCSVPWM [14-16] strategy is known as discontinuous strategy.

BCSVPWM strategy results in clamping of phase to either positive or negative rail for a period of time. Various clamping sequences are available in the SVPWM strategy and the placement of these sequences result in variation of their performance. These strategies exploit the flexibilities offered by the space vector approach like double-switching of a phase within a sub cycle, clamping of two phases within a sub cycle [13]. It is shown that the PWM waveforms generated by these strategies cannot be generated by comparing suitable 3-phase modulating waves with a triangular carrier wave. The performance of switching combinations are evaluated on the basis of total harmonic

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distortion (THD). The performance evaluation of the sequences results in the various switching strategies in SVPWM. The performance evaluation of any strategies depends on the switching loss and the THD. The sequences applied generates flux in the induction motor. The flux generated can be resolved in to d- axis and q-axis. The variation of sequences along these axis will results in the flux ripple in an induction motor drive. The flux ripple can be evaluated based on the closed loop analytical expression [16].

The performance of the existing SVPWM sequences are evaluated analytically as mentioned in literature [15]. The three level space vector is considered as an equivalent two level vector as mentioned in [14]. The Neutral point clamped inverter (NPC) form an important topology in three level VSI [19] due to less number of device and simplicity. The SVPWM sequences in two level inverter is applied to the three level inverter and further investigation is done to evaluate the performance of sequences[23-24]. The performance of different SVPWM techniques are mainly determined by the total harmonic distortion factor of the no load current. The harmonic distortion in the current is determined by the switching frequency and PWM techniques employed. The harmonic distortion in the motor phase currents must be low for satisfactory operation of the motor drive. The PWM application for renewable energy are discussed by numerous authors [23-32]

This paper studies the different SVPWM switching sequences for two level and three level VSIs and compares the performance in terms of weighted voltage THD in linear region of modulation index. This study is essential for the identification of hybrid SVPWM sequences. The switching sequences are heterogeneous in nature with respect to number of switching in different SVPWM techniques. This paper provides a unified comparison approach of two level and three level SVPWM with same pulse number and same modulation index based on a synchronized optimised open loop control. The details of study are discussed in the following sections. Section II presents the literature review of different SVPWM switching sequences for two level and three level along with the optimized dwell time computation and synchronous open loop control.

Section III presents the simulation and experimental results. Performance comparisons are demonstrated in Section IV. Section V concludes the paper.

2. SVPWM Switching Sequences

There are many switching patterns that are used to implement SVPWM in two and three level inverter. The generation of synchronized PWM switching sequences based on space vector maintains the waveform symmetry. It is necessary to arrange the switching sequences so that the switching frequency of each inverter leg is minimized.

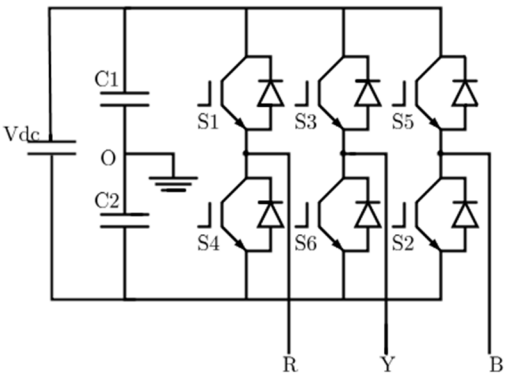


Fig. 1. Circuit diagram of three phase two level VSI

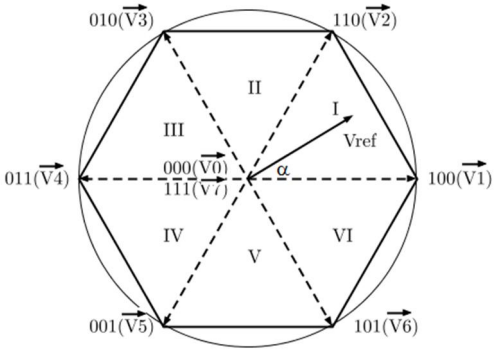


Fig. 2. Space vector diagram of three phase two level VSI

Table 1. Switching table for three phase two level VSI

State	R		Y		B	
	S1	S4	S3	S6	S5	S2
P	1	0	1	0	1	0
N	0	1	0	1	0	1

2.1 Two level SVPWM

The circuit diagram of three phase two level inverter as shown in Fig. 1. The switching table for the corresponding states is mentioned in Table 1. The switching state vectors in two level inverter are defined by the conducting and non conducting switches in the power circuit of the inverter.

Between The eight switching combinations correspond to eight stationary voltage vectors in space. The state diagram of six active voltage vectors $\overrightarrow{V_1}$(100), $\overrightarrow{V_2}$(110), $\overrightarrow{V_3}$ (010), $\overrightarrow{V_4}$ (011), $\overrightarrow{V_5}$(001), $\overrightarrow{V_6}$ (101) and two zero voltage vectors $\overrightarrow{V_0}$(000), $\overrightarrow{V_7}$ (111) forms a hexagon. The voltage vector diagram of two level inverter is shown in Fig 2. The entire space in two level inverter is divided into six equal sectors and size of each sector is 60 degrees. Each sector is bounded by two active vectors. The zero vectors are located at the origin of the hexagon.

The SVPWM is based on volt sec balance equation

$$\overrightarrow{V}_{ref} * T_s = \overrightarrow{V}_1 * T_1 + \overrightarrow{V}_2 * T_2 + \overrightarrow{V}_z * T_z \quad (1)$$

In case of two level inverter the above terms can be

written as Where T_1 corresponds to the active vector time for V1 and T2 corresponds to the active vector time for V_2 and T_z corresponds to the zero vector time for V_z. T_1 can be computed from dwell time equation as

$$T_1 = \frac{\vec{V}_{ref}}{V_{dc}} * \frac{\sin(60-\alpha)}{\sin(60)} * T_s \quad (2)$$

Similarly T_2 can be computed as

$$T_1 = \frac{\vec{V}_{ref}}{V_{dc}} * \frac{\sin(\alpha)}{\sin(60)} * T_s \quad (3)$$

The zero vector switching time can be obtained as follows

$$T_z = T_s - T_1 - T_2 \quad (4)$$

Conventional space vector strategy (CSVPWM) [1] uses two adjacent active vectors and two zero vectors to produce the reference vector in a sector.

Therefore the sequence $\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$ is named as conventional sequence. The clamping sequences $\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$, $\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_0}$, $\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$ and $\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$ use only one zero state for the generation of reference vector and are termed as bus clamping sequence[3-4]. In double switching sequence [6-12] either active state $\overrightarrow{V_1}$ or

Table 2. Switching sequence for three phase two level VSI

Sequence	Angle	Sequence
Conventional	6^0,18^0,30^0, 42^0 54^0	$\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$ $\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_0}$, $\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$, $\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_0}$, $\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$
BBCS-60	6^0,18^0,30^0, 42^0 54^0	$\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$, $\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$ $\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$, $\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$ $\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$,
BBCS-30	6^0,18^0,30^0, 42^0 54^0	$\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$, $\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_0}$ $\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$, $\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_0}$ $\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$,
AZCS-60	6^0,18^0,30^0, 42^0 54^0	$\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$, $\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$ $\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$ $\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_0}$, $\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$
AZCS-30	6^0,18^0,30^0, 42^0 54^0	$\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$, $\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_0}$ $\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$ $\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$, $\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$,
ABCPWM	6^0,18^0,30^0, 42^0 54^0	$\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$, $\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_0}$ $\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$, $\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_0}$ $\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$, $\overrightarrow{V_1}\,\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$, $\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_0}\,\overrightarrow{V_1}$ $\overrightarrow{V_1}\,\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$, $\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_0}\,\overrightarrow{V_1}$ $\overrightarrow{V_1}\,\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$,
ABCPWM	6^0,18^0,30^0, 42^0 54^0	$\overrightarrow{V_2}\,\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$, $\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}\,\overrightarrow{V_2}$ $\overrightarrow{V_2}\,\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$, $\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}\,\overrightarrow{V_2}$ $\overrightarrow{V_2}\,\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$, $\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$, $\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$ $\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$, $\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$ $\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$,

$\overrightarrow{V_2}$ can be applied for more than one interval. Hence, sequences like $\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$, $\overrightarrow{V_1}\,\overrightarrow{V_0}\,\overrightarrow{V_1}\,\overrightarrow{V_2}$, $\overrightarrow{V_2}\,\overrightarrow{V_7}\,\overrightarrow{V_2}\,\overrightarrow{V_1}$ and $\overrightarrow{V_2}\,\overrightarrow{V_1}\,\overrightarrow{V_2}\,\overrightarrow{V_7}$ fall in advanced bus clamping category where an active state time is divided in two equal halves. It results in double switching in a phase for a given sample. The SVPWM sequences for two level inverter are shown in Table 2.

2.2 Three level SVPWM

A three phase three level circuit diagram is shown in Fig 3. There are 27 switching states in three phase three level inverter. The switching table for three phase three level inverter is shown in Table III. The space vector diagram corresponding to the switching states is shown in Fig. 4. The diagram corresponding to the switching states is shown in Fig. 4(a). It is composed of six small hexagons. Each small hexagon presents the space vector diagram of a conventional two-level inverter as shown in Fig. 2. A three-level voltage source inverter produces 24 active vectors, each of normalized magnitudes 1, 0.866, and 0.5, besides zero vectors. In three level inverter a phase switches only between positive dc bus (P) and dc bus midpoint (O) during its positive half cycle and only between 0 and negative dc bus (N) during its negative half cycle. The three-level inverter can be viewed as an equivalent two-level inverter when the reference vector angle α is between

Table 3. Switching table for three phase three level VSI

State	R				Y				B			
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
P	1	1	0	0	1	1	0	0	1	1	0	0
O	0	1	1	0	0	1	1	0	0	1	1	0
N	0	0	1	1	0	0	1	1	0	0	1	1
P = +Vdc/2; O = 0; N = -Vdc/2												

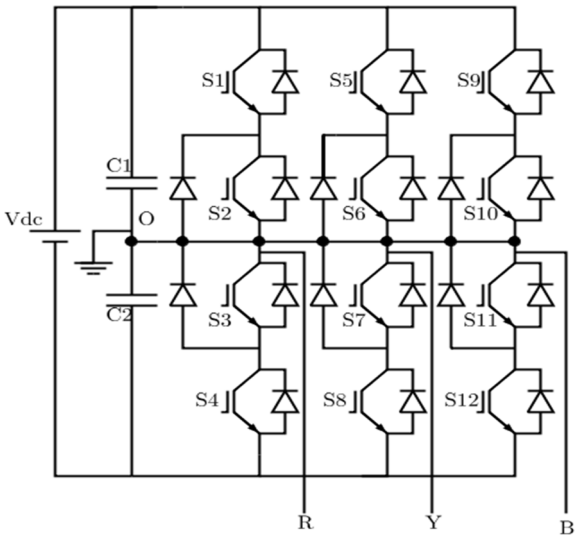


Fig. 3. Circuit diagram of three phase three level neutral point clamped VSI

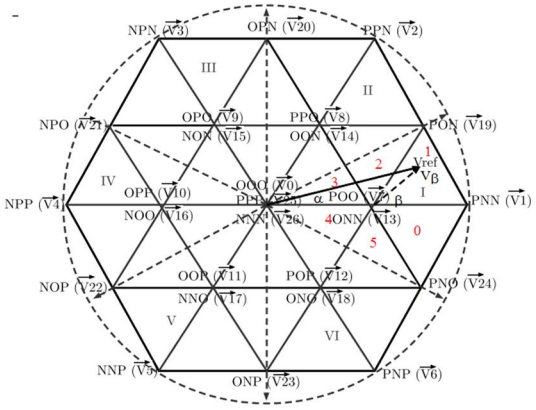


Fig. 4. (a) Space vector diagram of three phase three level VSI (b) equivalent two level space vector

-30^0 and $+30^0$ as shown in Fig. 4(a). This area of three level inverter is considered here as the sector I and is shown in Fig. 4(b). The six sectors corresponding to the two level can be obtained in a three level inverter. The active vectors of the equivalent two level inverters are located on the edges. The zero vector is considered at the midpoint of hexagon. The reference vector is passing through triangle 5,0,1,2 for modulation index (0.5< mi <0.865). The different clamping and double switching sequences. in a two level inverter can be realized in this region. The space vector is based on Volt-Sec balance as shown in equation (1). In case of three level inverter the above terms can be written as

$$T_1 = \frac{\overrightarrow{V_\beta}}{0.5*V_{dc}} * \frac{\sin(60-\beta)}{\sin(60)} * T_s \quad (5)$$

$$T_2 = \frac{\overrightarrow{V_\beta}}{0.5*V_{dc}} * \frac{\sin(\beta)}{\sin(60)} * T_s \quad (6)$$

$$V_{ref} \angle \alpha = V_\beta \angle \beta + 0.5V_{dc} \angle 0 \quad (7)$$

where $V_{ref,}, V_\beta$ are the reference vectors in two level and three level inverter and α, β are the reference angles for the same. In three level inverter the phases are clamped to conditions P O or N. The placing of clamping and double switching sequences results in various types of strategies.

Table 4. Switching Sequences for various triangles in sector I in three level SVPWM

Sector1 Voltage Vectors	Triangle 0	Triangle 1	Triangle 2	Triangle 3
$\overrightarrow{V_0}$	ONN	ONN	ONN	ONN
$\overrightarrow{V_1}$	PNN	PNN	OON	OON
$\overrightarrow{V_2}$	PNO	PON	PON	OOO
$\overrightarrow{V_7}$	POO	POO	POO	POO

Table 5. Switching sequences for three phase three level VSI

Strategy	Angle	Two level equivalent sequence (sector I)
Type-1	-18^0,-6^0, 6^0, 18^0, 30^0	$\overrightarrow{V_1V_2V_7}$ $\overrightarrow{V_7V_2V_1}$,$\overrightarrow{V_1V_2V_7}$ $\overrightarrow{V_7V_2V_1}$,$\overrightarrow{V_1V_2V_7}$
Type-1I	-18^0,-6^0, 6^0, 18^0, 30^0	$\overrightarrow{V_0V_1V_2}$,$\overrightarrow{V_2V_1V_0}$ $\overrightarrow{V_1V_2V_7}$,$\overrightarrow{V_7V_2V_1}$ $\overrightarrow{V_1V_2V_7}$
Type-III	-18^0,-6^0, 6^0, 18^0, 30^0	$\overrightarrow{V_7V_2V_1}$,$\overrightarrow{V_1V_2V_7}$ $\overrightarrow{V_2V_1V_0}$,$\overrightarrow{V_0V_1V_2}$ $\overrightarrow{V_2V_1V_0}$
Type-IV	-18^0,-6^0, 6^0, 18^0, 30^0	$\overrightarrow{V_0V_1V_2}$,$\overrightarrow{V_2V_1V_0}$ $\overrightarrow{V_0V_1V_2}$,$\overrightarrow{V_2V_1V_0}$ $\overrightarrow{V_0V_1V_2}$,
A1012	-18^0,-6^0, 6^0, 18^0, 30^0	$\overrightarrow{V_1V_0V_1V_2}$, $\overrightarrow{V_2V_1V_0V_1}$ $\overrightarrow{V_2V_7V_2V_1}$, $\overrightarrow{V_1V_2V_7V_2}$ $\overrightarrow{V_2V_7V_2V_1}$,
A2721	-18^0,-6^0, 6^0, 18^0, 30^0	$\overrightarrow{V_2V_7V_2V_1}$, $\overrightarrow{V_1V_2V_7V_2}$ $\overrightarrow{V_1V_0V_1V_2}$, $\overrightarrow{V_2V_1V_0V_1}$ $\overrightarrow{V_1V_0V_1V_2}$,
A7212	-18^0,-6^0, 6^0, 18^0, 30^0	$\overrightarrow{V_2V_1V_2V_7}$, $\overrightarrow{V_7V_2V_1V_2}$ $\overrightarrow{V_1V_2V_1V_0}$ $\overrightarrow{V_0V_1V_2V_1}$, $\overrightarrow{V_1V_2V_1V_0}$
A0121	-18^0,-6^0, 6^0, 18^0, 30^0	$\overrightarrow{V_1V_2V_1V_0V_0V_1V_2V_1}$, $\overrightarrow{V_2V_1V_2V_7}$, $\overrightarrow{V_7V_2V_1V_2}$ $\overrightarrow{V_2V_1V_2V_7}$,

In 60^0 and 30^0 clamping the phases are clamped to 60^0 and 30^0 in the positive and negative half cycle. The 60^0 clamping is divided in to various types for various load conditions namely unity power factor (upf),lagging and leading load conditions. They are classified as type I, type II, type III, type IV [14] strategy. The typeI strategy uses the sequence $\overrightarrow{V_1V_2V_7}$ throughout the sector. Sequence $\overrightarrow{V_0V_1V_2}$ is used for type IV strategy. Type II strategy uses sequence $\overrightarrow{V_0V_1V_2}$ and $\overrightarrow{V_1V_2V_7}$ in the first half and second half of the sector respectively. Sequences $\overrightarrow{V_1V_2V_7}$

and $\overrightarrow{V_0}\overrightarrow{V_1}\overrightarrow{V_2}$ are used in the first half and second half of the sector in type IV strategy. Therefore degree clamping (upf), 60^0 degree clamping (lag), 60^0 degree clamping (lead) and 300 clamping of a phase respectively in type I and type II type III and type IV strategy. Another category of SVPWM strategies use double switching sequences. The strategies are named as A0121, A7212, A1012, A2721[15-16]. A0121 use the sequences $\overrightarrow{V_0}\overrightarrow{V_1}\overrightarrow{V_2}\overrightarrow{V_1}$ and $\overrightarrow{V_7}\overrightarrow{V_2}\overrightarrow{V_1}\overrightarrow{V_2}$ in sector I. A7212 use the sequences $\overrightarrow{V_7}\overrightarrow{V_2}\overrightarrow{V_1}\overrightarrow{V_2}$ and $\overrightarrow{V_0}\overrightarrow{V_1}\overrightarrow{V_2}\overrightarrow{V_1}$ in sector I. A1012 use the sequences $\overrightarrow{V_1}\overrightarrow{V_0}\overrightarrow{V_1}\overrightarrow{V_2}$ and $\overrightarrow{V_2}\overrightarrow{V_7}\overrightarrow{V_2}\overrightarrow{V_1}$ in sector I. A2721 use the sequences $\overrightarrow{V_2}\overrightarrow{V_7}\overrightarrow{V_2}\overrightarrow{V_1}$ and $\overrightarrow{V_1}\overrightarrow{V_0}\overrightarrow{V_1}\overrightarrow{V_2}$ in sector I. Table 4 shows the various switching sequences used in various triangles in three level inverter. Table 5 shows the various switching sequences used in sectors in three level inverter.

2.3 Dwell time optimization and implementation in microcontroller

An open loop digital architecture is developed to implement the existing SVPWM techniques. The SVPWM is implemented in an 8 bit PIC microcontroller (PIC 18F452) under open loop control with a fixed value of modulation Index. Under this method the samples can be placed exactly at 30^0 as timing and pulse generation are maintained in a centralized and synchronized manner. The 8 bit voltage vector is sampl ed with a time period of T_s. Timing diagram of signal generation is shown in Fig. 5. There are 5 samples in sector I. 3rd sample is placed at 30^0. This architecture can be scaled for high frequency implementation. There is a delay involved in between the samples and sector identification and dwell time calculation.

The existing SVPWM techniques are implemented in a PIC controller using optimized computation algorithm. Region detection algorithm is implemented with multi-plication operation only. Division and arc tan operations are avoided. All computations are done on PIC 18f452 and pulse generation is achieved. SVPWM architecture is implemented following digital controller architecture. An 8-bit command is used for the reference voltage vector. The SVPWM controller samples the reference 8-bit command periodically by a signal generator block. There is a delay involved in between the samples and sector identification and dwell time calculation. This delay does not affect sample placement and can be aggregated with controller delay. Dwell time values are calculated for each sample. Subdivision of active vector is carried out by shifting operation as only two level sequences are used. Hence the architecture is scalable as higher levels can be implemented with additional shift operations. The optimized sequences for the proposed algorithm for different modulation index are stored as a part of code segment. In this implementation only 6 kB instruction memory is used (150 combinations are stored for various modulation indexes) whereas total available instruction memory is 64 kB. Switching sequences and the corresponding angles are stored in the look up table only for the first sector. Sequences for the other sectors are derived from the first sector. Therefore s pace constraint is not an important issue in look up table. The desired goal is to implement 3 level or more with switching frequency upto 10 kHz. PIC processing time for 75 samples per sector (this leads to a switching frequency of maximum 10 kHz) takes only 2.5ms. Fundamental frequency is 50 Hz and there is a slack of 17.5ms. Existing approaches do not use look up table

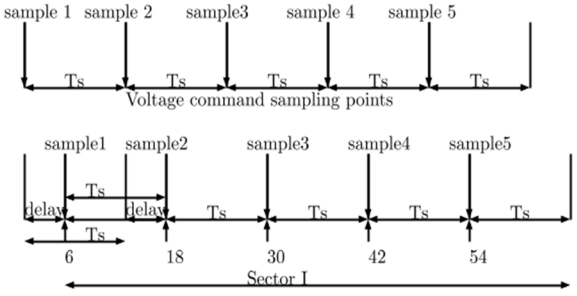
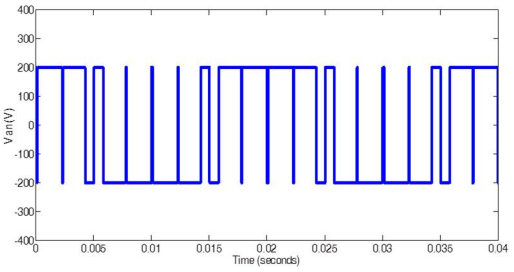


Fig. 5. Timing diagram for signal generation



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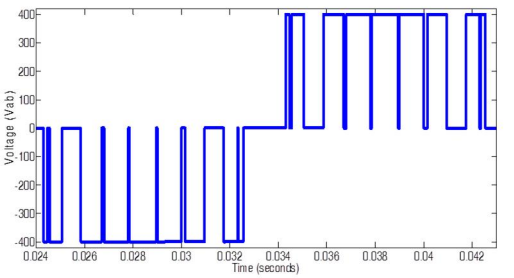

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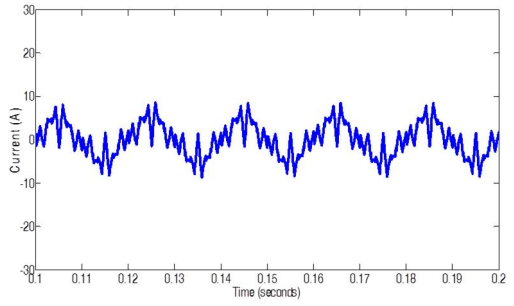


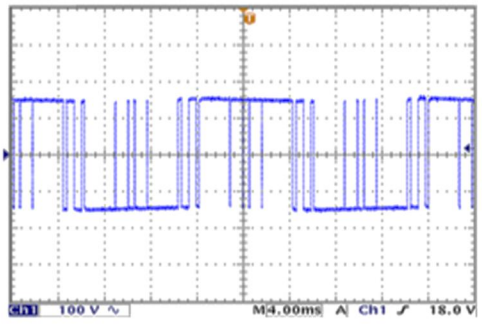
(c)

Fig. 6. Simulation Results for Two level VSI (a) Pole voltage waveform (b) Line voltage waveform (c) Current waveform

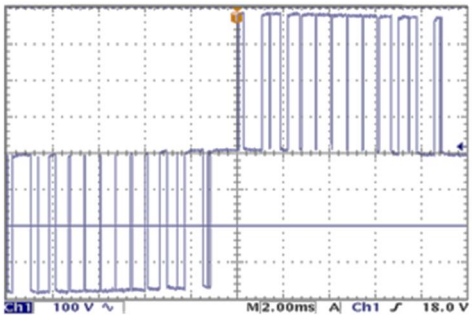
and generate PWM signal by c omparing measured voltage values. These approaches are not suitable to implement bus clamping algorithm. Hence the proposed digital controller architecture meets the requirement for high frequency and higher number of voltage level applications.

3. Simulation and Experimental Results

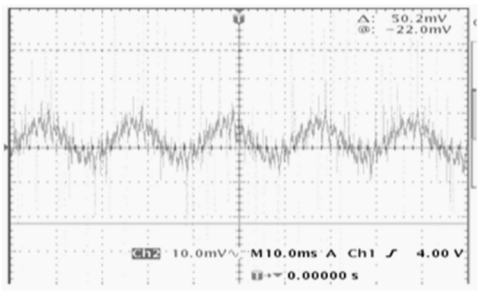
The algorithms for existing SVPWM techniques are mathematically modeled for three phase two level and three level NPC Inverter with an induction motor in MATLAB/SIMULINK environment. The experimental prototype of three level inverter and two level inverter are developed with a DC bus voltage of 400V. The SVPWM algorithm is implemented in a low cost PIC 18F452 microcontroller.



(a)



(b)



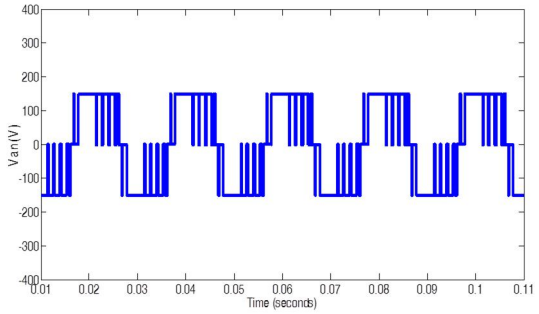
(c)

Fig. 7. Experimental Results for Two level VSI (a) Pole voltage waveform (b)Line voltage waveform (c) Current waveform

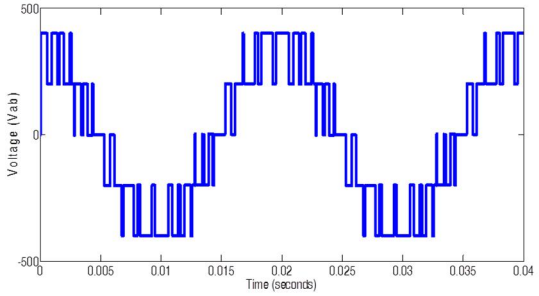
4. Performance Evaluation of Sequences

Performance of different Bus clamped strategies depend on specific sequences, clamping type (30degree or 60 degree), pulse number and modulation index values. The results are evaluated for different SVPWM startegies for a fixed frequency of 50 Hz. Different output voltages are obtained by varying the modulation index.

The performance of various clamping strategies varies under different modulation index range. The modulation index range of study is chosen in the range of 0.55 to 0.865. The analytical evaluation of various clamping strategies are done based on the error voltage for the computation. The error voltage vector sees the motor as its leakage inductance. The time integral of the error voltage vector is named as stator flux ripple vector [4-7]. The reduction of d axis flux ripple significantly reduces the harmonics in the line current ripple in a PWM inverter caused by the



(a)



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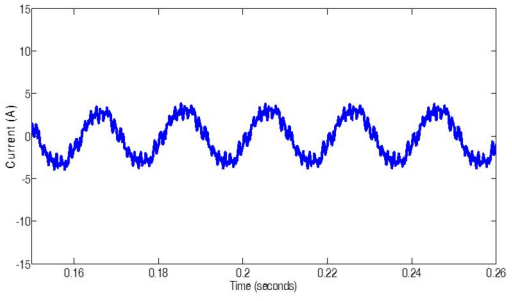
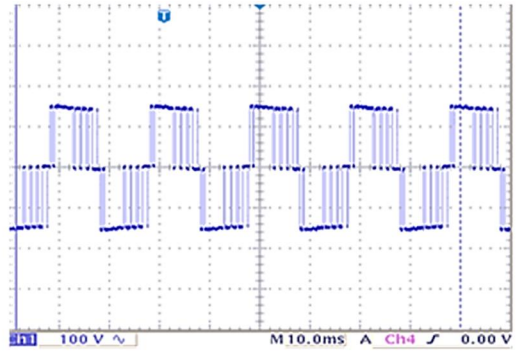
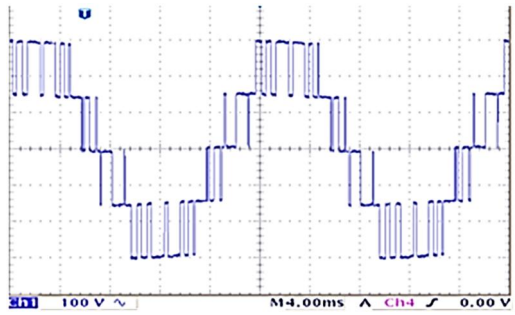


(c)

Fig. 8 Simulation Results for Three level VSI (a) Pole voltage waveform (b) Line voltage waveform (c) Current waveform



(a)



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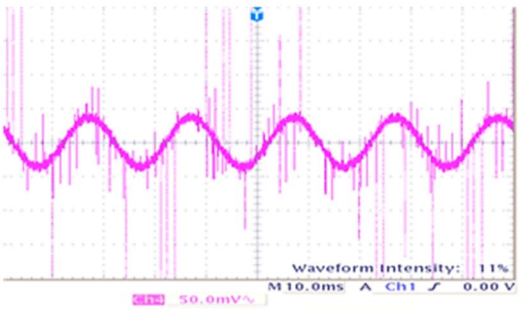


(c)

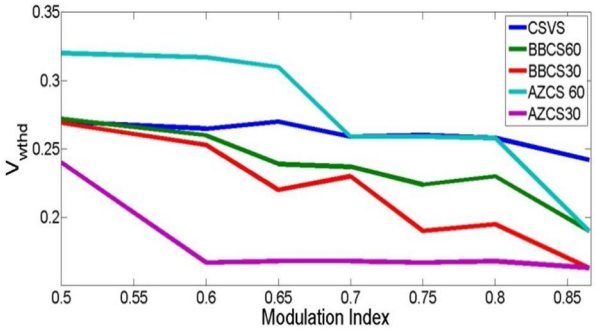
Fig. 9. Experimental results for Three level VSI (a) Pole voltage waveform (b) Line voltage waveform (c) Current waveform

instantaneous error between the applied and reference voltages.

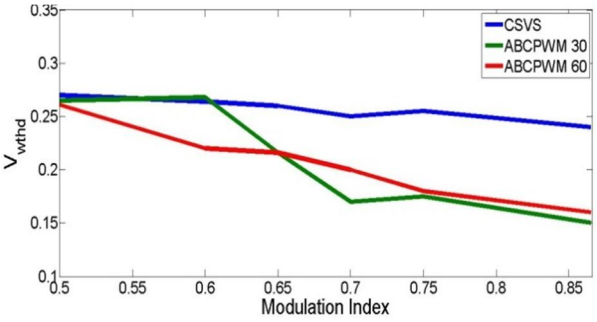
The resulted THD in CSVPWM is less than bus clamped strategies at lower modulation indices. 30 degree bus clamping strategies works better than 60 degree bus clamping strategies at lower modulation indices. The performance analysis of different switching strategies for 3- phase drives is discussed based on no-load current. The performance analysis of different sequences are evaluated on the basis of weighted voltage THD (wthd).

The weighted voltage total harmonic distortion is defined as

$$V_{wthd} = \sqrt{\frac{\sum\left(\frac{V_n}{n}\right)^2}{V_1}} \tag{8}$$



(a)



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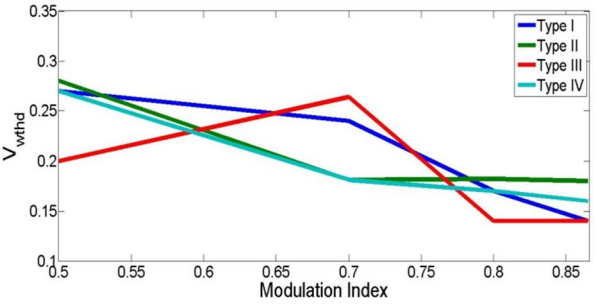
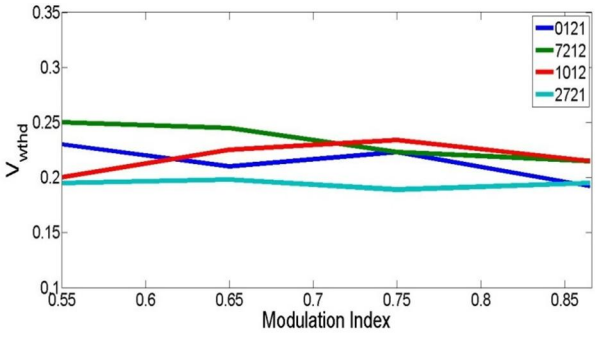


(c)



(d)

Fig. 10. (a) & (b) Performance evaluation of clamping and advanced bus clamping strategies in two level inverter, (c) & (d) Performance evaluation of clamping and advanced bus clamping strategies in three level inverter

where V_1 and V_n are RMS values of the fundamental and nth harmonic voltage of the line voltage waveform

respectively. The weighted voltage THD is approximately proportional to the current THD and independent of motor parameters. The performance of different SVPWM techniques on two level inverter and three level inverter are studied at different modulation indices. Fig. 10(a) and 10(b) present a comparison of the harmonic distortions due to the different strategies in a two level inverter. Fig. 10(c) and 10(d) present different strategies in a three level inverter. CSVPWM uses conventional sequence 0127 throughout the cycle. 30 degree bus clamping strategies works better than 60 degree bus clamping strategies at lower modulation indices due to the reduction in total harmonic distortion AZCS uses 7212 or 0121 in the middle sample and BBCS uses 012 or 721 in the middle sample. Despite the lack of quarter wave symmetry (QWS), AZCS performs best for higher modulation indices. The effect of modulation index on the Type I, Type II, Type III and Type IV.SVPWM technique is presented in Fig. 10.(c). As modulation index increases the THD is reduced. The resulted THD in CSVPWM is less than bus clamped THD at higher modulation index of bus clamping techniques is due to the reduction in d axis flux ripple. d axis flux ripple is more dominant for higher modulation indices but q axis flux ripple varies for the entire modulation range. ABCPWM sequences result in double switching in a phase for a given sample. Therefore the number of switching is higher than the Type I, Type II strategy with same sample number. In a three level inverter voltage vector plane, the sequences 1012 and 2721 result less ripple in the lower and medium modulation index range. In higher modulation index region most of the samples are located in the first half of sector and therefore the sequence 0121 result in reduction of harmonic content. The weighed harmonic distortion analysis is done in three level level inverter for 60 degree clamping and 30 degree clamping under different modulation index conditions. The experimental plots of weighed harmonic distortion shows that the higher modulation index regions 30 degree clamping has worse performance compared to 60 degree clamping strategies.

At lower modulation index regions 30 degree clamping has better performance. Type III strategy is better at lower and higher modulation index. Type IV strategy is better at mid modulation index range. A2721 has better performance among double switching sequences.

The performance index is computed as

$$\text{Performance Index}(\%)= \frac{V_{wthd-sequence}}{V_{wthd-conventional}} *100 \qquad (9)$$

The comparison of performance is done for strategies of equal type in two and three level inverter and is listed in Table 6. The clamping strategies are compared for the same value of pulse number and at modulation index of 0.85. as shown in Table 4. The advanced bus clamping strategies and A2721 has better performance compared to other strategies for the same parameters. The experimental and simulation method shows that bus clamping methods has less distortion compared to conventional SVPWM methods.

Table 6. Performance evaluation in two and three level inverter at modulation index=0.85 Pulse number = 15

Sequence	Simulation results		Experimental results	
	2level	3level	2level	3level
BBCS30 & Type IV	82%	80%	78%	75%
BBCS60 & Type I	89%	88%	85%	79%
ABCPWM A1012	76%	79%	72%	70%
ABCPWM A2721	69%	63%	62%	56.8%
ABCPWM A7212	78%	64%	74%	70%

5. Conclusion

This paper presents a study of transitions of different SVPWM switching sequences for two and three level inverter in a synchronized optimized SVPWM open loop control in PIC 18f452microcontroller. The optimized dwell time computation algorithm is verified in simulation and experiment results. The weighted voltage THD is considered as performance index. The effect of different switching sequences on THD have been analyzed on three level and two level inverter. It is observed that an appropriate clamping position at modulation index range has reduced value of THD. For practical bus clamping strategies for higher modulation indices with respect to Vwthd proves out to be superior performances compared to conventional sequences. The performance of advanced bus clamping sequence (A2721) outcomes conventional sequences bus clamping strategies. Three level sequence (A2721) outcomes two level (A2721 sequence) by 8% at higher modulation index range.

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