# 6-GHz-to-18-GHz AlGaN/GaN Cascaded Nonuniform Distributed Power Amplifier MMIC Using Load Modulation of Increased Series Gate Capacitance

Dong-Hwan Shin, In-Bok Yom, and Dong-Wook Kim

**A 6-GHz-to-18-GHz monolithic nonuniform distributed power amplifier has been designed using the load modulation of increased series gate capacitance. This amplifier was implemented using a 0.25-µm AlGaN/GaN HEMT process on a SiC substrate. With the proposed load modulation, we enhanced the amplifier's simulated performance by 4.8 dB in output power, and by 13.1% in power-added efficiency (PAE) at the upper limit of the bandwidth, compared with an amplifier with uniform gate coupling capacitors. Under the pulse-mode condition of a 100-µs pulse period and a 10% duty cycle, the fabricated power amplifier showed a saturated output power of 39.5 dBm (9 W) to 40.4 dBm (11 W) with an associated PAE of 17% to 22%, and input/output return losses of more than 10 dB within 6 GHz to 18 GHz.**

**Keywords: AlGaN/ GaN HEMT, Distributed power amplifier, High power amplifier, MMIC.**

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## I. Introduction

Wideband power amplifiers are essential in electronic systems such as electronic warfare (EW) systems and electromagnetic compatibility (EMC) testing systems that are required to operate within a broad frequency range. Thus far, traveling wave tube (TWT)-based power amplifiers have generally been used for wideband and high-power applications in spite of their disadvantages in terms of occupied volume and reliability. Over the past few years, many studies on solid-state monolithic amplifier solutions using GaAs and GaN technologies have been made to replace TWT amplifier solutions within the microwave region.

Recent advances in GaN process technology have led to an improved performance in high-power amplifier MMICs. A GaN high-electron mobility transistor (HEMT) on a SiC substrate has a bandgap two to three times wider than those of conventional Si and GaAs devices, a high saturated electron velocity of $2.5 \times 10^7$ cm/s yielding a high current density, and a high thermal conductivity of 4.5 W/cm-K. These electrical and thermal properties of the GaN HEMT provide high-power/high-efficiency amplifiers with remarkable benefits [1].

A distributed amplifier (DA) topology is more advantageous in terms of a flat gain and low return loss in a wide frequency range than other amplifier structures with lossy matching, a balanced topology, and a feedback network. This is because the input and output reactive elements of the active devices can be absorbed into the gate and drain artificial transmission lines, and the Bode–Fano criterion does not limit the operating frequency [2]–[4].

Typically, it is difficult for a distributed amplifier topology to achieve high power and high efficiency owing

to its inherent characteristics. To increase the output power and efficiency of a distributed power amplifier (DPA), a nonuniform distributed approach is preferred, allowing each characteristic impedance of the drain artificial transmission lines to reach near the optimum load impedance of each transistor [5].

This paper presents a 6-GHz-to-18-GHz GaN two-stage nonuniform distributed power amplifier (NDPA) MMIC using a load modulation effect that allows the drain transmission lines near the output port to have higher characteristic impedance than that required in conventional approaches. For high gain in a wide frequency range, the NDPA MMIC is designed in a cascaded structure. To maintain a flat output power and efficiency at the maximum operating frequency, the gate coupling capacitances of the second-stage HEMTs near the output port are increased for the higher characteristic impedance of the drain transmission lines. A higher characteristic impedance is achieved by the load modulation effect from the increased gate voltages and the resulting increased drain currents. With the proposed load modulation, the amplifier's performance is enhanced by 4.8 dB in output power and by 13.1% in power-added efficiency (PAE) at the upper limit of the bandwidth, as well as an output power variation of less than 1 dB and a PAE variation of less than 5%.

## II. Device Technology and Unit Cell Design

The NDPA MMIC is fabricated using a GH25-10 0.25-μm AlGaN/GaN HEMT on a SiC substrate of United Monolithic Semiconductors (UMS). The HEMT breakdown voltage is above 100 V, the pinch-off voltage is around −3.5 V, and $I_{dss}$ is 480 mA/mm. In addition, $f_{max}$ and $f_T$ of the 0.25-μm GaN technology are about 90 GHz and 30 GHz at a drain current of 60 mA for a 4 × 100 μm HEMT cell, respectively. The SiC wafer is thinned to 100 μm, and its backside plane is plated with Au [6]. The nominal quiescent condition of the GH25-10 HEMT cell is a 30-V drain voltage and 100-mA/mm drain current; however, a derating of the drain voltage is applied for reliability and thermal stability in military applications. The selected bias condition for the HEMT cell in this work is a 26-V drain voltage and 80-mA/mm drain current.

The periphery of each HEMT in the NDPA configuration should be carefully selected considering the upper cutoff frequency of the artificial transmission line and the required linear gain/output power. If a large device size is selected for a large output power, the cutoff frequency of the amplifier cannot have a high value without sacrificing the gain. To select the proper device

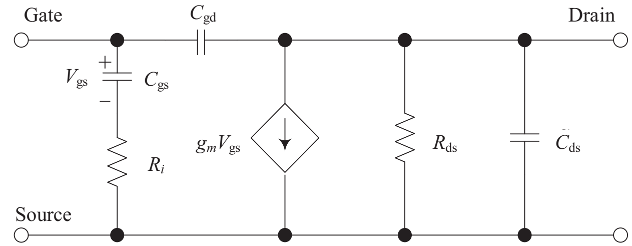


Fig. 1. Simplified equivalent circuit model of a GaN HEMT.

size, the intrinsic elements of the GaN HEMT shown in Fig. 1 are extracted through admittance $Y$ parameters, which are derived from the intrinsic small-signal equivalent circuit [5], [7].

$$R_{ds}^{-1} = Re(y_{22} + y_{12}), \tag{1}$$

$$C_{ds} = \frac{1}{\omega} Im(y_{22} + y_{12}), \tag{2}$$

$$R_i = Re\left(\frac{1}{y_{11} + y_{12}}\right), \tag{3}$$

$$\frac{1}{\omega C_{gs}} = -Im\left(\frac{1}{y_{11} + y_{12}}\right), \tag{4}$$

$$g_m = \frac{|y_{21} - y_{12}|}{|y_{11} + y_{12}|}\left\{Im\left(\frac{1}{y_{11} + y_{12}}\right)\right\}^{-1}. \tag{5}$$

Using equivalent model parameters of the FET cell determined by (1) through (5), the cutoff frequency, optimum number of stages, and gain of a conventional DA can be calculated as shown in [2], [5], and [8], respectively. For a 4 × 100 μm HEMT cell, $C_{gs}$ = 0.97 pF, $R_i$ = 5 ohm, $C_{ds}$ = 0.145 pF, $R_{ds}$ = 373 Ω, $C_{dg}$ = 0.023 pF, and $g_m$ = 0.14 S are obtained at 14 GHz. If the input and output impedances of the amplifier are 50 Ω, the cutoff frequency of the DA is only 7.96 GHz owing to the large $C_{gs}$ value of the FET cell. However, the cutoff frequency of the DA can be increased through the insertion of series-connected coupling capacitors at the gates of the HEMTs, although they decrease the linear gain of the DA. The coupling capacitors are also used as stabilizing elements when they are connected in parallel with resistors at the gate nodes.

A schematic circuit and layout of the parallel RC network is illustrated in Fig. 2. The RC parallel network extends the cutoff frequency of the input artificial transmission line and makes the amplifier unconditionally stable. The value of $C_S$ is set to be equal to or less than the value of $C_{gs}$ for lowering the input equivalent capacitance of the FET cell, and $R_S$ has a slightly high value to avoid affecting the capacitive coupling. The values of $C_S$ and $R_S$ in our design are basically 0.2 pF and 300 Ω, respectively.

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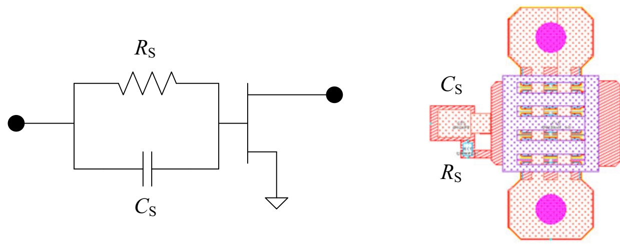
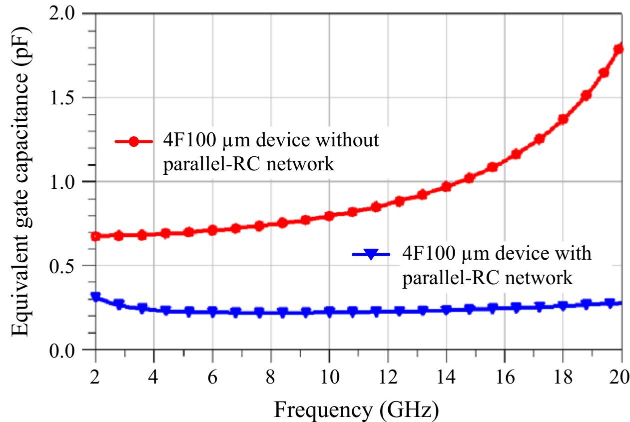
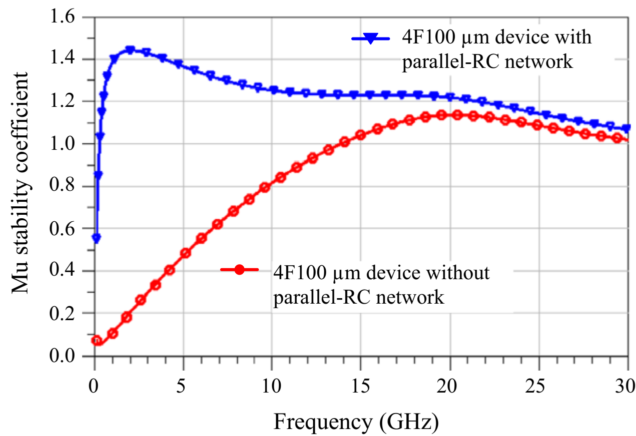



Fig. 2. Schematic circuit and layout of capacitively coupled stabilized HEMT.




(a)




(b)

Fig. 3. Gate capacitance (a) and Mu stability factor (b) vs. frequency before and after applying parallel RC network at the gate.

The effects of the parallel RC network are shown in Fig. 3. The equivalent input capacitance of the capacitively coupled 4 × 100-μm cell is reduced to 0.23 pF, which increases the cutoff frequency up to 27 GHz. The 4 × 100 μm cell with a parallel RC network is stable from 300 MHz in terms of the geometrically derived stability coefficient (Mu).

The load–pull simulation result of a 4 × 100 μm HEMT with a parallel RC network is plotted in Fig. 4.

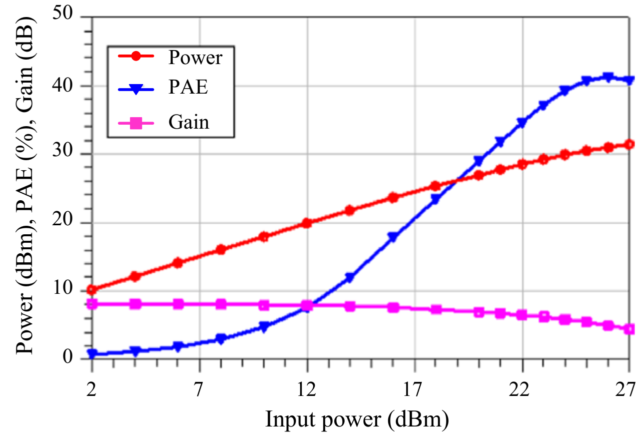



Fig. 4. Load–pull simulation results of 4 × 100 μm HEMT with a parallel RC network operating at 18 GHz.

The drain bias point is $V_{DS}$ = 26 V and $I_{DS}$ = 46 mA. The result shows a 41% PAE with an associated output power of 31 dBm at 18 GHz where the optimum load impedance is 11.5 + j43.6 Ω. The capacitor connected in series with the transistor acts as a voltage divider, and thus, the gain is reduced to 5 dB when the input power is 26 dBm. To obtain a 10-W output power in the DPA, we need at least ten 4 × 100 μm HEMTs.

## III. Distributed Power Amplifier Design

Conventional design methods for NDPAs are explained well in previous studies [5], [9], [10]. The representative description of NDPA topology is shown in Fig. 5 [10]. In the NDPA design, a drain termination resistor of the first transistor $Q_1$ can be removed for moderate bandwidth applications ($f_{max}/f_{min} < 3$) [10], and HEMT cells with unequal gate width and drain lines with unequal characteristic impedances are fully utilized. The NDPA can provide each transistor with a nearly optimum load impedance through the proper impedance tapering of the drain lines. If an individual HEMT cell is matched to its optimum load resistance ($R_{p,n}$), the relationship between the total HEMT periphery ($W_Q$) of the NDPA and the load resistance ($R_L$) is expressed as (6) because each $R_{p,n}$ is combined in parallel and the total parallel combination should be equal to $R_L$ [10]. Here, $R_P$ is the normalized optimum load resistance for maximum output power, and it corresponds to the optimum load resistance of the transistor with a 1-mm gate width.

$$\frac{R_p(\Omega \cdot \mathrm{mm})}{R_L(\Omega)} = \sum_{i=1}^{N} W_{Q_i} = W_Q. \qquad (6)$$

With $R_L$ fixed, (6) limits the total transistor periphery and thus the output power of the NDPA. To increase the

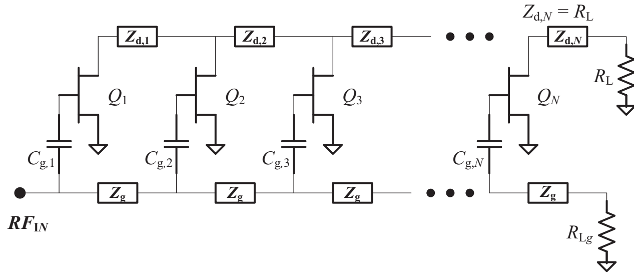



Fig. 5. Conventional NDPA topology.

output power, it is necessary to transform $R_L$ to a lower value or to make the amplifier operate at a higher voltage to enlarge $R_p$. The load resistance of the $n$th transistor can be replaced by the characteristic impedance $Z_{d,n}$ of the $n$th drain line, as shown in (7) [10].

$$Z_{d,n} = \frac{R_p(\Omega \cdot \text{mm})}{\sum_{i=1}^{n} W_{Q_i}}. \tag{7}$$

The output power density and the value of $R_p$ can be found from a loadpull simulation. For a 4 × 100 μm HEMT, we obtain an output power density of 3 W/mm and $R_p$ of 70 Ω-mm at a drain-source voltage of 26 V. A DPA consisting of ten 4 × 100 μm HEMT cells theoretically has a 12-W output power if the drain line impedance of each cell is tuned to the optimum value.

Figure 6 shows the optimum characteristic impedance $Z_{d,n}$ calculated for nonuniform distributed power amplifiers with equal- and unequal-sized HEMTs. The NDPA with equal-sized HEMTs is composed of ten 4 × 100-μm HEMTs, and the NDPA with unequal-sized HEMTs has one 6 × 100-μm HEMT, which corresponds to $Q_1$ in Fig. 5, and nine 4 × 100-μm HEMTs. In the former NDPA, $Z_{d,1}$ is 175 Ω, which is an impedance value unavailable by the microstrip line on a SiC substrate when we consider the current density limit and the design rules of the given GaN process. By choosing a larger HEMT as $Q_1$, the first drain line impedance can be realizable. In the latter NDPA, we use a 6 × 100-μm HEMT as the first transistor, and reduce $Z_{d,1}$ to 117 Ω.

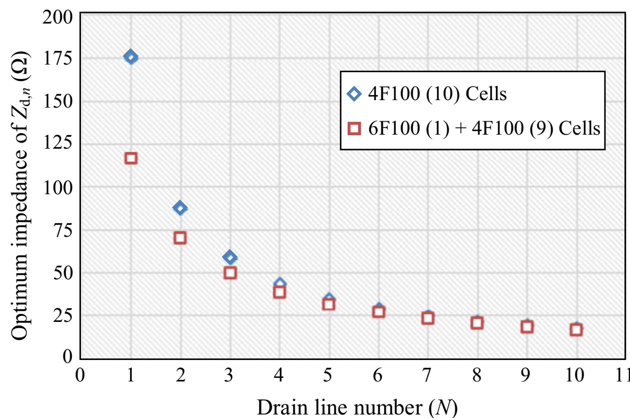



Fig. 6. Optimum characteristic impedance, $Z_{d,n}$, calculated for nonuniform distributed power amplifiers with equal-sized HEMTs and unequal-sized HEMTs.

The load resistance $R_L$ should be reduced to the optimum impedance value of the last HEMT cell to obtain a sufficient output power. In the 10-cell DPA design, $R_L$ is about 17 Ω, as shown in Fig. 6, which is too low to be realized in a compact NDPA design. In this paper, considering the circuit size, 30 Ω is used as the minimum drain line impedance. Because of a relatively higher drain line impedance compared with the estimated optimal load resistance, the last three transistors ($Q_8$, $Q_9$, and $Q_{10}$) are poorly loaded, and therefore will be unable to properly contribute to the output power and efficiency increase. This problem appears especially in the transistors of the DPA requiring a low optimum load resistance, and the maximum output power of the DPA is not fully achieved. To overcome this constraint and increase the output power, a new load modulation concept can be used.

Figure 7 shows a simplified model using a current source instead of the $n$th transistor in the DPA. The relationship between the optimum output resistance $R_{p,n}$ and the characteristic impedance of the drain line (or the load resistance) $Z_{d,n}$ required for the maximum output power is described as

$$R_{p,n} = \frac{V}{-I_{Qn}} = Z_{d,n}\left(1 + \frac{\sum_{i=1}^{n-1} I_{Qi}}{I_{Qn}}\right). \tag{8}$$

If we increase $I_{Qn}$, we are allowed to have a larger $Z_{d,n}$ for the same $R_{p,n}$. With some mathematical manipulations, the required optimum drain line impedance $Z_{d,n}$ can be calculated for the case with uniform gate coupling capacitances and the case with variations in the gate coupling capacitances. For the former case,

$$Z_{d,n} = \frac{R_{p,n}}{n} = \frac{R_p(\Omega \cdot \text{mm})}{n \cdot W_{Q_n}}, \forall I_{Q_i} = I_1. \tag{9}$$

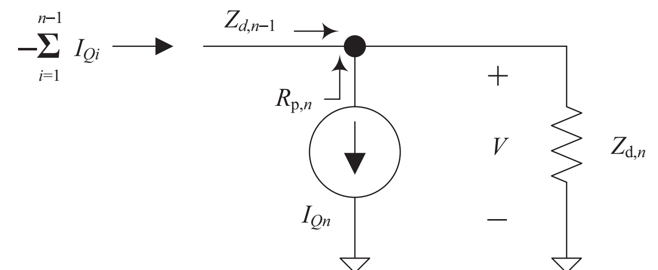



Fig. 7. Simplified DPA model using current source instead of transistor.

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For the latter case,

$$Z_{d,n} = \left(1 + \frac{n-1}{x}\right)^{-1} \frac{R_p(\Omega\cdot\text{mm})}{W_{Q_n}}, \text{ when} \\ I_{Q_n} = xI_1 \text{ and } I_{Q_i} = I_1 (1 \le i \le n-1). \quad (10)$$

In the conventional approach, gate capacitance tapering is applied to maintain the same voltage at the gate of each transistor by compensating the loss of the actual gate transmission line. The proposed scheme in this work makes gate voltages of the transistors near the output port larger compared with those the other transistors, which allows high characteristic impedances for the drain lines near the output port by the load modulation effect. From Fig. 3, the gate capacitance ($C_{gs}$) of the 4F 100-μm device without a parallel-RC network is estimated to be 1.2 pF at 17 GHz. $Z_{d,10}$ of the 10-stage NDPA with a uniform $C_{g,n}$ of 0.2 pF is calculated as 17.5 Ω from (9). If we change the value of $C_{g,10}$ from 0.2 pF to 0.6 pF, the drain current increment $x$ in (10) becomes 2.3, and $Z_{d,10}$ is obtained as 35.7 Ω.

Taking the ratio of the actual drain line impedance (30 Ω) to the estimated optimal load resistance (17 Ω) into account, the initial value of the gate coupling capacitance of the last three transistors is determined to be 0.6 pF, which is three times larger than $C_s$ in Fig. 2. This is tuned using a computer simulation. For a flat output power and efficiency even at a high-band edge, the gate coupling capacitors of the last three HEMT cells ($C_{g,8}$, $C_{g,9}$, and $C_{g,10}$) are adjusted to 0.62 pF, 0.9 pF, and 0.65 pF, respectively. A quarter-wavelength transformer is added at the output of the NDPA to transform the output impedance from 30 Ω to 50 Ω.

The proposed amplifier (case III) is compared with the amplifier having a uniform gate coupling capacitance (case I) and the amplifier having a gate coupling capacitance tapering (case II) in Fig. 8. The simulation results show that the load modulation through the intentional drain current increase of the last three transistors in case III improves the output power by 4.8 dB and 3.3 dB at 18 GHz, compared with case I and case II. The load modulation also improves the PAE by 13.1% and 10.3% at 18 GHz, respectively, compared with case I and case II.

The cascaded NDPA architecture is used to obtain a high gain and good return loss in a wide frequency range of operation. A schematic diagram of the designed two-stage NDPA is shown in Fig. 9. The power stage consists of one 6 × 100-μm HEMT ($Q_{21}$) and nine 4 × 100-μm HEMTs ($Q_{22}$ through $Q_{210}$), and the driver stage consists of one 6 × 100-μm HEMT ($Q_{11}$) and five 4 × 100-μm HEMTs ($Q_{12}$ through $Q_{16}$). The schematic circuit is designed using the values given in Fig. 6. The drain transmission line absorbs a frequency-limiting drain capacitance, and its length represents a series inductance in a distributed configuration. The length of the drain and gate transmission lines is tuned such that all the drain currents are combined in phase.

For a drain bias circuit with choke inductors, considering the current density limit, the width of double-layered bias lines and inductors should be greater than or equal to 70 μm. In addition, the first metal crossover line width of the choke inductor should be larger than 100 μm. The inductor design parameters such as the inductance or self-resonance frequency are determined to have a minimal impact on the low- and high-frequency performance of the NDPA. In the circuit design, three bonding wires with a length of 300 μm on the RF input and output pads are included in the simulations. The schematic design, including the drain transmission lines, gate transmission

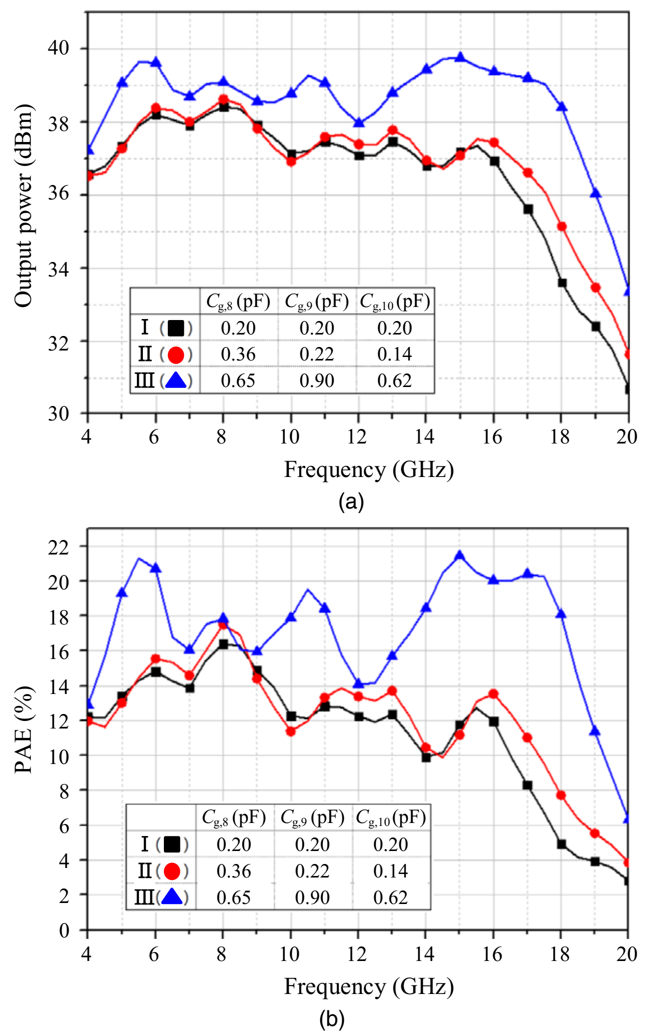


Fig. 8. Simulated output power and PAE of NDPA with variation of gate coupling capacitances at available input power of 27 dBm and $V_{DS}$ = 26 V: uniform (I), capacitance tapering (II), and load modulation (III) cases.

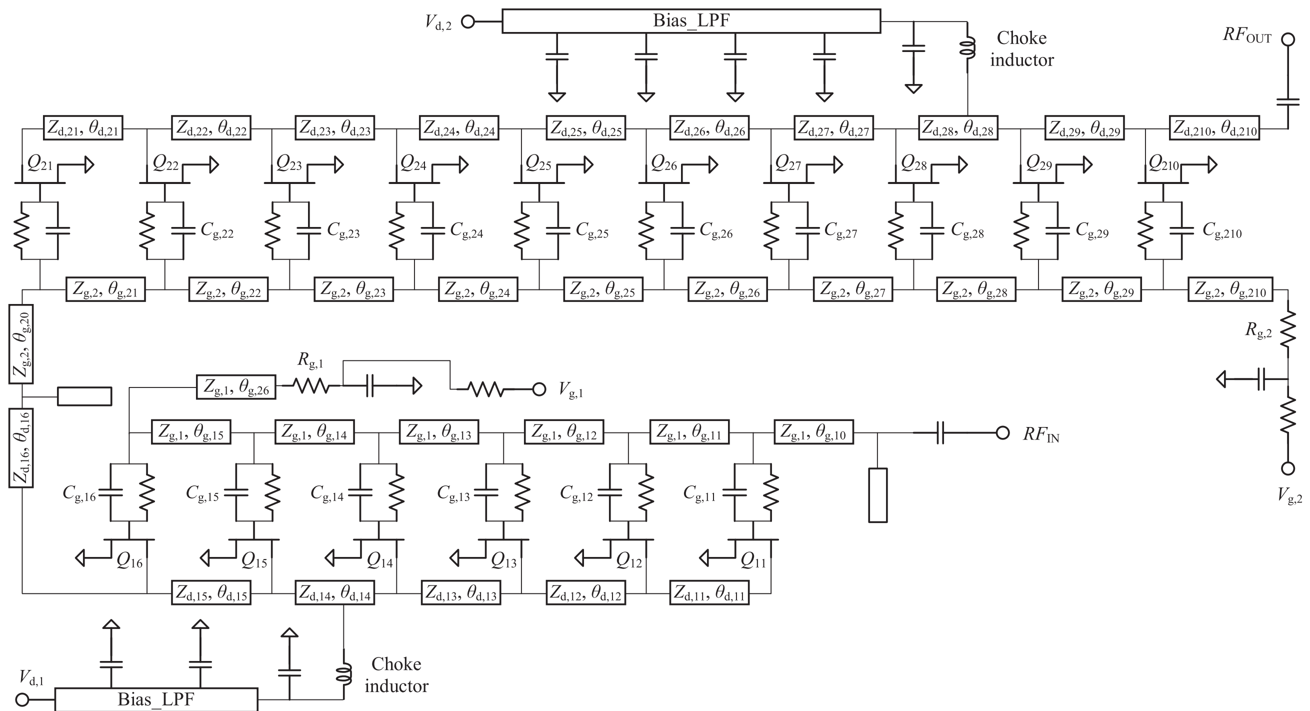


Fig. 9. Schematic diagram of cascaded NDPA MMIC.

lines, an output impedance transformer, and matching circuits, is electromagnetically simulated to include physical layout effects.

A photograph of the fabricated cascaded NDPA MMIC is shown in Fig. 10. The chip occupies an area of $5 \times 5$ mm$^2$ except for the test device area.

## IV. Measured Results

A test jig for the characterization of the NDPA MMIC is designed and fabricated as shown in Fig. 11. The MMIC is attached to a 2-mm-thick Cu/$Mo_{70}$Cu/Cu (CPC) carrier using an eutectic die attach process for an optimal heat sink. A circuit board including 50-Ω input/output microstrip lines and bias networks is attached to the carrier with a silver epoxy adhesive. The entire test circuit is made on an 8-mil-thick RO4003 substrate ($\varepsilon_r$ = 3.38) with Au-plated lines. The MMIC is connected to the circuit board using 18-μm-diameter gold bond wires, and the carrier is bolted to the test jig where 2.92-mm end launch connectors are installed.

The NDPA MMIC is nominally biased at a drain-source voltage of 26 V and a drain current of 600 mA for the measurement. To avoid thermal degradation, small- and large-signal performances of the NDPA MMIC are measured under a pulse-mode condition. A pulsed gate

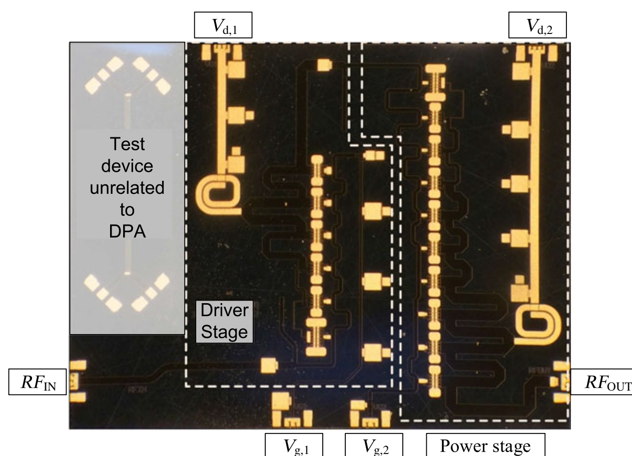


Fig. 10. Photograph of cascaded NDPA MMIC (dimensions of $5 \times 5$ mm$^2$, except for test device area).

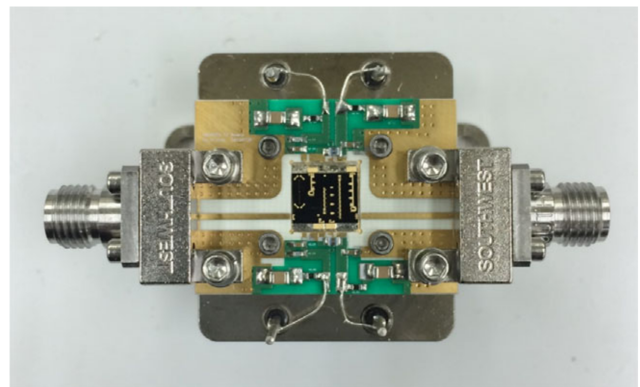


Fig. 11. NDPA MMIC mounted on test jig.

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bias voltage ($V_G$) of −6.0 V to −3.0 V is applied with a 10% duty cycle and 100-μs pulse width, whereas the drain-source bias voltage ($V_{DS}$) is constant.

Figure 12 shows the measured and simulated *S* parameters of the NDPA MMIC. The measured results (solid lines) are in good agreement with the simulation (dotted lines). The small-signal gain is 17.6 dB to 21.8 dB, and the input/output return loss is better than 10 dB from 6 GHz to 18 GHz when a 26-V drain-source voltage is applied.

The measured (solid lines) and simulated (dotted lines) large-signal results of the NDPA MMIC are shown over the bandwidth in Fig. 13 with an available input power of 27 dBm at a drain-source voltage of 26 V. From 6 GHz to 18 GHz, the output power is 39.4 dB to 40.3 dBm, the PAE is 17.0% to 21.8%, and the associated gain is 12.4 dB to 13.3 dB. It is noticeable that the load modulation effect maintains the small-signal and large-signal performance well up to 18 GHz.

Figure 14 shows the measured output power, PAE, and gain of the NDPA MMIC with the input power at 6 GHz to 18 GHz. Here, each line represents the data at a specific frequency of 6 GHz to 18 GHz, and the measurements are done with a step frequency of 1 GHz. The variations in the saturated output power and PAE with an available input power of 27 dBm are shown in Fig. 15 when the drain bias voltage is at 24 V, 26 V, and 28 V. The output power increases by about 0.4 dB when the drain voltage changes from 24 V to 26 V, whereas the PAE decreases by about 2.5% when the drain voltage moves from 28 V to 26 V. Considering output power, PAE, and reliable operation of the NDPA MMIC, the most desirable supply voltage is 26 V. With the same bias and input power conditions, the output power and PAE under CW

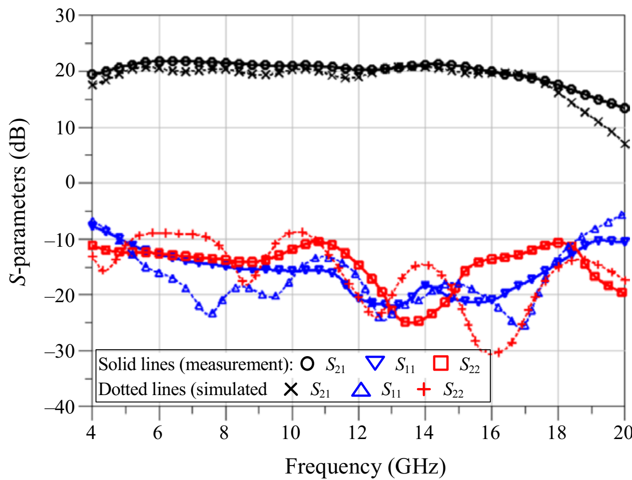


Fig. 12. Measured and simulated *S* parameters of NDPA MMIC.

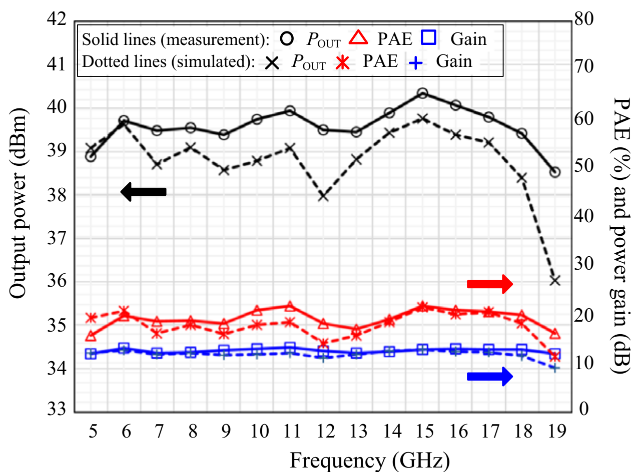


Fig. 13. Measured (solid lines) and simulated (dotted lines) large- signal performance of NDPA MMIC with available input power of 27 dBm at $V_D$ = 26 V.

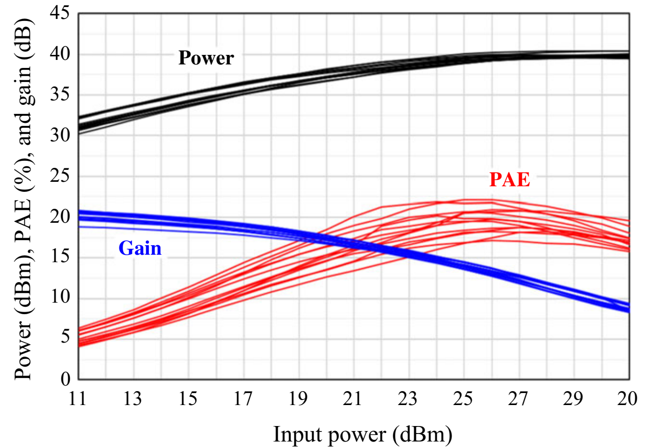


Fig. 14. Measured output power, PAE, and gain of NDPA MMIC with input power of 6 GHz–18 GHz.

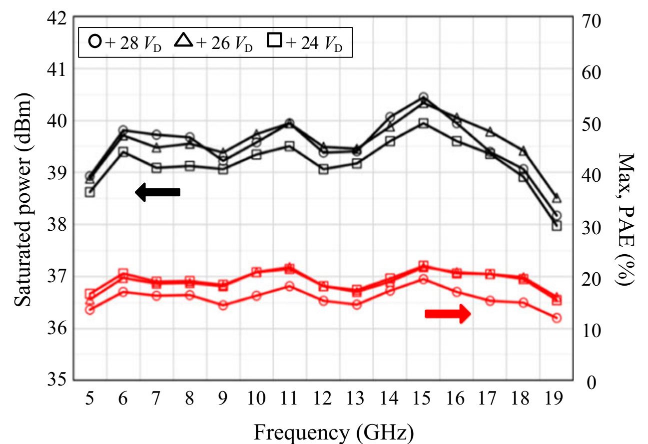


Fig. 15. Measured output power and PAE with available input power of 27 dBm when drain-source voltage is 24 V, 26 V, and 28 V.

Table 1. Comparison of wideband power amplifier MMICs fabricated using the 0.25-μm GaN HEMT process.

| Ref. | Topology | Freq. (GHz) | Mode | Small signal gain (dB) | PSAT (W) | Power gain (dB) | PAE (%) | Input return loss (max., dB) | VD (V) | Area ($mm^2$) |
|---|---|---|---|---|---|---|---|---|---|---|
| [11] | 2-stage Balanced RMA* | 6–18 | CW | 20–29 | 11–20 | 13–16 | 10–23 | 15 | 30 | 27.5 |
| [12] | 3-stage RMA | 6–18 | CW | 18–23 | 5.6–10 | 15–18 | 13–26 | 5 | 25 | 19.8 |
| [13] | 3-stage RMA | 6–18 | Pulse | 19–28 | 9–13.5 | 9–14 | 10–24.5 | 9 | 28 | 19.25 |
| [10] | 1-stage NDPA | 1.5–17 | CW | 10–14 | 8–13 | 7–9 | 20–38 | 8 | 30 | 15.34 |
| [14] | 2-stage Balanced NDPA | 6–18 | Pulse | 8–10 | 10–13.5 | 4–5† | 13–20 | 18 | 40 | 18.72 |
| [15] | 2-stage NDPA | 6–18 | CW | 10–15 | 6–10 | 5.1–8.1 | 7.4–16 | 9 | 36 | 6.7 |
| This work | 2-stage NDPA | 6–18 | Pulse | 18–20 | 9–11 | 12–13.3 | 17–22 | 10 | 26 | 25 |

*RMA, reactive matched amplifier.
†This data is estimated from the graph of Reference.

operation show a reduction of about 0.6 dB and 1.6%, respectively.

Some state-of-the-art wideband power amplifier MMICs fabricated using the 0.25-μm GaN HEMT process showed a saturated output power of 6 W to 20 W and a PAE of 8% to 25%, as summarized in Table 1. From the viewpoint of the flatness and compromised performance of the output power and PAE across the 6-to-18 GHz frequency range, it appears clearly from Table 1 that our NDPA MMIC is very competitive with the state-of-the-art results. Moreover, it is notable that the return loss is better than or equal to 10 dB over a frequency band of 6 GHz to 18 GHz. Therefore, our proposed load modulation scheme is successfully applied and is demonstrated to be very effective for the distributed GaN HEMT power amplifier MMIC.

## V. Conclusion

A 6-GHz-to-18-GHz cascaded nonuniform distributed power amplifier MMIC with load modulation through increased gate coupling capacitance was demonstrated using an industrial 0.25-μm AlGaN/GaN HEMT process, and its measurement results were presented. The NDPA MMIC features a flat output power and PAE performance up to the maximum frequency of the bandwidth. The measured results showed a saturated output power of 39.5 (9 W) to 40.4 dBm (11 W) with an associated PAE of 17% to 22%, and an input/output return loss of more than 10 dB within 6 GHz to 18 GHz. A flat small-signal gain of 18 dB to 20 dB was also obtained through a cascaded structure.

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