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Current Harmonics Rejection and Improvement of Inverter-Side Current Control for the *LCL* Filters in Grid-Connected Applications

Jinming Xu†, Shaojun Xie*, and Binfeng Zhang*

†,*College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing, China

Abstract

For grid-connected *LCL*-filtered inverters, the inverter-side current can be used as the control object with one current sensor for both *LCL* resonance damping and over-current protection, while the grid-voltage feedforward or harmonic resonant compensator is used for suppressing low-order grid current harmonics. However, it was found that the grid current harmonics were high and often beyond the standard limitations with this control. The limitations of the inverter-side current control in suppressing low-order grid current harmonics are analyzed through inverter output impedance modeling. No matter which compensator is used, the maximum magnitudes of the inverter output impedance at lower frequencies are closely related to the *LCL* parameters and are decreased by increasing the control delay. Then, to improve the grid current quality without complicating the control or design, this study proposes designing the filter capacitance considering the current harmonic constraint and using a PWM mode with a short control delay. Test results have confirmed the limitation and verified the performance of the improved approaches.

Key words: Grid current harmonics rejection, Inverter-side current control, *LCL* filter

I. INTRODUCTION

The grid-connected inverter is widely used in distributed power generations, and an *LCL* filter is used to suppress the switching harmonics caused by the pulse width modulation (PWM) [1]-[4]. Depending on the current sensor location, the current control for an *LCL*-filtered inverter consists of grid current control [5]-[7], and inverter-side current control [8]-[10]. Both of them are available in practical applications [11], [12]. Since the inverter-side current control is capable of limiting the current in the inverter-side inductor, over current protection can be realized both for the switching devices and the inductor [8]-[12]. Even though inverter-side current control drew a lot of attention due to its use of fewer sensors, two major tasks should be carried out by inverter-side current control, i.e., the damping of *LCL* resonance and the suppression of low-order grid current harmonics.

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†Corresponding Author: xjinming01@163.com
Tel.: +86 13913391056, Nanjing Univ. of Aeronautics and Astronautics
*College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, China

For the *LCL*-resonance damping, if the control delay is ignored, the system is stable [8], [9]. However, the delay in a digital control system could not be ignored. The phase lag caused by the control delay considerably affected the stability [10]-[12]. If a one-sample delay exists, the system is stable when the *LCL* resonance frequency is far lower than the control frequency [12]. In the case of instability, an active damping (AD) was usually used to achieve higher flexibility and efficiency, when compared with the passive damping in [13]. The existing AD techniques fall into two categories, i.e., feedback-based AD (i.e., with additional feedbacks) and filtered-based AD (i.e., with a digital filter) [14]-[17]. For the feedback-based AD, more current or voltage variables have to be measured or estimated. To reduce the number of sensors in the industry, J. Dannehl et al. recommended the AD in [14]. With notch filter AD, the resonance was highly damped [14]-[16].

For suppressing the low-order harmonics, the grid-voltage feedforward and harmonic resonant controller are well known in *L*-filtered applications. There have been a lot of studies on the current harmonics rejection of *LCL*-filtered inverters with the grid current control applying two harmonic compensators

[18]-[26]. The proportional voltage feedforward in [18] and [19], the feedforward with high-order derivative functions in [20] and [21], and the band-pass filter based feedforward in [22] were applied in the grid current control. Grid current control using a resonant controller was also shown to assure a high-quality grid current [23]-[26]. However, things are different for inverter-side current control. As shown in the studies of inverter-side current control [8]-[12], [14]-[16], [27]-[29], at a light power or with a distorted grid voltage, the grid current was greatly distorted even with a feedforward and/or resonant controller. Although there are many studies on the grid current harmonics rejection with the inverter-side current control, the reason for poor grid current quality was not clear.

As can be seen from the above studies, for inverter-side current control, although the *LCL* resonance is solved based on the studies in [10]-[17], the low-order harmonics rejection has yet to be well accomplished. Since the grid current is indirectly controlled by the inverter-side current feedback, it is worth wondering whether the grid-voltage feedforward and harmonic resonant controller are still capable of suppressing grid current harmonics. This study aims to improve the performance with inverter-side current control. First, based on the inverter output impedance model, the impact of the grid voltage distortion on the grid current quality with inverter-side current control is analyzed. For the first time, the reason the typical inverter-side current control with grid-voltage feedforward and/or harmonic resonant controller cannot highly suppress the low-order grid current harmonics is explained in detail through theoretical analysis. Based on an analysis of the reason for the grid current distortion with inverter-side current control, two simple approaches capable of improving the grid current quality are proposed and tested on an inverter prototype.

II. System Description and Modeling

A. Grid-Connected LCL-Filtered Inverter

As shown in Fig. 1, the *LCL* filter includes an inverter-side inductor L_1, a capacitor C_1 and a grid-side inductor L_2. U_{dc} denotes the dc-link voltage, u_{inv} is the inverter output voltage, i_{L1} and i_g are the inverter-side current and the grid current, and u_g is the grid voltage. In practice, U_{dc} can be a renewable energy source or the output of a MPPT converter. The current reference i_{ref} is generated by the dc-link voltage control and the phase-locked loop. The grid voltage and inverter-side current are sampled to facilitate the control and to generate the PWM reference u_m.

The transfer function from u_{inv} to i_{L1} is:

$$G_{u_{inv}}^{i_{L1}}(s)=\frac{L_2C_1s^2+1}{L_1L_2C_1s^3+(L_1+L_2)s} \tag{1}$$

The *LCL* resonance frequency ω_{res} is:

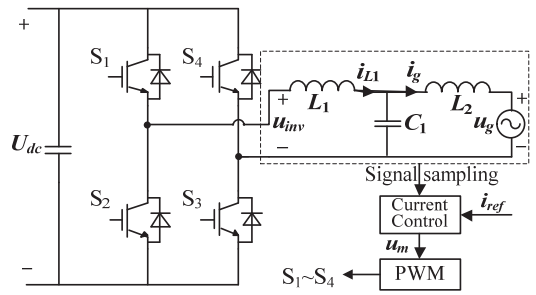


Fig. 1. Grid-connected *LCL*-filtered inverter.

TABLE I
System Parameters

Symbol	Description	Value (per unit)
U_g	Grid voltage (RMS)	220 V
f_0	Grid frequency	50 Hz
U_{dc}	DC-link voltage	380 V
P	Rated output power	5 kW
f_s	Control/switching frequency	15 kHz
L_1	Inverter-side inductance	0.6 mH (1.95%)
L_2	Grid-side inductance	0.36 mH (1.17%)
C_1	Filter capacitance	7 μF (2.13%)

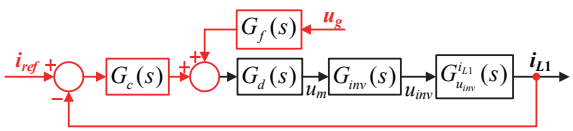


Fig. 2. Typical inverter-side current control.

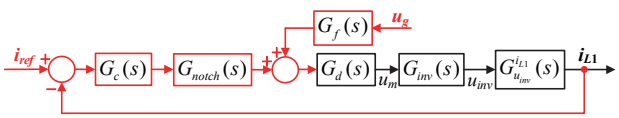


Fig. 3. Inverter-side current control with filter-based AD.

$$\omega_{res}=\sqrt{\frac{L_1+L_2}{L_1L_2C_1}} \tag{2}$$

The default parameters are shown in Table I. Note that the design of the *LCL* parameters is not the main theme of this study and will not be discussed here.

B. Inverter-Side Current Feedback Control

The typical inverter-side current control is shown in Fig. 2, where $G_c(s)$ is the current controller, $G_f(s)$ is the grid-voltage feedforward factor, and $G_d(s)$ denotes the computation delay between the sampling of i_{L1} and the reloading of u_m:

$$G_d(s)=e^{-sT} \tag{3}$$

where T is the delay time. If the sampling is at the beginning of the control period and the reloading of u_m is at the end of the control period, the delay is one period, and it is named one-sample delay (T=T_s=1/f_s) [9]. In addition, $G_{inv}(s)$ behaves like a zero-order holder (ZOH):

$$G_{inv}(s)=\frac{1}{T_s}\cdot\frac{1-e^{-sT_s}}{s}\cdot k_{\mathrm{PWM}}\approx k_{\mathrm{PWM}}e^{-sT_s/2} \tag{4}$$

where k_{PWM} is equal to U_{dc}/U_{tri} and U_{tri} is the amplitude of the triangular carrier.

For $G_c(s)$, the proportional-integral (PI) controller is:

$$G_{PI}(s)=k_p(1+\frac{1}{T_i s}) \tag{5}$$

where k_p and T_i are the proportional gain and the time constant. In this study, the PI parameters are tuned by the symmetrical optimum [12], i.e., $k_{PWM}k_p$=7.2, T_i=0.0006. An analysis in MATLAB shows that the current control in Fig. 2 works stably if $G_d(s)$ is equal to 1 (i.e., T=0). The phase margin (PM) at the lowest 0dB-crossing frequency is 66°, while the gain margin (GM) is 6.5dB. However, considering the one-sample delay, the system is unstable because the phase crosses −180° at that frequency with a gain above 0dB [11], [14], [29]. Hence, to solve the instability in the case of $T=T_s$, the filter-based AD with a notch filter has been suggested [12], [14]-[16]. Its structure is shown in Fig. 3 and the notch filter is:

$$G_{notch}(s)=\frac{s^2+2\zeta_z\omega_{res}s+\omega_{res}^2}{s^2+2\zeta_p\omega_{res}s+\omega_{res}^2} \tag{6}$$

where ζ_z and ζ_p are the damping factors. The notch filter is implemented by a Tustin approximation with frequency pre-warping [14], which guarantees a good performance.

Fig. 4 shows open-loop Bode plots with the control in Fig. 3 for different values of ζ_p (i.e., 0.3, 0.5, 0.7 and 0.9) while ζ_z is 0.01 and $k_{PWM}k_p$ is 7.2. The system is stable with the AD. The PM ranges from 16° to 28° and the GM ranges from 3.0dB to 4.5dB. Reducing k_p and increasing T_i help improve the margins. For instance, if $k_{PWM}k_p$ is 4.3 and T_i increases to 0.001, the PM increases from 20° to 44° and the GM increases from 3.5dB to 8.7dB, in the case of ζ_p=0.7.

The control in Fig. 2 and the filter-based AD in Fig. 3 are denoted as Strategy 1 and Strategy 2, respectively. Based on the above analysis, for T=0, Strategy 1 is sufficient. However, for $T=T_s$, Strategy 2 is required for better stability.

C. Common Approaches to Suppress Low-Order Grid Current Harmonics

A proportional-resonant (PR) controller centered at the fundamental and the 3rd~11th odd harmonic frequencies is:

$$G_{PR}(s)=k_p+\sum_{n=1,3,...,11}\frac{k_r s}{s^2+\omega_c s+(n\omega_0)^2} \tag{7}$$

where ω_0 is equal to $2\pi f_0$, n is the order of the harmonic that needs to be suppressed, ω_c denotes the bandwidth of the resonant control, and k_r/ω_c is the resonant gain at $n\omega_0$. In [23]-[26] where the design of the PR controller is emphasized, ω_c is 6, and changing k_r changes the PR gain at $n\omega_0$.

Because grid voltage distortion is a major cause of the grid current distortion, grid-voltage feedforward is also considered as a promising approach to improve the grid current quality. For the purpose of simple implementation and high reliability in the industry, proportional grid-voltage feedforward is discussed, i.e., $G_f(s)=1/k_{PWM}$.

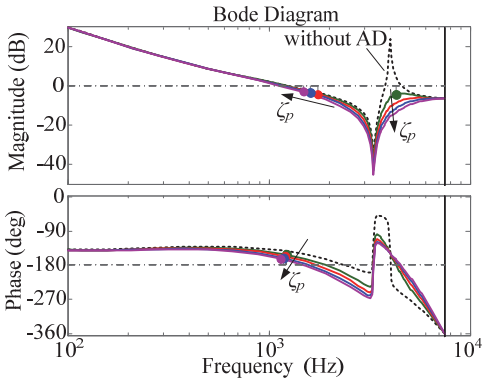


Fig. 4. Open-loop bode plots with a filter-based AD control for one-sample delay and different damping factors ζ_p.

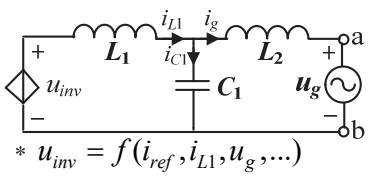


Fig. 5. Structure of current-controlled *LCL*-filtered inverter.

D. Inverter Output Impedance Model

The impact of u_g on i_g is studied with the use of the inverter output impedance model. The current-controlled inverter in Fig. 1 is depicted in Fig. 5, where u_{inv} is a dependent voltage source related to the current control.

The expression of u_{inv} with Strategy 1 in the case of T=0 is:

$$u_{inv}=\left[\left(i_{ref}-i_{L1}\right)G_c(s)+u_g G_f(s)\right]G_{inv}(s) \tag{8}$$

In addition, u_{inv} with Strategy 2 in the case of $T=T_s$ is:

$$u_{inv}=\left[\left(i_{ref}-i_{L1}\right)G_c(s)G_{notch}(s)+u_g G_f(s)\right]G_d(s)G_{inv}(s) \tag{9}$$

According to Kirchhoff's law:

$$\begin{cases} u_{inv}=L_1 s\cdot i_{L1}+L_2 s\cdot i_g+u_g \\ \dfrac{1}{C_1 s}\cdot i_{C1}=L_2 s\cdot i_g+u_g \\ i_{L1}=i_g+i_{C1} \end{cases} \tag{10}$$

Using (8) and (10), the output impedance in Fig. 5 at port a-b with Strategy 1 in the case of T=0 is:

$$Z_{out1}=\frac{L_1L_2C_1s^3+G_c(s)G_{inv}(s)L_2C_1s^2+(L_1+L_2)s+G_c(s)G_{inv}(s)}{L_1C_1s^2+G_c(s)G_{inv}(s)C_1s+1-G_f(s)G_{inv}(s)} \tag{11}$$

Similarly, using (9) and (10), the output impedance at port a-b with Strategy 2 in the case of $T=T_s$ is:

$$Z_{out2}=\frac{\left[\begin{array}{l}L_1L_2C_1s^3+G_c(s)G_{notch}(s)G_d(s)G_{inv}(s)L_2C_1s^2+\\(L_1+L_2)s+G_c(s)G_{notch}(s)G_d(s)G_{inv}(s)\end{array}\right]}{\left[\begin{array}{l}L_1C_1s^2+G_c(s)G_{notch}(s)G_d(s)G_{inv}(s)C_1s+\\1-G_f(s)G_d(s)G_{inv}(s)\end{array}\right]} \tag{12}$$

It should be mentioned that the larger the magnitude of the

inverter output impedance at $n\omega_0$ is, the smaller the n-order grid current harmonic value becomes. In the next sections, performance will be evaluated on the basis of (11) and (12).

III. Investigations of Low-Order Grid Current Harmonics Rejections

A. Performances without harmonic compensators

For Strategy 1 in the case of T=0, if $G_f(s)$ is 0 and (5) is used, (11) changes to:

$$Z_{out1\_PI} = L_2 s + \frac{1}{C_1 s}\left[1 - \frac{1}{L_1 C_1 s^2 + G_{PI}(s) G_{inv}(s) C_1 s + 1}\right] \quad (13)$$

First of all, $L_1C_1s^2$ can be neglected at low frequencies and the phase lag caused by $G_{inv}(s)$ is negligible. In addition, for PI, $G_{PI}(s)$ is seen as $k_p/(T_i s)$ at frequencies below $1/T_i$, while it is k_p at frequencies above $1/T_i$. Therefore, $G_{PI}(s)G_{inv}(s)C_1s$ can be seen as a proportional factor at frequencies below $1/T_i$, while it is an imaginary factor at frequencies above $1/T_i$. Hence, the values of the term in the square brackets (i.e., $G_{PI}(s)G_{inv}(s)C_1s/(G_{PI}(s)G_{inv}(s)C_1s+1)$) grow with an increase in the PI gain. However, the PI gain is strictly limited. Hence, $|Z_{out1\_PI}|$ at low frequencies satisfies:

$$\left|Z_{out1\_PI}\right| << \left|Z_{out\_max}\right| = \left|L_2 s + \frac{1}{C_1 s}\right| \quad (14)$$

For Strategy 2 in the case of T=T_s, (12) is rewritten as:

$$Z_{out2\_PI} = L_2 s + \frac{1}{C_1 s}\left\{1 - \frac{1}{\left[L_1 C_1 s^2 + G_{PI}(s) G_{notch}(s) \cdot G_d(s) G_{inv}(s) C_1 s + 1\right]}\right\} \quad (15)$$

Due to the limited PI gain, the magnitudes of Z_{out2_PI} at low frequencies are much smaller than $|Z_{out\_max}|$, i.e., $|Z_{out2\_PI}|<<|Z_{out\_max}|$. Thus, the grid current quality without the harmonic compensators is poor even if u_g is slightly distorted.

Fig. 6 shows some inverter output impedance magnitude plots with only the PI in different cases. Although the inverter output impedance magnitudes increase with and an increasing k_p or with a reducing T_i, the magnitudes at low frequencies (e.g., 0.1~1 kHz) are limited. In addition, it is seen from Figs. 6(a) and 6(b) that the one-sample delay results in poor performance for two main reasons:

1) If T is 0, (15) approximates to (13) because the notch filter in (6) can be seen as 1 at a frequency that is much smaller than ω_{res}. However, with the one-sample delay (i.e., T=T_s), $G_d(j\omega)$ has an imaginary part which makes the gain response of the denominator in the square brackets of (15) different from that of (13). Therefore, even with the same PI parameters, the one-sample delay changes the inverter output impedance magnitudes, as shown in Figs. 6(a) and 6(b), from 0.2 to 1 kHz.
2) The one-sample delay causes an extra lag in the open-loop phase. Therefore, control stability is endangered so that a notch filter is needed. However, the notch filter also causes an extra lag in the open-loop phase, as indicated by Fig. 4. Then, the PI parameters for Strategy 2 must be reduced to improve the phase margin. As a result, the inverter output impedance magnitudes at low frequencies with Strategy 2 are further reduced.

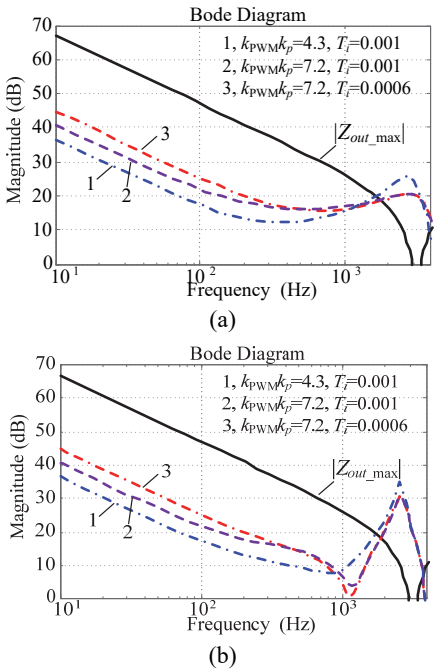


Fig. 6. Inverter output impedance magnitude plots with only the PI for: (a) Strategy 1 (T=0); (b) Strategy 2 (T=T_s).

B. Performances with the Grid-Voltage Feedforward

With the proportional grid-voltage feedforward (PGF), the following equation is fulfilled at low frequencies:

$$\begin{aligned} &1 - G_f(j\omega) G_{inv}(j\omega) = 1 - G_{inv}(j\omega)/k_{PWM} \\ &\approx 1 - \cos(\omega T_s/2) + j\sin(\omega T_s/2) \approx j\sin(\omega T_s/2) \end{aligned} \quad (16)$$

where $\omega T_s/2$ is so small (e.g., 12° at 1 kHz) that its cosine value is approximately equal to 1. Then, it is obtained that:

$$\begin{aligned} &\left|L_1 C_1 s^2 + G_{PI}(s) G_{inv}(s) C_1 s + 1 - G_{inv}(s)/k_{PWM}\right| \\ &\approx \left|L_1 C_1 s^2 + G_{PI}(s) G_{inv}(s) C_1 s\right| \end{aligned} \quad (17)$$

Using (11) and (17), the impedance magnitudes at low frequencies with Strategy 1 with the PI and PGF satisfy:

$$\left|Z_{out1\_PI\&PGF}\right| \approx \left|L_2 s + \frac{1}{C_1 s}\left[1 + \frac{L_2 s}{L_1 s + G_{PI}(s) G_{inv}(s)}\right]\right| \quad (18)$$

Generally, for an L or LCL filter whose inductance is L_1+L_2, the 0dB-crossing frequency should be designed above the frequencies of the low-order harmonics in order to suppress the current harmonics. It is deduced that at low frequencies:

$$\left|\frac{G_{PI}(s) G_{inv}(s)}{(L_1 + L_2)s}\right| > 1 \quad (19)$$

where the left side grows much higher than 1 by decreasing the frequency. Thus, at low frequencies, it is obtained that:

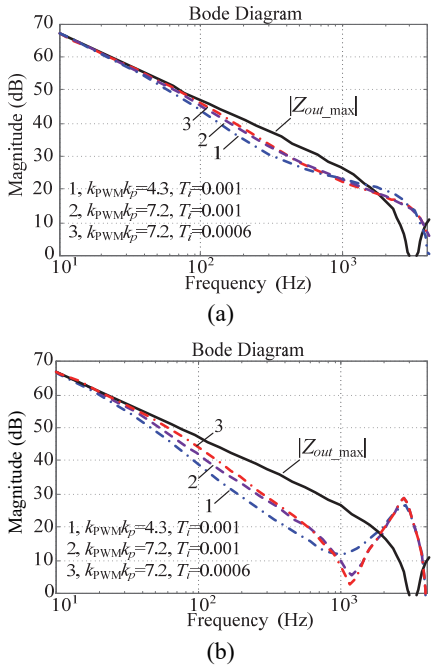


Fig. 7. Inverter output impedance magnitude plots with PGF+PI for: (a) Strategy 1 (T=0); (b) Strategy 2 (T=T_s).

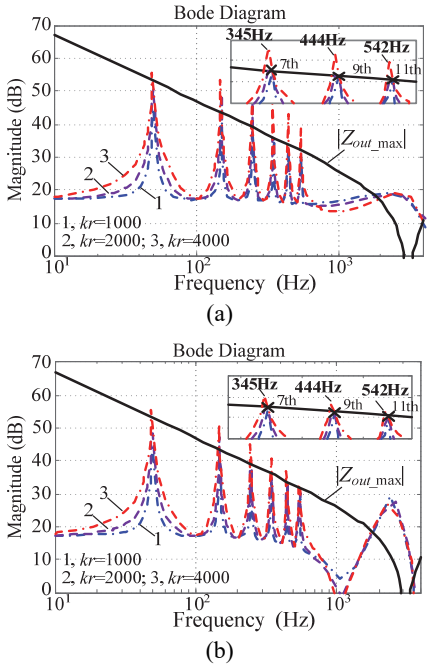


Fig. 8. Inverter output impedance magnitude plots with the PR for: (a) Strategy 1 (T=0); (b) Strategy 2 (T=T_s).

$$\left|Z_{out1\_PI\&PGF}\right| < \left|Z_{out\_max}\right| \tag{20}$$

Similarly, for Strategy 2, it is also deduced that $|Z_{out2\_PI\&PGF}|$ is lower than $|Z_{out\_max}|$ at low frequencies.

To prove the correctness of the above analysis, Figs. 7(a) and 7(b) give inverter output impedance plots with the PGF and PI. For comparisons, the PI parameters are the same as those in Fig. 6. Compared with Fig. 6, the impedance magnitudes at low frequencies are greatly increased. In addition, the impedance magnitudes change slightly when the PI parameters vary. As a result, once the PGF is used, the grid current quality with the inverter-side current PI control is improved. However, it has limitations because of $|Z_{out\_max}|$. In addition, as can be seen from the curves with the same PI parameters in Figs. 6(a) and 6(b), the one-sample computation delay weakens the performance in suppressing low-order grid current harmonics for the same reasons explained in Section III-A.

C. Performances with the Harmonic Resonant Controller

Note that the PR gain in (7) at $n\omega_0$ is actually a constant, i.e., k_p+k_r/ω_c. For Strategy 1, when $G_f(s)$ is 0 and (7) is used, the inverter output impedance at $n\omega_0$ is rewritten as:

$$Z_{out1\_PR} = L_2 s + \frac{1}{C_1 s}\left\{1 - \frac{1}{\left[L_1C_1s^2 + (k_p + k_r/\omega_c)\cdot G_{inv}(s)C_1 s + 1\right]}\right\} \tag{21}$$

It is noted that increasing k_r can make the PR gain at $n\omega_0$ much higher than PI. Thus, with a high PR gain, the values of the term in the braces in (21) are approximately 1 at $n\omega_0$. $|Z_{out1\_PR}|$ at $n\omega_0$ is approximately equal to $|Z_{out\_max}|$.

Similarly, for Strategy 2, $|Z_{out2\_PR}|$ at $n\omega_0$ is approximately equal to $|Z_{out\_max}|$, in the case of a high PR gain.

As can be seen from Fig. 8, the inverter output impedance magnitude at $n\omega_0$ with the PR is kept invariant and cannot exceed the maximum value even if a larger k_r is used. With a larger k_r, it is true that the peaks are all heightened. However, the frequencies centered at the peaks are no longer the n-order grid-harmonic frequencies. In addition, the curves in Figs. 8(a) and 8(b) indicate that the one-sample delay yields a poorer performance in suppressing the grid current harmonics at certain frequencies (e.g., 13th, 15th ...) where the harmonic resonant controller is not located.

D. Performances with both the Grid-Voltage Feedforward and Harmonic Resonant Controller

As analyzed above, with either the PGF or PR, the inverter output impedance magnitudes at grid-harmonic frequencies are always below their maximums. This section evaluates if the use of both the PGF and PR can break this limitation.

Given that the gain of the PR at $n\omega_0$ is much higher than that of the PI, the same as (17) for the PI and PGF, the following equation for the PR and PGF at $n\omega_0$ is satisfied:

$$\begin{aligned}&\left|L_1C_1s^2 + G_{PR}(s)G_{inv}(s)C_1s + 1 - G_{inv}(s)/k_{PWM}\right| \\ &\approx \left|L_1C_1s^2 + G_{PR}(s)G_{inv}(s)C_1s\right|\end{aligned} \tag{22}$$

In addition, unlike (19) for the PI, $|G_{PR}(s)G_{inv}(s)|$ at $n\omega_0$ is far higher than $|(L_1+L_2)s|$. Thus, for Strategy 1 with both the PGF and PR, it is obtained that:

$$\left|Z_{out1\_PR\&PGF}\right| \approx \left|Z_{out\_max}\right| \tag{23}$$

Similarly, for Strategy 2, it is obtained that $|Z_{out2\_PR\&PGF}|$ at $n\omega_0$ is approximately equal to $|Z_{out\_max}|$.

Figs. 9(a) and 9(b) show some inverter output impedance magnitude plots with both the PGF and PR. Compared with Figs. 6 and 7, the output impedance magnitudes at the 3rd~11th odd frequencies are increased so that the grid current quality is improved. Compared with Figs. 8(a) and 8(b), the higher magnitudes at other frequencies indicate a better performance in suppressing the grid current harmonics. However, the limitations of the impedance magnitudes are still clearly noticed. Thus, even when two compensators are used together in the inverter-side current control, the grid current quality is surely improved, but the improvement is limited due to the maximum impedance values. Note that a poorer performance is also caused by the computation delay.

E. Summary

Basically, two conclusions are obtained.

1) The grid-voltage feedforward and harmonic resonant controller both help to improve the grid current quality with the inverter-side current control. However, because the inverter output impedance magnitudes at low-order grid-harmonic frequencies always have maximum values $|Z_{out\_max}|$, the low-order grid current harmonics induced by the grid voltage distortion cannot be lower than the magnitudes of the low-order grid voltage harmonics divided by the maximum impedance values.
2) The computation delay is harmful to the grid current quality. First, the stability is endangered by the phase delay so that k_p has to be reduced to improve stability although the notch filter AD is adopted. In addition, the PR controller causes more grid current harmonics due to the decreased PM produced by the delay and PR. Moreover, the delay also causes a decrease in the output impedance magnitudes. As a result, a reduction in the grid current quality is produced in the case of a larger delay.

In summary, the delay, compensators and *LCL* parameters all affect the suppression of low-order grid current harmonics. In past studies, inverters with the inverter-side current control generated a lot of grid current harmonics because the inverter was not properly designed since there was a lack in understanding the relation among the low-order grid current harmonics rejection, the control delay and *LCL* parameters. It is necessary to take serious considerations of such relations when finding approaches to improve the grid current quality with inverter-side current control.

IV. Discussions and Improved Approaches in Practical Applications

A. Constraint for LCL-Filter Parameter Design

According to the analysis in Section III, the maximum magnitudes $|Z_{out\_max}|$ at low frequencies are mainly determined by the capacitance of the *LCL* filter, even with

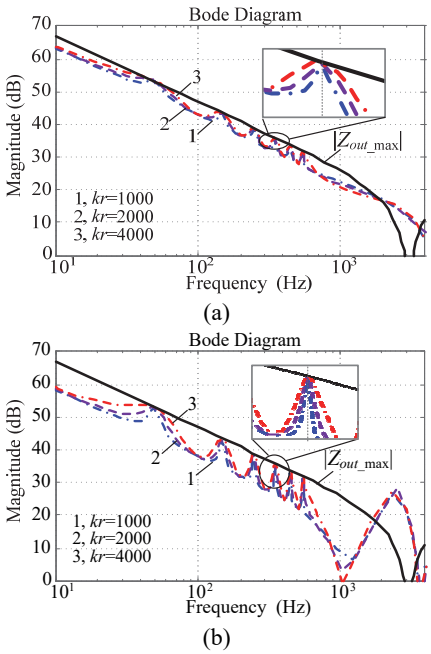


Fig. 9. Inverter output impedance magnitude plots with the PGF+PR for: (a) Strategy 1 (T=0); (b) Strategy 2 (T=T_s).

harmonic compensators. Denote the ratio of the *n*-order harmonic and fundamental values in the grid voltage as λ_n%. The minimal percentage of the *n*-order harmonic distortion level in i_g, caused by the distortion of u_g, is approximately expressed as:

$$D_n\% = \frac{n\omega_0 C_1 U_g}{I_g} \cdot \lambda_n\% \tag{24}$$

where I_g is the RMS value of i_g. This equation indicates the maximum ability of the inverter-side current control in suppressing low-order grid current harmonics caused by grid voltage distortions. In applications where the *n*-order grid voltage distortion λ_n% is known or measured in advance, the typical inverter-side current control is applicable only if the value of D_n%, determined by (24), does not exceed the distortion limit (D_{n_limit}%) in standards like IEEE std 929-2000 (also 1547.2-2008). In other words, (24) determines the maximum value of C_1 in the practical applications, i.e.,

$$C_1 < C_{1\_max} = \min\left\{\frac{I_g D_{3\_limit}}{3\omega_0 U_g \lambda_3}, \frac{I_g D_{5\_limit}}{5\omega_0 U_g \lambda_5}, \frac{I_g D_{7\_limit}}{7\omega_0 U_g \lambda_7}, \ldots\right\} \tag{25}$$

During the inverter operation, non-ideal factors such as the dead-time and parasitic parameters can also cause some low-order harmonics so that the grid current quality gets even poorer. Adopting an *n*-order resonant controller helps to improve the grid current quality. However, it can only make the *n*-order grid current harmonic close to the minimum value expressed in (24). Seen from (24), decreasing C_1 makes the *n*-order current harmonic further reduced. It should be noted that, if C_1 is decreased but L_1 and L_2 are unchanged, the ability of the switching harmonics rejection becomes poor. Thus, in the case of a smaller value of C_1, a larger inductance

has to be used for the purpose of suppressing the switching harmonics in the grid current (i.e., below 0.3%). In other words, if the grid voltage is badly distorted, a trade-off has to be made when designing a small value of C_1. Otherwise, if C_1 is not reduced, the typical strategies with harmonic compensators in Figs. 2 and 3 are no longer suitable, and different kinds of current control should be used.

Based on the above thought, the available range of C_1 for the inverter-side current control is determined and this study proposes to take the criterion of C_1 in (25) into account when designing the *LCL* parameters. An example is illustrated here. In IEEE std 929-2000, the 11th current harmonic limit is 2% at full power, i.e., D_{11_limit}=2. If the value of λ_{11}% in the application can increase up to 5%, C_1 must be smaller than 12 μF according to (25) for U_g=220 V, P=5 kW and ω_0=100π *rad*/*s*.

B. Computation Delay Issue

Based on the analysis in Section III-E, for the inverter-side current control, the computation delay should be shortened or compensated in order to make the inverter output impedance magnitudes close to $|Z_{out\_max}|$ at low frequencies. Thus, the digital PWM needs to be selected properly. Typically, there are two simple PWM implementations in a digital signal processor (DSP) at a control frequency of f_s, as shown in Fig. 10. The triangle carrier is either asymmetrical or symmetrical. The signal sampling is enabled at the beginning of the control period (i.e., when the counter is 0), while the PWM reference is reloaded at the top of the triangle carrier (i.e., when the counter reaches the value of the period register). In Fig. 10(a), the computation delay T is equal to T_s. However, in Fig. 10(b), T is reduced to $0.5T_s$. The digital implementation in Fig. 10(b) is the simplest way to reduce the computation delay, which is why it is suggested. It should be noted that there are also several other ways, such as increasing the control frequency, adjusting the sampling instant and so on [30].

IV. Test Results

Test results are provided to verify the above analysis and the improved approaches. A single-phase inverter is built in Saber simulator. The dc side is a 380V voltage source and the grid voltage is 220V/50Hz. In addition, a non-isolated grid-connected inverter is also built in the lab based on a DSP TMS320F28035. The power switches are IGBTs IKW40N120T2 from Infineon. The dc-link is rectified from a three-phase grid voltage, while the ac side is a commercial 220V/50Hz grid. During the entire test, the system parameters are the same as those in Table 1, except that C_1 is changed. The control parameters can be found in Section II.

A. Tests for T=0 (Simulation)

For T=0, an inverter with Strategy 1 is tested. The *LCL* and controller parameters are the same as those in Section II. In the test, an 11th harmonic voltage with a magnitude of 5% of

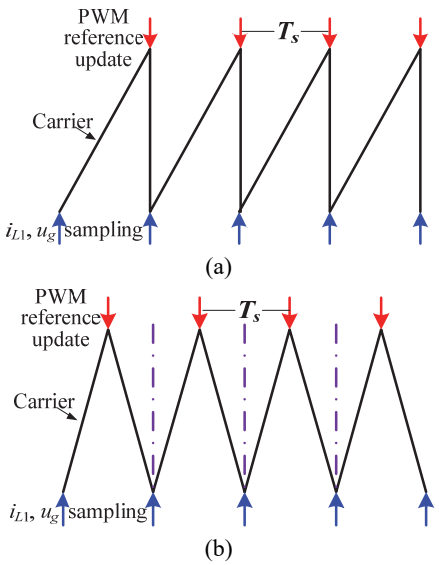


Fig. 10. Typical implementations with: (a) asymmetrical; (b) symmetrical carriers in a DSP at a control frequency of f_s.

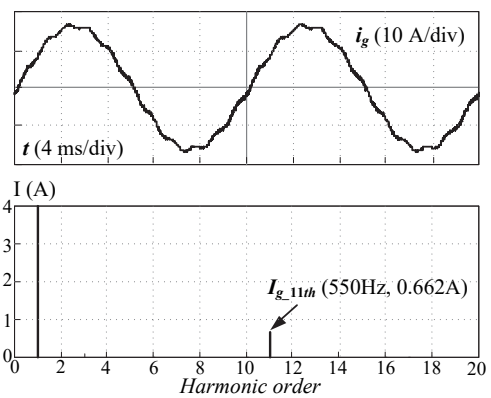


Fig. 11. Grid current waveform and spectrum with the PI+PGF in the case of 5% 11th grid voltage harmonic.

the fundamental grid voltage is added to u_g. In this case, according to the above Sections, the minimum value "I_{min}" of the grid current 11th harmonic is the 11th voltage magnitude (i.e., 311*5%) divided by the inverter output impedance value of (14), i.e., I_{min}=0.388A. Simulations with different harmonic compensators are tested. First, the grid current waveform and its spectrum with the PI+PGF are given in Fig. 11. The 11th grid current harmonic I_{g_11th} is much larger than I_{min}. In addition, the magnitudes of I_{g_11th} with the PR or PR+PGF are given in Fig. 12. With only the PR, the 11th harmonic magnitude of i_g gets close to the minimum value with an increase of k_r, but not proportionally. This result agrees with the analysis in Section III-C. For the PR and PGF, when compared with that of PR only, the harmonic in i_g is only slightly suppressed while I_{g_11th} cannot be smaller than I_{min}. Even with a higher PR gain, the low-order grid current harmonic cannot be further reduced, as analyzed in Section III-D.

B. Tests for T≠0 (Experiment)

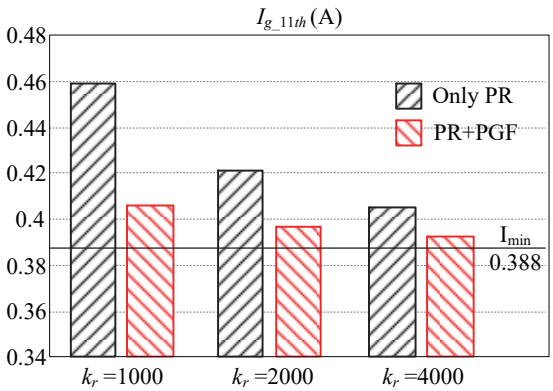


Fig. 12. Magnitudes of the 11th grid current harmonic with the PR or PR+PGF in the case of 5% 11th grid voltage harmonic.

The ac grid in the experimental tests in this paper has a lot of low-order harmonics. Obtained from a power analyzer, the spectrum of u_g at low frequencies (i.e., 0.1~1 kHz) is shown in Fig. 13. It is clear that the 3rd to 17th odd voltage harmonics are relatively large. According to (25), in such a grid distortion case, the grid current with the system parameters (i.e., C_1=7 μF) in Table I is assumed to be capable of satisfying the low-order current harmonics limitations of IEEE 929-2000 and 1547.2-2008 even if the power is 50% of the rated output. As discussed in Section IV, for the purpose of improving the grid current quality as much as possible, a small value of C_1 and a short computation delay are recommended. Next, the inverter is tested in four cases, i.e., Case I: C_1=17 μF and $T=T_s$; Case II: C_1=7 μF and $T=T_s$; Case III: C_1=17 μF and $T=0.5T_s$; Case IV: C_1=7 μF and $T=0.5T_s$.

At first, the experiments at half power with Strategy 2 using the PI and PGF in the four cases are tested. The measured THDs in the four cases are 6.84%, 5.47%, 4.61% and 3.57%, respectively. With a smaller C_1 or T, the grid current quality is better. Moreover, Fig. 14(a) shows the measured grid current spectra at half power in different cases, while the current waveforms are not shown due to space limitations. For the 3rd current harmonic, the harmonic value varies slightly while changing C_1 or T because harmonics caused by inverter non-ideal factors cannot be suppressed by the PGF. For other low-order grid current harmonics, a comparison of Cases I and III or Cases II and IV indicates that decreasing T helps to suppress those harmonics, while a comparison of Cases I and II or Cases III and IV demonstrates that decreasing C_1 helps. The effectiveness of the two approaches in Section IV have been verified. Moreover, the inverter-side current control in Case IV makes the grid current quality much better than the standards in IEEE 929-2000 even at half power. In other words, with the two approaches, including decreasing C_1 and shortening T, the grid current quality is greatly improved.

Performances with the PR controller in (7) are also verified. The measured grid current spectra in the four cases at half power are depicted in Fig. 14(b). The THDs in the four cases

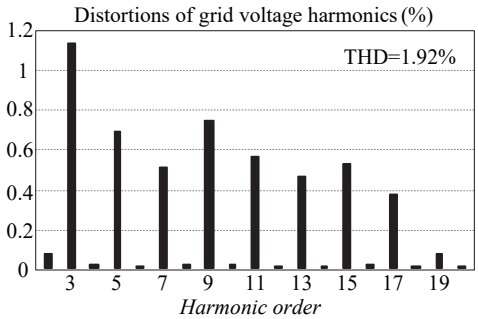
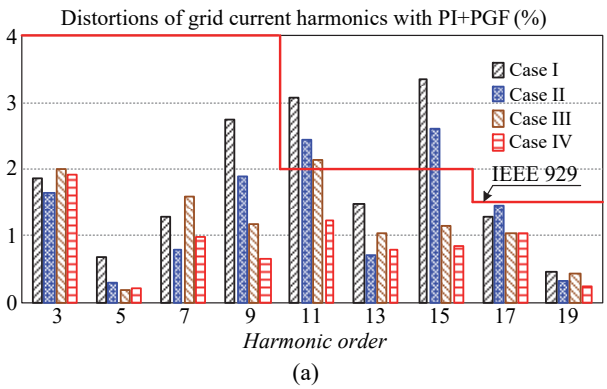
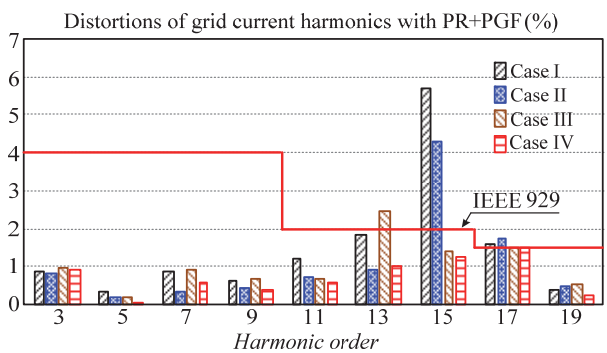


Fig. 13. Grid voltage spectrum (0.1~ 1 kHz) in the tests.



(a)



(b)

Fig. 14. Measured grid current spectra at half power with: (a) PI+PGF; (b) PR+PGF.

are 7.44%, 5.53%, 4.24% and 3.06%. The grid current quality improves with decreasing C_1 or T, which is the same as the PI+PGF. However, when compared with the THDs of PI+PGF, the use of the PR+PGF yields higher THDs in Cases I and II. A comparison of Figs. 14(a) and 14(b) indicates two things in general. First, the use of 3rd to 11th resonant controllers reduces the 3rd to 11th grid current harmonics, as shown in Figs. 7(b) and 9(b). Second, the 13th to 17th grid current harmonics are greatly amplified. This is actually due to insufficient PM values when using a multi-harmonic resonant controller. Fig. 15 shows open-loop Bode plots with Strategy 2 and the PR in Cases I and II. The open-loop phase values at the 13th to 17th frequencies are so close to −180° that the inverter with the inverter-side current control is very sensitive to the noises around these frequencies. As a result, the use of the PR produces higher THDs in Cases I and II.

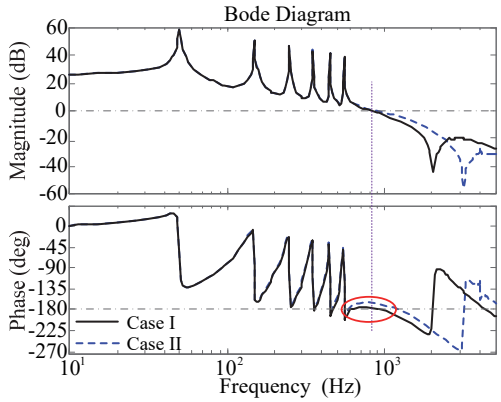
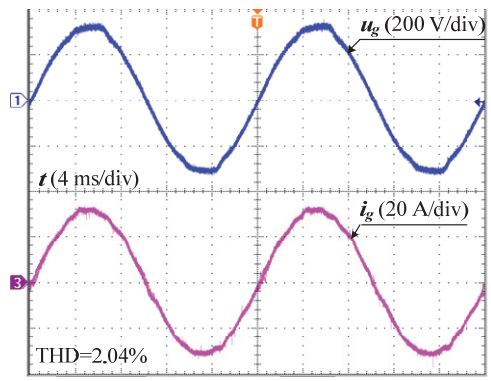
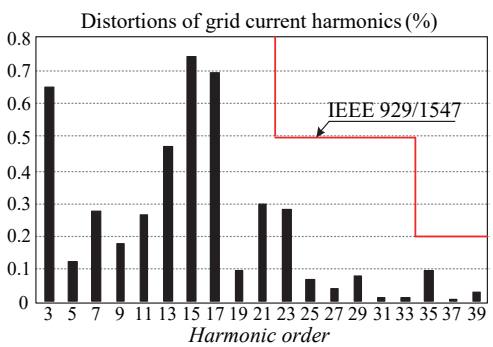


Fig. 15. Open-loop Bode plots with the PR in Cases I and II.



(a)



(b)

Fig. 16. Results in the preferred Case IV with the PR+PGF: (a) grid current waveform; (b) grid current spectrum.

Seen from the above measured results, the inverter in Case IV (i.e., with the two improved approaches) shows an obvious improvement over the other cases. Then, the overall performance of the inverter prototype with the inverter-side current control in Case IV is further tested. Fig. 16 gives some results including the grid current waveform and spectrum at full power. The current quality standard is well satisfied. Moreover, the THD and PF plots in different power cases are displayed in Fig. 17. The PF at 10% of the rated output is much higher than 0.85 while the THD is lower than 5% even at 30% of the rated output. In addition, as shown in Fig. 18, the *LCL*-filtered inverter exhibits a good performance in the case of a change in the output power.

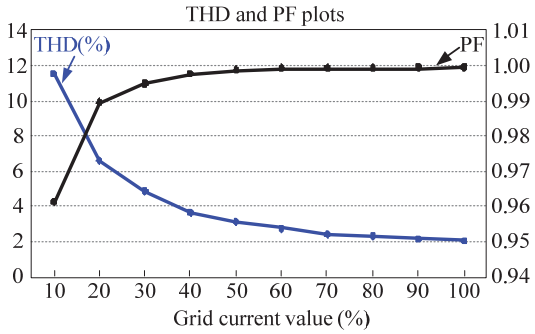


Fig. 17. Grid current THD and PF with respect to different values of the grid current.

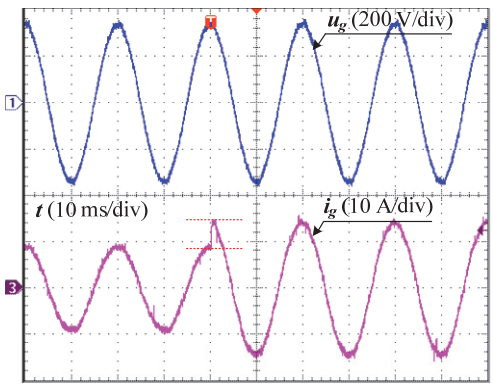


Fig. 18. Waveform when the current reference steps up.

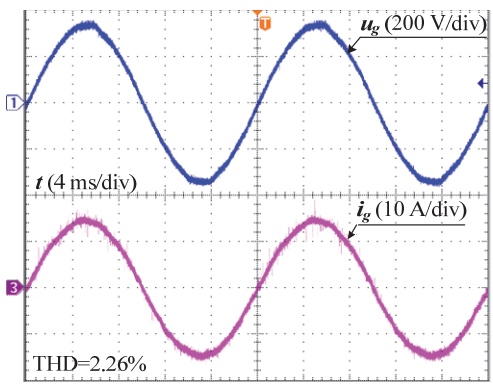


Fig. 19. Experimental waveform with a 1mH grid impedance.

Recently, more studies have been focused on the performance in weak grid cases. Fig. 19 shows steady-state waveforms when a 1mH inductor is added to simulate grid impedance. It is shown that the grid current is still synchronized with the PCC voltage with a low distortion.

VI. Conclusion

This study discussed low-order grid current harmonics suppression for *LCL*-filter inverters with inverter-side current control, through the inverter output impedance model. The contributions of this study include:

1) The adoption of harmonic compensators (i.e., the grid-voltage feedforward and harmonic resonant controller) in

the inverter-side current control can result in complicated situations, unlike that in the grid current control. First, with or without compensators, the magnitudes of the inverter output impedance at low frequencies have maximum values related to the *LCL* parameters. Second, the harmonic resonant controller cannot fully suppress the grid current harmonics, and a high resonant gain cannot make the output impedance magnitudes at grid-harmonic frequencies greater than their maximums. Third, a delay is harmful to the grid current quality, even when harmonic resonant controllers are adopted. In other words, the reasons for the poor grid current quality in past studies are clearly explained.

2) Based on an analysis of the limitations of inverter-side current control, two approaches have been proposed to improve the grid current quality. One is to design the capacitance of the *LCL* filter considering the harmonic current constraints, and the other is to select a PWM implementation with a shorter control delay.
3) It is shown that, even if an inverter is connected to a distorted grid, the inverter-side current control is able to effectively suppress grid current harmonics and satisfy the standards very well with the two improved approaches.

ACKNOWLEDGMENT

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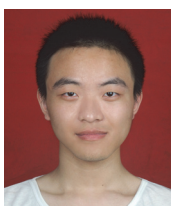
REFERENCES

[1] H.-G. Jeong, D.-K. Yoon, and K.-B. Lee, "Design of an *LCL*-filter for three-parallel operation of power converters in wind turbines," *Journal of Power Electronics*, Vol. 13, No. 3, pp. 437-446, May 2013.
[2] X. Zheng, L. Xiao, Y. Lei, and Z. Wang, "Optimisation of LCL filter based on closed-loop total harmonic distortion calculation model of the grid-connected inverter," *IET Power Electron*., Vol. 8, No. 6, pp. 860-868, Jun. 2015.
[3] J. Xu, S. Xie, L. Huang, and L. Ji, "Design of LCL-filter considering the control impact for grid-connected inverter with one current feedback only," *IET Power Electron.*, Vol. PP, No. PP, doi: 10.1049/iet-pel.2016.0849.
[4] X. Guo, W. Liu, and Z. Lu, "Flexible power regulation and current-limited control of the grid-connected inverter under unbalanced grid voltage faults," *IEEE Trans. Ind. Electron.*, Vol. 64, No. 9, pp. 7425-7432, Sep. 2017.
[5] S. G. Parker, B. P. McGrath, and D. G. Holmes, "Regions of active damping control for *LCL* filters," *IEEE Trans. Ind. Appl.*, Vol. 50, No. 1, pp. 424-432, Jan./Feb. 2014.
[6] J. Xu, S. Xie, and T. Tang, "Active damping-based control for grid-connected *LCL*-filtered inverter with injected grid current feedback only," *IEEE Trans. Ind. Electron.*, Vol.61, No.9, pp.4746-4758, Sep. 2014.
[7] L. Zhou, Y. Chen, A. Luo, J. M. Guerrero, X. Zhou, Z. Chen, and W. Wu, "Robust two degrees-of-freedom single-current control strategy for LCL-type grid-connected DG system under grid-frequency fluctuation and grid-impedance variation," *IET Power Electron.*, vol. 9, no. 14, pp. 2682-2691, Nov. 2016.
[8] R. Teodorescu, F. Blaabjerg, U. Borup, and M. Liserre, "A new control structure for grid-connected *LCL* PV inverters with zero steady-state error and selective harmonic compensation," *in Proc. IEEE APEC*, pp. 580-586, 2004.
[9] Y. Tang, P. C. Loh, P. Wang, F. H. Choo, and F. Gao, "Exploring inherent damping characteristic of *LCL*-filters for three-phase grid-connected voltage source inverters," *IEEE Trans. Power Electron.*, Vol. 27, No. 3, pp. 1433-1443, Mar. 2012.
[10] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values," *IEEE Trans. Power Electron.*, Vol. 21, No. 1, pp. 263-272, Jan. 2006.
[11] C. Zou, B. Liu, S. Duan, and R. Li, "Influence of delay on system stability and delay optimization of grid-connected inverters with *LCL* filter," *IEEE Trans. Ind. Informat*., Vol. 10, No. 3, pp. 1775-1784, Aug. 2014.
[12] J. Dannehl, C. Wessels, and F. W. Fuchs, "Limitations of voltage-oriented pi current control of grid-connected PWM rectifiers with *LCL* filters," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 2, pp. 380-388, Feb. 2009.
[13] R.N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C.L. Bak, "A review of passive power filters for three-phase grid- connected voltage-source converters," *IEEE J. Emerg. Sel. Top. Power Electron.*, Vol. 4, No. 1, pp. 54-69, Mar. 2016.
[14] J. Dannehl, M. Liserre, and F. W. Fuchs, "Filter-based active damping of voltage source converters with *LCL* filter," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 8, pp. 3623-3633, Aug. 2011.
[15] R. Peña-Alzola, M. Liserre, F. Blaabjerg, M. Ordonez, and T. Kerekes, "A self-commissioning notch filter for active damping in a three-phase *LCL*-filter-based grid-tie converter," *IEEE Trans. Power Electron.*, Vol. 29, No. 12, pp. 6754-6761, Dec. 2014.
[16] W. Yao, Y. Yang, X. Zhang, F. Blaabjerg, and P.C. Loh, "Design and analysis of robust active damping for *LCL* filters using digital notch filters," *IEEE Trans. Power Electron.*, doi: 10.1109/TPEL.2016.2565598, early access
[17] B. Bahrani, M. Vasiladiotis, and A. Rufer, "High-order vector control of grid-connected voltage-source converters with *LCL*-filters," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 6, pp. 2767-2775, Jun. 2014.
[18] Y. Zhang, M. Xue, M. Li, Y. Kang, and J. M. Guerrero, "Co-design of the *LCL* filter and control for grid-connected inverters," *Journal of Power Electronics*, Vol. 14, No. 5, pp. 1047-1056, Sep. 2014.
[19] J. Xu, S. Xie, and T. Tang, "Improved control strategy with grid-voltage feedforward for *LCL*-filter-based inverter connected to weak grid," *IET Power Electron.*, Vol. 7, No. 10, pp. 2660-2671, Oct. 2014.
[20] M. Xue, Y. Zhang, Y. Kang, Y. Yi, S. Li, and F. Liu, "Full feedforward of grid voltage for discrete state feedback controlled grid-connected inverter with *LCL* filter," *IEEE Trans. Power Electron.*, Vol. 27, No. 10, pp. 4234-4247, Oct. 2012.
[21] W. Li, X. Ruan, D. Pan, and X. Wang, "Full-feedforward schemes of grid voltages for a three-phase *LCL*-type grid-connected Inverter," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 6, pp. 2237-2250, Jun. 2013.
[22] J. Xu, S. Xie, Q. Qian, and B. Zhang, "Adaptive feedforward algorithm without grid impedance estimation for inverters to suppress grid current instabilities and

harmonics due to grid impedance and grid voltage distortion," *IEEE Trans. Ind. Electron.*, Vol. 64, No. 9, pp. 7574-7586, Sep. 2017.
[23] Y. Jia, J. Zhao, and X. Fu, "Direct grid current control of *LCL*-filtered grid-connected inverter mitigating grid voltage disturbance," *IEEE Trans. Power Electron.*, Vol. 29, No. 3, pp. 1532-1541, Mar. 2014.
[24] J. Xu, T. Tang, and S. Xie, "Research on low-order current harmonics rejections for grid-connected *LCL*-filtered inverters," *IET Power Electron.*, Vol. 7, No. 5, pp. 1227-1234, May 2014.
[25] Y. Han, P. Shen, and J. M. Guerrero, "Stationary frame current control evaluations for three-phase grid-connected inverters with PVR-based active damped *LCL* filters," *Journal of Power Electronics*, Vol. 16, No. 1, pp. 297-309, Jan. 2016.
[26] Q. Qian, S. Xie, L. Huang, J. Xu, Z. Zhang, and B. Zhang, "Harmonic suppression and stability enhancement for parallel multiple grid-connected inverters based on passive inverter output impedance," *IEEE Trans. Ind. Electron.*, Vol. 64, No. 9, pp. 7587-7598, Sep. 2017.
[27] N. Hoffmann, M. Hempel, M. C. Harke, and F. W. Fuchs "Observer-based grid voltage disturbance rejection for grid connected voltage source PWM converters with line side *LCL* filters," in *Proc. IEEE ECCE*, pp. 69-76, 2012.
[28] J. Wang, J. D. Yan, L. Jiang, and J. Zou, "Attenuation of low-order current harmonics in three-phase *LCL*-filtered grid-connected inverters," in *Proc. IEEE IECON*, pp. 1982-1987, 2015.
[29] J. Wang, J. D. Yan, L. Jiang, and J. Zou, "Delay-dependent stability of single-loop controlled grid-connected inverters with *LCL* filters," *IEEE Trans. Power Electron.*, Vol. 31, No. 1, pp. 743-757, Jan. 2016.
[30] J. Xu, S. Xie, and B. Zhang, "Stability analysis and improvement of the capacitor current active damping of the LCL filters in grid-connected applications," *Journal of Power Electronics*, Vol. 16, No. 4, pp. 1565-1577, Jul. 2016.

Jinming Xu was born in Jiangsu, China, in 1987. He received his B.S. degree in Electrical Engineering, and his Ph.D. degree in Power Electronics from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2009 and 2017, respectively. In 2017, he joined the College of Automation Engineering, NUAA, where he is presently working as a Lecturer. He received an IET Power Electronics Premium Award in 2015. His current research interests include grid-connected inverters and control strategies.

Shaojun Xie was born in Hubei, China, in 1968. He received his B.S., M.S. and Ph.D. degrees in Electrical Engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1989, 1992 and 1995, respectively. In 1992, he joined the Faculty of Electrical Engineering Teaching and Research Division, NUAA, where he is presently working as a Professor in the College of Automation Engineering. In the past five years, he has authored or coauthored over 100 technical papers published in journals and international conference proceedings. His current research interests include aviation electrical power supplies and power electronic conversion.



Binfeng Zhang was born in China, in 1991. He received his B.S. degree in Electrical Engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2013, where he is presently working towards his Ph.D. degree. His current research interests include grid-connected inverters and the application of wide bandgap devices.