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Discontinuous PWM Scheme for Switching Losses Reduction in Modular Multilevel Converters

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Abstract

The modular multilevel converter (MMC) is generally considered to be a promising topology for medium-voltage and high-voltage applications. However, in order to apply it to high-power applications, a huge number of switching devices is essential. The numerous switching devices lead to considerable switching losses, high cost and a larger heat sink for each of the switching device. In order to reduce the switching losses of a MMC, this paper analyzes the performance of the conventional discontinuous pulse-width modulation (DPWM) method and its efficiency. In addition, it proposes a modified novel DPWM method for advanced switching losses reduction. The novel DPWM scheme includes an additional rotation method for voltage-balancing and power distribution among sub modules (SMs). Simulation and experimental results verify the effectiveness and performance of the proposed modulation method in terms of its switching losses reduction capability.

Key words: Discontinuous PWM, Modular multilevel converter, Switching losses

I. INTRODUCTION

In recent years, voltage-source converter based high voltage direct current (VSC-HVDC) has been widely used as a solution for numerous high power applications [1]-[8]. In particular, modular multilevel converters (MMCs) are regarded as a promising topology for VSC-HVDC systems and flexible alternating current transmission systems, due to their advantages such as modular structure, high power quality, and dc-fault ride-through capability [9]-[11]. Fig. 1 shows the construction of a three-phase MMC. Each arm of the MMC is composed of series-connected half-bridge sub modules (HB-SMs) and an arm inductor. Due to this modular construction, the MMC is able to easily generate various voltage and power level demands.

Great effort has been made to improve and develop the performance and reliability of the MMC. Many researchers have studied the MMC. They focused on the mathematical modeling [12], control strategy [13], circulating current suppression [14], capacitor voltage balancing [15], fault detection and tolerance [16], etc.

The modulation scheme is important due to the influences of the harmonics, control dynamics, filter size, and switching losses. Various modulation schemes have been proposed including the nearest level modulation (NLM) [17], [18] selective harmonic elimination (SHE) [19], and carrier-based pulse width modulation (CPWM) [20]-[22]. The SHE method becomes very complex to design and implement for a MMC with many SMs. When compared to the SHE method, the NLM approach is computationally less complex. However, in spite of its low switching frequency and simple implementation, the NLM scheme distorts the quality of the output voltage and currents more than the CPWM [23]. Multicarrier based PWM methods such as the phased-shifted PWM (PS-PWM), and the level-shifted PWM (LS-PWM) have been successfully applied for MMCs. However, the discontinuous PWM (DPWM) scheme, which is generally used to reduce switching losses, has not been studied much for the MMC.

The DPWM scheme minimizes the switching losses by reducing the number of switching operations in a fundamental frequency. Several DPWM methods are classified based on discontinuous sections, such as: 120˚, 60˚ and 30˚ DPWM. Among these, the 60˚ DPWM scheme is typically used. It can reduce the switching frequency by

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retaining the switch state as turn ON or turn OFF during a 60˚ period when the magnitude of the phase voltage is greatest [24]. Due to this characteristic, the DPWM scheme has been applied in a lot of topologies [25]-[30].

A DPWM scheme using the zero-sequence components to the MMC with reducing the capacitor voltage ripple and switching losses has been proposed in [31]. However, this switching scheme requires additional SMs to prevent over-modulation during the modulation. The authors of [32] proposed model predictive control with a DPWM scheme to enhance the output quality with reduced switching losses. This method can be achieved by operating considerable complex computations. In addition, since the MMC consists of many SMs and switching devices for use in medium-power and high-power applications, the switching losses of the MMCs with the proposed methods in [31] and [32] are still considerable.

This paper introduces a conventional carrier-based DPWM scheme for the MMC. Then, it analyzes the performance of the modulation scheme in detail. Furthermore, this paper proposes a novel DPWM scheme with advanced switching losses reduction capability for the MMC. The proposed DPWM scheme can achieve a significant reduction of the switching losses when compared to the conventional DPWM scheme, by using the constructive characteristics of the MMC. In order to reduce the losses, each of the SMs in a MMC includes additional discontinuous switching intervals when compared to the conventional DPWM scheme. Even if the reference voltages of the SMs are modified to achieve switching losses reduction, the output pole voltages are coincident with those of the conventional DPWM scheme, to maintain the output quality of the system. Finally, the proposed method achieves decreases in the size and cost of the heatsink due to its reduced switching losses by applying the proposed method without additional hardware components. In addition, the proposed method can be easily applied to a MMC which consists of a number of SMs (e.g. more than ten or fifty) for medium-voltage to high-voltage applications. PSIM simulation and experimental results verify the validity of the proposed modulation schemes in terms of switching losses reduction.

II. Basic Model of the MMC

A. Basic Operation of the MMC

As shown in Fig. 1, an HB-SM-based three-phase MMC consists of six arms, and each arm has series-connected HB-SMs and an arm inductor (L). Each leg consists of an upper arm (u) and a lower arm (l). Each HB-SM has an electrolytic capacitor and two IGBTs (T_1, T_2). The terminal voltage for each HB-SM (V_{SM}) has two values: its capacitor voltage (V_c) when T_1 is ON and T_2 is OFF; and zero when T_1 is OFF and T_2 is ON.

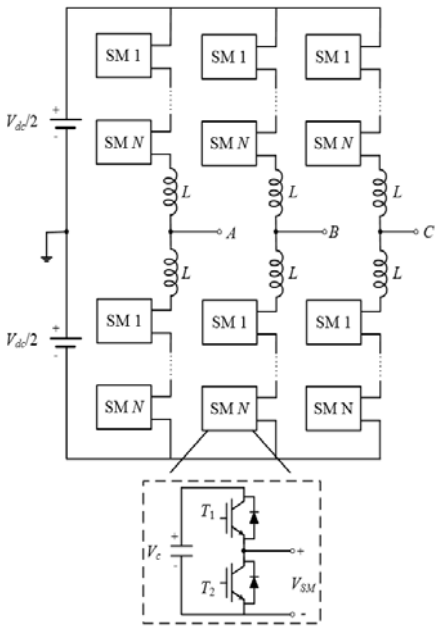


Fig. 1. Construction of a MMC.

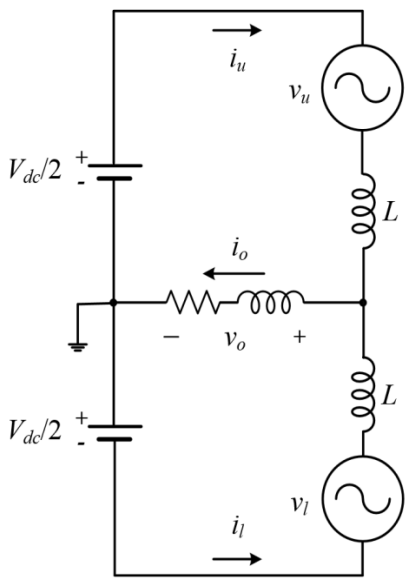


Fig. 2. Single-phase equivalent circuit of the MMC.

For the sake of simplicity, the switching function of each SM can be expressed as (i=1, 2, 3,⋯, N):

$$S_i = \begin{cases} 1, & \text{when } T_1 \text{ is ON and } T_2 \text{ is OFF, SM}_i \text{ is ON} \\ 0, & \text{when } T_1 \text{ is OFF and } T_2 \text{ is ON, SM}_i \text{ is OFF} \end{cases} . \quad (1)$$

B. Modeling of the MMC

Fig. 2 shows a phase leg of a MMC expressed by an equivalent circuit model. Through the equivalent model, the external characteristic of the SM in the MMC needs to be identified for mathematical modeling of the whole system. According to Kirchhoff's voltage law, the upper-output and lower-output arm voltages are presented as follows [12]:

$$v_u = \frac{V_{dc}}{2} - L\frac{di_u}{dt} - v_o \quad (2)$$

$$v_l = \frac{V_{dc}}{2} + L\frac{di_l}{dt} + v_o \quad (3)$$

where, V_{dc} is the dc-link voltage; v_u and i_u are the voltage and current of the upper arm; and v_l and i_l are the voltage and current of the lower arm.

Let the output current be i_o. The output current can then be expressed as $i_o = i_u + i_l$. The circulating current i_{cc} is determined as $i_{cc} = (i_u - i_l)/2$. Therefore, the arm current can be indicated with the sum of half the output current and the circulating current i_{cc} as follows:

$$i_u = \frac{i_o}{2} + i_{cc} \quad (4)$$

$$i_l = \frac{i_o}{2} - i_{cc}\,. \quad (5)$$

Through Eqs. (2)-(5), it is possible to calculate:

$$v_o = \frac{v_l - v_u}{2} - \frac{L}{2}\frac{di_o}{dt} \quad (6)$$

$$v_{diff} = L\frac{di_{cc}}{dt} = \frac{V_{dc}}{2} - \frac{v_l + v_u}{2} \quad (7)$$

where, v_{diff} is referred as the MMC internal voltage that drives the circulating current.

For each SM, the output SM voltage is generated with the value of its capacitor voltage and zero by a comparison between its reference signal and carrier band.

The voltages of the upper arm and lower arm can then be represented as the sum of the SM output voltages.

$$\begin{aligned} v_u &= S_{u1}\cdot V_{cu1} + S_{u2}\cdot V_{cu2} + \cdots + S_{uN}\cdot V_{cuN} \\ &= \sum_{i=1}^{N} S_{ui}\cdot V_{cui} \end{aligned} \quad (8)$$

$$\begin{aligned} v_l &= S_{l1}\cdot V_{cl1} + S_{l2}\cdot V_{cl2} + \cdots + S_{lN}\cdot V_{clN} \\ &= \sum_{i=1}^{N} S_{li}\cdot V_{cli} \end{aligned}\,. \quad (9)$$

According to the control objectives, it is important to ideally maintain the sum of the upper and lower arm voltages to be equal to the dc bus voltage, and to keep the output voltage a strictly sinusoidal waveform as expressed in Eq. (10) and Eq. (11).

$$v_u + v_l = V_{dc} \quad (10)$$

$$v_u - v_l = V_{dc} m\cos\omega t \quad (11)$$

where, m is the output voltage modulation index, and ω is the output fundamental frequency. Then, the references of the upper and lower arm voltages can be expressed as:

$$v_u = \frac{V_{dc}}{2}(1 - m\cos\omega t) \quad (12)$$

$$v_l = \frac{V_{dc}}{2}(1 + m\cos\omega t)\,. \quad (13)$$

C. Conventional DPWM Scheme for the MMC

The main objective when using the DPWM scheme is to reduce the switching losses. To achieve this purpose, the converter outputs are alternately connected to the top or bottom of the dc-link during selected discontinuous intervals [24]. Fig. 3 illustrates the implementation of the 60˚ DPWM method. Fig. 3(a) shows the three reference phase voltages (v^*_{as}, v^*_{bs}, v^*_{cs}), Fig. 3(b) shows the obtained offset voltage (v_{offset}), and Fig. 3(c) shows the reference pole voltages (v^*_{an}, v^*_{bn}, v^*_{cn}), which are generated by adding the reference phase voltages and the offset voltage for DPWM operation. The offset voltage is calculated by the phase voltages and the dc-link voltage (V_{dc}) as Eq. (14).

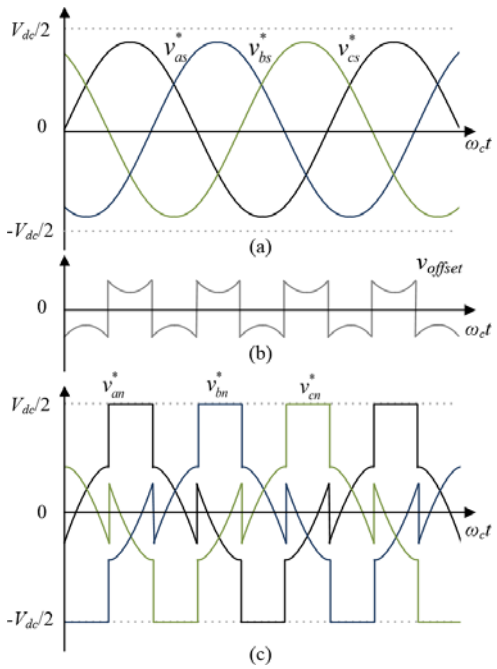


Fig. 3. Reference modulation signals of the conventional DPWM scheme: (a) three-phase voltages; (b) offset voltage; (c) pole voltages.

$$v_{offset} = \begin{cases} \frac{V_{dc}}{2} - v_{\max}, & |v_{\max}| > |v_{\min}| \\ -\frac{V_{dc}}{2} - v_{\min}, & |v_{\max}| < |v_{\min}| \end{cases}\,. \quad (14)$$

$$v_{\max} = \max(v^*_{as}, v^*_{bs}, v^*_{cs}), \quad v_{\min} = \min(v^*_{as}, v^*_{bs}, v^*_{cs})$$

The reference pole voltages of the conventional DPWM method are expressed as:

$$v^*_{xn} = v^*_{xs} + v_{offset},\ x = a,b,c\,. \quad (15)$$

In the general three-phase two-level voltage source inverter with six-switch bridges, the three-phase reference pole voltages are used as the modulation signals of the 60˚ DPWM scheme. However, in a MMC system, the modulation signals in a phase differ between the upper-arm and lower-arm, which are derived as follows:

$$v^*_{xu} = \frac{V_{dc}}{2} - (v^*_{xs} + v_{offset}),\ v^*_{xl} = \frac{V_{dc}}{2} + (v^*_{xs} + v_{offset}) \quad (16)$$

where, v^*_{xu} and v^*_{xl} are the modulation signals applied to the 60˚ DPWM scheme. In the conventional DPWM scheme,

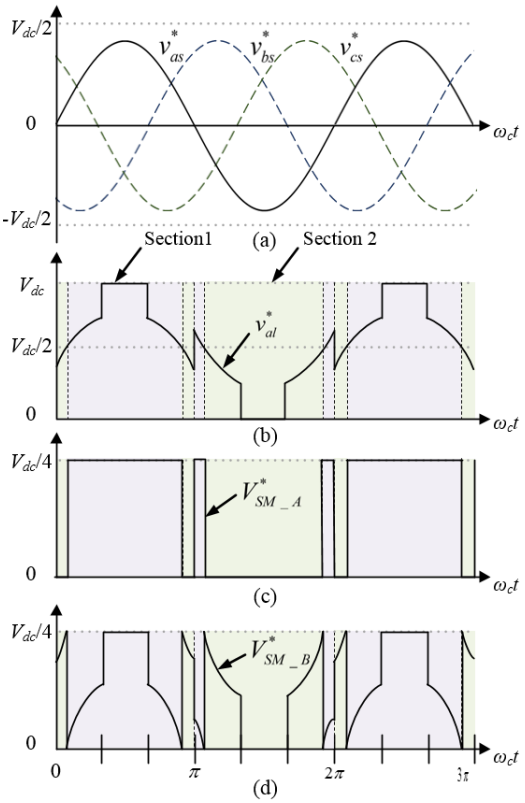


Fig. 4. Reference modulation signals of the proposed DPWM scheme: (a) three-phase voltages; (b) lower arm voltage; (c) A-type SM voltage; (d) B-type SM voltage.

the switching devices of each SM do not conduct switching operation during the 60° period when the phase voltage has the greatest magnitude in a fundamental period.

III. The Proposed DPWM Scheme

A. Principle of the Proposed DPWM Scheme

To achieve advanced switching losses reduction, this paper proposes a novel DPWM scheme for a half-bridge based MMC. Fig. 4 shows modified modulation signals of the proposed DPWM scheme for a three-phase MMC system with four SMs per arm. The arm voltages are decided by the sum of the SM output voltages in an arm, as shown in Eq. (8) and Eq. (9). Therefore, the references of the pole voltage, and the upper and lower arm voltages for the proposed DPWM scheme are the same as those of the conventional DPWM scheme, as shown in Fig. 4(b). This shows that the quality of the output currents and voltages is kept the same as the conventional DPWM scheme. However, the SM reference voltages are modified to different waveforms with the arm voltage for additional switching losses reduction, as shown in Fig. 4(c) and Fig. 4(d). This figure shows that all of the SMs in an arm are either turned ON or turned OFF, while the reference arm voltage is clamped to the upper or lower terminals of the dc sources. In addition, the produced SM voltages are clamped in additional intervals, even though the reference arm voltages are in continuous intervals.

The A-type SM reference voltage ($V^*_{SM\_A}$) in Fig. 4(c) makes the selected SM continue clamping for an additional switching losses reduction of the MMC system. Furthermore, Fig. 4(d) shows the B-type SM reference voltage ($V^*_{SM\_B}$), which is modified to maintain the output arm voltage while considering the clamping operation of the A-type SM voltage.

The clamping intervals to turn ON or OFF the A-type SM voltage are decided by the amplitude of the arm voltage. Since two SMs modulate at the same reference in the proposed method, the summation of A-type SMs is equal to $V_{dc}/2$ during the ON clamping intervals. For this reason, when the reference of the arm voltage is higher than $V_{dc}/2$ (section 1), the A-type SM maintains the state of turn ON. At the same time, the B-type SM implements the switching operation to maintain the arm voltage, while considering the clamping operation of the A-type SM.

On the other hand, when the reference arm voltage is lower than $V_{dc}/2$ (section 2), the A-type SM maintains the state of turn OFF and the B-type SM performs modulation to keep the arm voltage. The two types of the reference voltage for the SMs in the lower arm can defined as shown in Eq. (17):

$$\begin{cases} \text{section 1}: \; V^*_{SM\_A} = \dfrac{V_{dc}}{4}, \; V^*_{SM\_B} = \dfrac{(v^*_{xs} + v_{offset})}{2} \\ \text{section 2}: \; V^*_{SM\_A} = 0, \quad V^*_{SM\_B} = \dfrac{(v^*_{xs} + v_{offset})}{2} + \dfrac{V_{dc}}{4} \end{cases} . \quad (17)$$

B. Rotation Method for SM Voltage-Balancing

When the SM is turned ON, the HB-SM capacitor operates to either charge or discharge, depending on the direction of the arm current. The operation of the continuous ON clamping states of the A-type SM reference generates a large fluctuation of the SM capacitor voltage. Therefore, an additional modification of the SM reference voltages is required.

Fig. 5 shows the SM reference voltages with an additional rotation for the SM capacitor voltage balancing. Fig. 5(a) indicates the A-type and B-type SM references that are generated by Eq. (17). These two reference signal patterns should rotate for the voltage-balancing and power distribution for all of the SMs. The final reference voltages are shown in Fig. 5(b), with a rotation to diminish the unbalancing issue among capacitor voltages of the SMs. The final two types of voltage references coincide with each other due to a delayed-phase. By using the proposed DPWM scheme, with these final SM reference voltages, the SM capacitor voltages are balanced in constant.

C. SM Selection for Harmonic Cancellation

In a three-phase MMC system that has N SMs per arm, the N triangular carriers of each SM are incrementally shifted by $2\pi/N$ with a V_{dc}/N amplitude, when it uses the phase-shifted

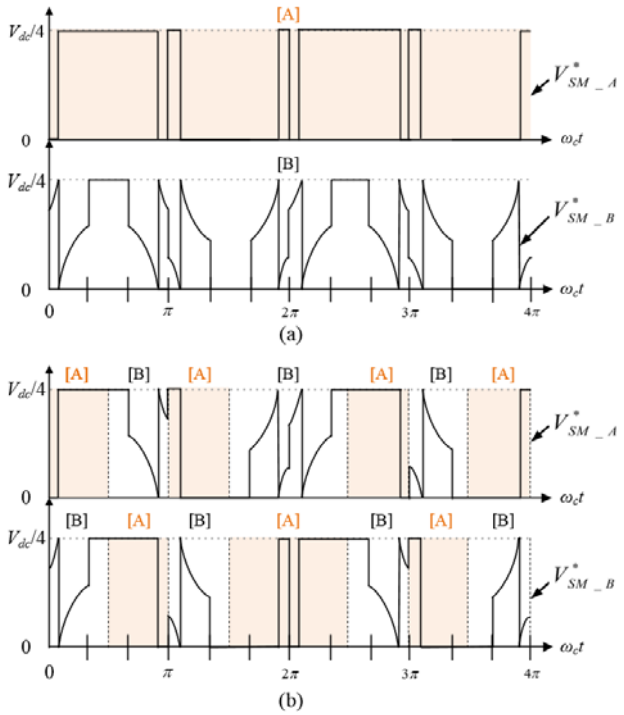


Fig. 5. SM reference voltages of the proposed DPWM scheme: (a) without rotation; (b) with rotation.

PWM (PS-PWM) scheme. The phase angle $\theta_l(i)$ of the i-th carrier C_{ln} in the lower arm can be expressed as:

$$\theta_l(i) = \frac{2\pi}{N} \times (i-1). \quad (18)$$

Fig. 6 shows the reference signal and carrier bands of four SMs for a five-level MMC. The magnitude of each carrier band is $V_{dc}/4$.

Since the proposed DPWM scheme has two kinds of SM references with four SMs per arm, it is essential to select two SMs for one of the reference signals, in order to minimize the harmonic distortion of the output voltage. The harmonics characteristic of the output voltage varies depending on the combination of SMs, which uses carrier waves with different phase angles. Based on Eq. (18), the two triangular carriers are shifted by π from each other when they modulate with a single reference signal. Therefore, the two triangular carriers are shifted by π to achieve the best harmonic cancellation features. Fig. 7 shows the actual variation of the output voltage ripples depending on the combination of two SMs. The figure shows that the best choice is two SMs (SM1 and SM3) with π phase-shifted triangular carriers using the same reference signal. Therefore, in a five-level MMC, SM1 and SM3 are given the same reference signal, while SM2 and SM4 use another reference signal for the proposed DPWM.

Finally, the proposed DPWM scheme can achieve additional switching losses reduction while maintaining the output quality. In addition, the concept of the proposed DPWM scheme can be easily expanded to MMCs with $2N$ SMs per arm. Fig. 8 shows block diagrams of the proposed

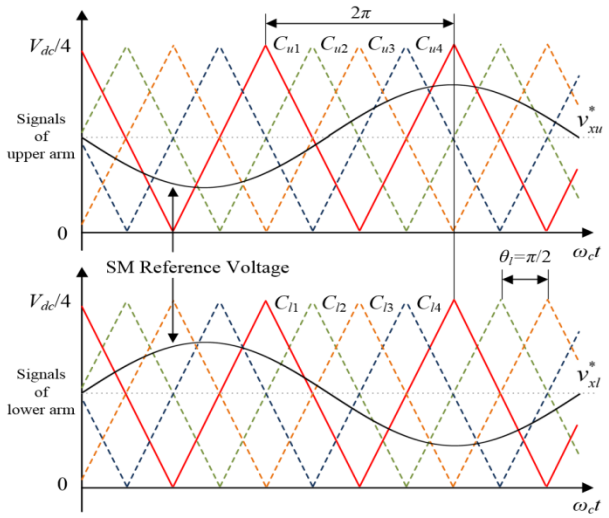


Fig. 6. PS-PWM of a five-level MMC with four SMs per arm.

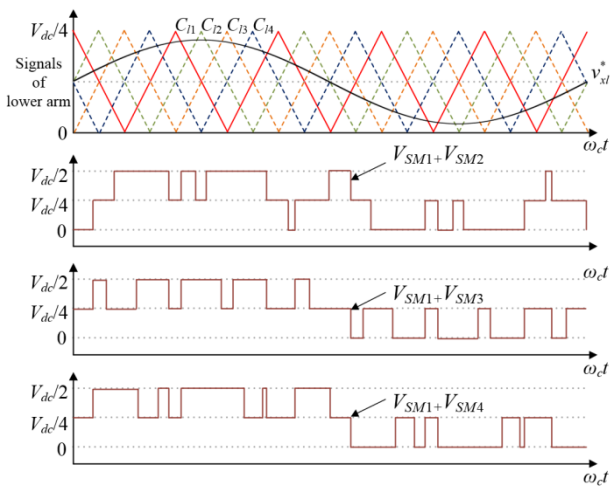


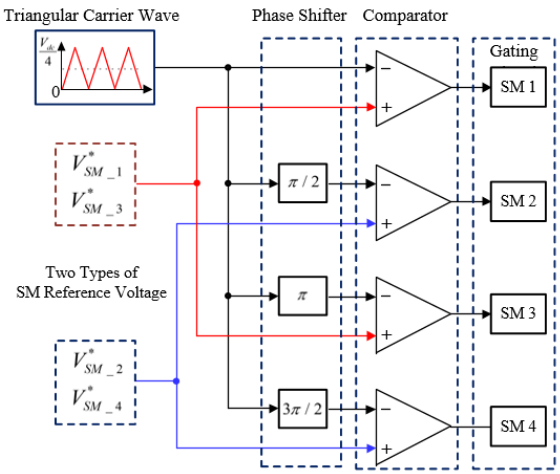
Fig. 7. Variation of the output voltage based on the SM selection.

DPWM scheme with different numbers of SMs per arm. As shown in the figure, the basic structure of the diagram for the proposed modulation is similar. In a MMC with $2N$ SMs per arm, the generated two kinds of reference voltage are distributed to the odd number SMs and even number SMs for the harmonic cancellation effect.

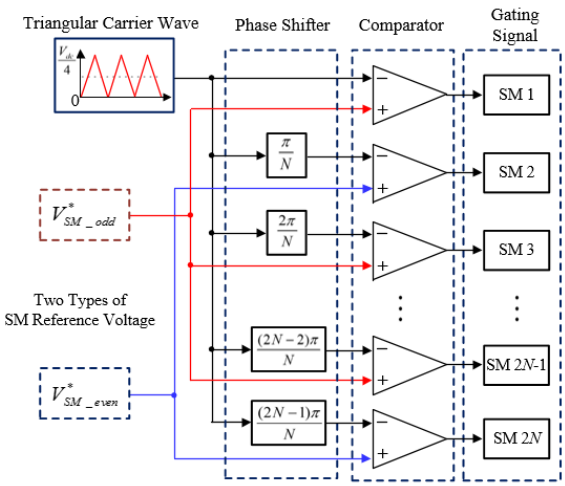
IV. Simulation Results

Simulations have been performed to verify the effectiveness of the proposed modulation method. The simulation studies are implemented in the PSIM software tool. Table I lists the simulation parameters related to the MMC. The switching frequency is set to 10 kHz to emphasize the effectiveness of the switching losses reduction capability of the proposed DPWM scheme. The input DC voltage in all of the cases is controlled to 600 V and the rated SM voltage V_c is 150 V.

Fig. 9 and 10 show performance waveforms of the



(a)



(b)

Fig. 8. Block diagram of the proposed DPWM scheme: (a) applied to an arm with four SMs; (b) applied to an arm with 2N SMs.

TABLE I
CIRCUIT PARAMETERS USED FOR SIMULATIONS

Parameters	Values
Number of SMs per Arm, N	4
SM Capacitors, C	600 µF
Arm Inductors, L	0.6 mH
Resistor Load, R_L	10 Ω
Inductor Load, L_L	3 mH
Carrier Frequency MMC, f_c	10 kHz
Output Frequency, f	60 Hz
Modulation Ratio, m	0.8

conventional DPWM scheme and the proposed DPWM scheme. Fig. 9 shows the references for the SM voltage and pole voltage, which have the same shape as those of the conventional DPWM scheme. Fig. 10 shows waveforms of

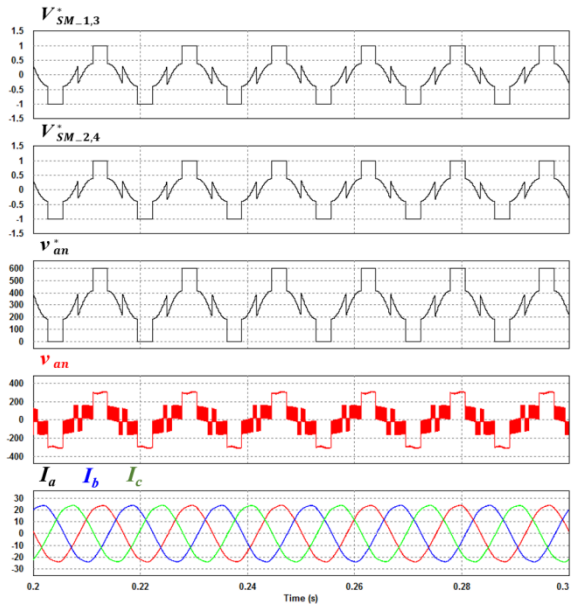


Fig. 9. Conventional DPWM scheme for a five-level MMC.

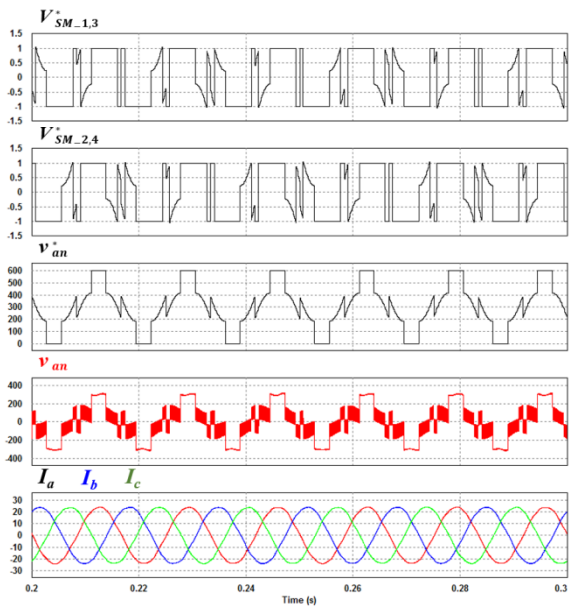


Fig. 10. Proposed DPWM scheme for a five-level MMC.

the proposed DPWM scheme with the SM reference voltages and output pole voltage. The advanced switching losses reduction capability is obtained by additional clamping intervals for each of the SM voltages. Even if the SMs implement the modified switching reference, the final reference and output of the pole voltage and the output currents are the same as those of the conventional DPWM scheme.

Fig. 11 shows the performance of the rotation method with the proposed DPWM for SM capacitor voltage-balancing. The proposed DPWM scheme without the rotation method is applied until 0.15 s. Due to the unbalanced clamping intervals between the SM reference voltages, the capacitor voltages of the SM in a leg become unbalanced. In addition, the output

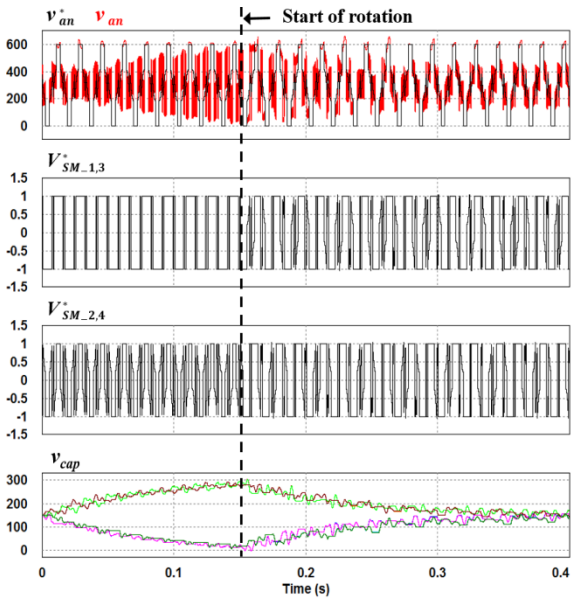


Fig. 11. Rotation method with the proposed DPWM scheme for SM capacitor voltage-balancing.

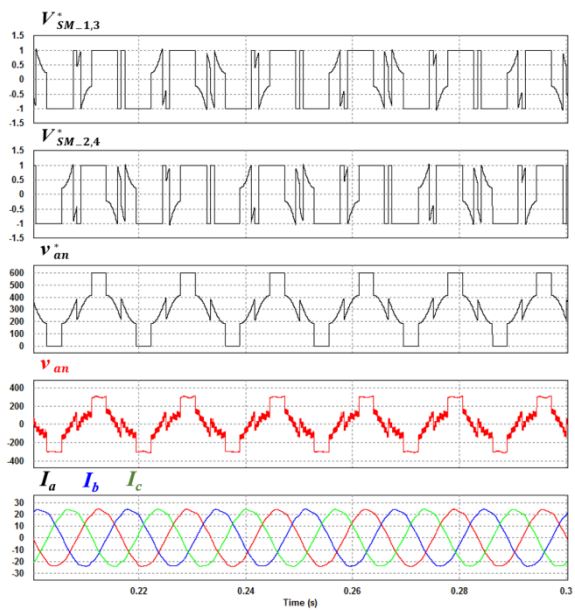


Fig. 12. Proposed DPWM scheme for a seven-level MMC.

voltage is degraded due to unbalanced SM voltages. After 0.15 s, the rotation method is applied to the proposed DPWM scheme, and the reduced unbalance problem of the SM voltages is confirmed. Therefore, the quality of the output pole voltage is improved by the rotation method.

Simulations for the expanded MMC at the academic laboratory level are also implemented in this paper. Fig. 12 shows results for a MMC with six SMs per arm. As with Fig. 10, the proposed method with six SMs per arm uses two kinds of reconfigured reference signals to achieve additionally reduced switching losses. The generated reference signals are distributed to odd number SMs (SM1, SM3 and SM5) and even number SMs (SM2, SM4 and SM6)

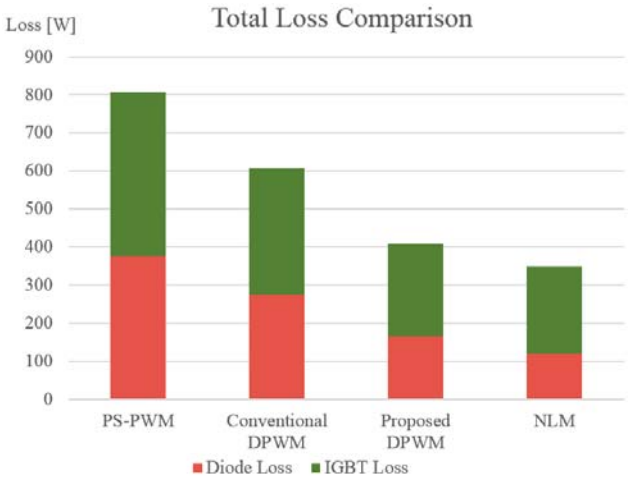


Fig. 13. Losses analysis of the switches for different modulation methods.

for the harmonic cancellation effect. The obtained simulation results show the maintained output quality of the MMC. In the same way, the proposed method can be easily expanded to a MMC with 2N SMs per arm by using two kinds of SM reference voltages for MVDC to HVDC applications.

To verify the improvement in efficiency through the proposed modulation scheme, this paper considers the IGBT and diode losses, which consist of switching loss and conduction loss. The switching loss ($P_{diode.switch}$) and conduction loss ($P_{diode.cond}$) of a diode are calculated as [28]:

$$\begin{cases} P_{diode.switch} = f_{sw} \times E_{rr} \\ P_{diode.cond} = V_d \times I_F \times D_{diode} \end{cases} \quad (19)$$

where, f_{sw} is the switching frequency, E_{rr} is the reverse recovery energy loss, V_d is the diode voltage drop, I_F is the diode forward current, and D_{diode} is the duty ratio of the diode.

The switching loss ($P_{IGBT.switch}$) and conduction loss ($P_{IGBT.cond}$) of an IGBT are calculated as follows:

$$\begin{cases} P_{IGBT.switch} = f_{sw} \times (E_{ON} + E_{OFF}) \\ P_{IGBT.cond} = V_{CE} \times I_C \times D_{sw} \end{cases} \quad (20)$$

where E_{ON} and E_{OFF} are the turn ON and turn OFF energy losses, I_C is the collector current, and D_{sw} is the duty ratio of the IGBT.

Based on Eq. (19) and Eq. (20), the loss analysis simulation is also implemented by PSIM simulations. The overall simulation parameters are the same as those in Table I, where the output power is about 8.5 kW. The features of the IGBT module S2124PA300SC by Vincotech are considered to analyze the switching losses of the proposed method. In addition, the junction temperature is 150˚C which has the limit condition of the IGBT.

Fig. 13 shows a comparison of the switching losses to verify the effectiveness of the proposed method. In order to compare the reduced switching losses of the proposed DPWM scheme with those of other modulation methods, the PS-PWM scheme, the conventional DPWM scheme, and the

TABLE II
COMPARISON OF SWITCHING MODULATION METHODS

	Switching Loss [W]			THD [%]
	IGBT	Diode	Total	
PS-PWM	431.7	376.2	807.9	1.87
Conventional DPWM	334.6	273.1	607.7	2.16
Proposed DPWM	243.3	165.2	408.5	3.09
NLM	229.3	119.6	348.9	17.69

NLM scheme are considered.

Since the PS-PWM continuously conducts the switching operation, it has the largest switching losses among the tested methods. On the other hand, the NLM method has the smallest switching losses by approximating the reference to the closest available voltage level. The conventional DPWM scheme and proposed DPWM scheme show reduced switching losses because of the discontinuous intervals. Especially, the total loss of the proposed DPWM is smaller than that of the conventional DPWM scheme with additional clamping intervals for each of the SMs. The proposed DPWM scheme has an advanced switching losses reduction capability of about 32.8% when compared with the conventional DPWM scheme.

Table II shows the total loss and output current THD for each of the modulation methods. The current THD of the PS-PWM shows the lowest value because of the continuous switching operation. The proposed DPWM scheme shows a slightly increased current THD when compared with that of the conventional DPWM method, because of the additional clamping intervals. However, the proposed method maintains its output quality with significantly reduced switching losses when compared to those of the NLM method. The distortion in the output current generated by the NLM method is considerable when applied in a MMC with few SMs. For this reason, the proposed DPWM scheme is more appropriate than the NLM method in MVDC (1 kV to 35 kV) applications, where numerous SMs are not required.

V. EXPERIMENTAL RESULTS

In order to demonstrate the proposed modulation scheme and verify the simulation results, an experiment is conducted in the laboratory. Fig. 14 shows the experimental setup of the power converter and control unit of the MMC.

The system is controlled by a control unit, which consists of a TMS320C28346 digital signal processor (DSP) board with an FPGA (Xilinx, XC6SLX45-CSG324) and other peripherals. The proposed modulation scheme is programmed

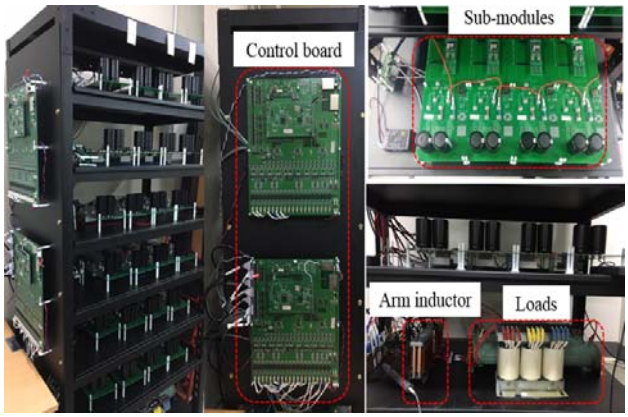
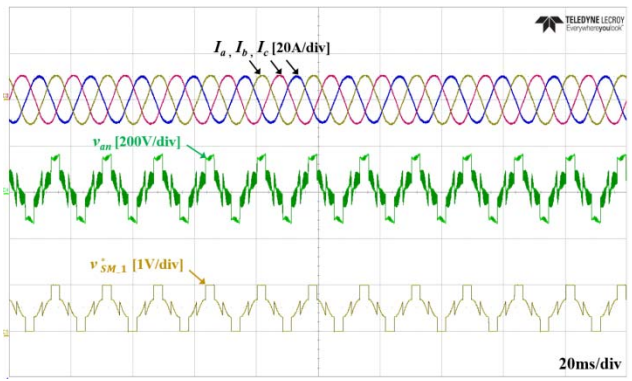
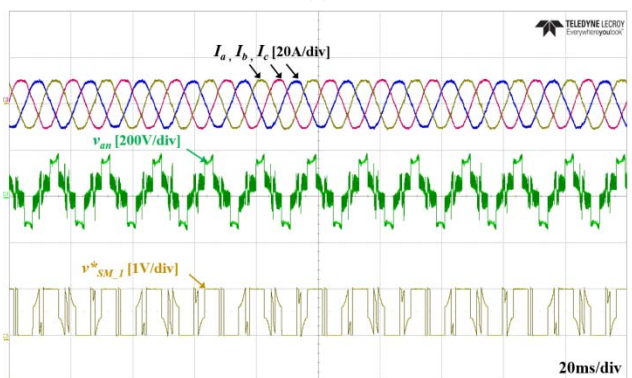


Fig. 14. Experimental setup of a three-phase five-level MMC.



(a)



(b)

Fig. 15. Experimental output waveforms of the DPWM scheme for a MMC with the: (a) conventional DPWM; (b) proposed DPWM.

on the DSP board. The input DC voltage in all of the cases for the experiment is set to 300 V and the rated SM voltage is 75 V. This DC voltage is small for the original purpose of an MMC topology. However, it is sufficient to show the switching results of the proposed modulation method. The other experimental parameters and operating conditions are the same as those of the PSIM simulation.

Fig. 15 shows experimental waveforms of the DPWM scheme for the MMC. Fig. 15 (a) shows that the conventional DPWM scheme has clamping intervals of the SM voltage during the 60° period when the magnitude of the phase voltage is at its largest. Fig. 15 (b) shows the experimental

output for the proposed DPWM scheme. As explained in Section III, the SM reference voltage includes additional clamping intervals for advanced switching losses reduction capability. Since the proposed scheme is modulated to generate the same reference as the pole voltage, the output pole voltage waveform of the proposed DPWM scheme is similar to that of the conventional DPWM scheme. However, as with the simulation results, the output three-phase currents are slightly degraded using the proposed method.

VI. CONCLUSIONS

This paper presents a novel DPWN method with advanced switching losses reduction capability for MMC systems. The proposed method modifies the reference voltages for each of the SMs to increase the non-switching intervals for losses reduction. The modified SM reference voltages also consider the output pole and arm voltage to maintain the output quality of the system. In addition, the rotation method is also applied in the proposed DPWM scheme for voltage-balancing of the SM capacitors. Both simulation and experimental results demonstrate the validity of the modulation method with a five-level MMC. A comparison with other modulation methods confirms the validity of the proposed method. The results show that the proposed DPWM scheme has advanced switching losses reduction capability, while maintaining the output quality of the system. The proposed method is a possible power loss reducing modulation method for MMCs.

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