

Novel Adaptive Blanking Regulation Scheme for Constant Current and Constant Voltage Primary-side Controlled Flyback Converter

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Abstract

Primary-side regulation (PSR) scheme is widely applied in low power applications, such as cell phone chargers, network adapters, and LED drivers. However, the efficiency and standby power requirements have been improved to a high standard due to the new trends of DOE (Department Of Energy) Level VI and COC (Code Of Conduct specifications) V5. The major drawbacks of PSR include poor regulation due to inaccurate feedback and difficulty in acquiring acceptable regulation. A novel adaptive blanking strategy for constant current and constant voltage regulation is proposed in this paper. An accurate model for the sample blanking time related to transformer leakage inductance and the metal-oxide-semiconductor field-effect transistor (MOSFET) parasitic capacitance is established. The proposed strategy can achieve accurate detection for ultra-low standby power. In addition, numerous control factors are analyzed in detail to eliminate the influence of leakage inductance on the loop stability. A dedicated controller integrated circuit (IC) with a power MOSFET is fabricated to verify the effectiveness of the proposed control strategy. Experimental results demonstrated that the prototype based on the proposed IC has excellent performance.

Key words: Adaptive blanking time, Primary-side regulation, Transformer leakage inductance

I. INTRODUCTION

In AC-DC charger application, a constant current and constant voltage (CCCV) converter should be established to charge the batteries of equipment, such as cell phone, digital camera, and laptop. The switching power supply can be designed to satisfy almost all conceivable application specifications, such as efficiency, performance, communications, protection, approval compliance, and power density.

Quasi-resonant (QR) flyback, active clamped forward, and LLC resonant converters are preferred in medium power applications. By contrast, in the low power applications, flyback converter is the best option, and the QR operation

mode is better due to the valley turn-on that reduces the switching loss [1]-[3]. Generally, the optimized primary-side regulation (PSR) is selected to satisfy the DOE Level VI and COC V5 efficiency standards [4], [5], especially in the power deliver 2.0/3.0 and Type-C applications that require ultra-low standby power loss [6].

During the past decade, the PSR technology has been rapidly developed. PSR can reduce the opto-coupler and TL431 feedback components. The primary-side control method is straightforward and relatively simple compared with traditional secondary-side regulation (SSR) method. This method can save printed circuit board space, reduce cost, and improve the entire system reliability [1], [7]. In addition, the most important benefit of PSR is that it can eliminate the opto-coupler, which suffers from CTR degradation over time and temperature [7]-[9]. Nevertheless, among many isolated switching mode power supply topologies, flyback converter is one of the most preferred options for low power applications due to its low cost, high efficiency, and

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extensive input range in low output power applications [1]-[3], [10]-[14]. Therefore, the PSR controlled flyback converter is widely used in small and medium power applications, such as cell phone charger and LED driver applications.

However, the PSR is not perfect due to its indirect feedback control mechanism. The load regulation effectiveness is influenced by real-time load changes, component temperature, and batch tolerance. Extensive studies have been conducted on PSR control within this decade. Different PSR techniques are proposed in terms of knee point detector, which involves constant time sampling with high-speed sample and hold method. The techniques can be implemented by either using analog or digital control [7], [8], [10]-[12], [15]-[18]. Considering the constant current applications, many studies have been conducted for accuracy improvement. In various primary-side control novel techniques, such as detection methods, mathematical models, and transformer leakage inductance model, delay time compensation is introduced by industrial and academic fields [11]-[15], [16]. A few special technologies are investigated for dynamic response efficiency improvement using the new snubber topology [19]-[21].

In [7]-[10], a sample and hold circuit is presented for knee point detection to ensure that the sampling is near the instance when the inductor current is zero. The feedback voltage is accurate under various load conditions because the diode voltage is not affected by the diode current. However, the knee point detection method cannot solve the line input voltage and transformer leakage influence. In [11], [12], PSR for LED drivers with high power factor is proposed. The highly precise constant current and power factor and low total harmonic distortion (THD) can be achieved by this control technology. PSR has low bill-of-material (BOM) cost and high reliability and is only proposed for the constant current applications. In [13], considering all the factors, such as winding resistance, the leakage inductance of transformer, voltage drop of rectified diode on the secondary side, and effective turn ratio, an analytical model of the flyback transformer is established for feedback error analysis. However, this model can only solve the regulation for a dedicated case and is not a general method. In [14], a current compensation circuit is proposed to improve the load regulation in continuous conduction mode operation (CCM). However, the accuracy of this proposed circuit is still unacceptable. In [15], [16], although the highly precise current and voltage regulation is obtained by using different control strategies, the precondition indicates that the transformer leakage inductance is sufficiently small and the influence effect is neglected.

In [22], an S/H logic that can sample and hold the auxiliary voltage at the demagnetization is proposed to discriminate the oscillations due to the resonances between the leakage

inductance and the drain-source capacitance at the MOSFET turn-off, thereby avoiding any abnormal output voltage oscillation due to these parasitic effects, which are independent from the output load and/or input voltage range. Thus, the proposed logic can obtain superior voltage and current regulation. However, the detailed information is not analyzed. As previously mentioned, a time delay block is used to blank the spike voltage after MOSFET turn-off. This block can prevent any negative edge that follows leakage inductance demagnetization from erroneously triggering the zero voltage crossing detection (ZCD) circuit in [23]. In addition, a variable blanking time is proposed, where $T_{\text{BLANK}} = 30 \mu\text{s}$ for $V_{\text{COMP}} = 0.9 \text{ V}$ in the light load based on the voltage on COMP Pin and almost linearly decreases to $T_{\text{BLANK}} = 6 \mu\text{s}$ for $V_{\text{COMP}} = 1.3 \text{ V}$ in the heavy load. This variable blanking time is only used as the frequency fold back for high light-load efficiency and is not useful for accurate PSR regulation.

Although the PSR is well developed, only a small number of studies on the relationship between transformer leakage inductance and the regulations exist. Moreover, although references [7] and [9] considered this issue, no effective solution was proposed. The influence of leakage inductance on the regulation becomes serious with the widespread use of non-sandwich transformer structure. The current and voltage regulations will cause a deteriorative control effect due to the large leakage inductance nature of the non-sandwich structure. In [1], an adaptive blanking time strategy is proposed to improve regulation. However, no detailed model is available to setup the blanking time to obtain a good performance.

Therefore, the PSR control is simple and economical, but its regulation is poor compared with SSR. In addition, PSR is affected by many factors, such as the sampling method, which is highly related to the transformer leakage inductance. Recently, due to a new efficiency standard requirement and Y-capacitorless design for ultra-low leakage current design, a transformer is developed for non-sandwich with large leakage inductance. This paper focuses on solving the PSR CCCV regulation in the Y-capacitorless with large leakage inductance transformer.

Considering the preceding problems mentioned, an adaptive blanking time method for CCCV regulations is proposed in this paper. A mathematical model is constructed based on the transformer leakage inductance and MOSFET parasitical capacitance. This model could be optimized for better standby power and light-load efficiency to satisfy DOE Level VI and COC V5 requirements. In addition, this model has the advantage of excellent regulations among the full-load range without any cost. A dedicated QR flyback PSR control IC with the adaptive blanking time scheme is fabricated by $0.35 \mu\text{m}$ complementary metal-oxide-semiconductor (CMOS) process to verify the effectiveness of the proposed strategy. The method is proven to have excellent

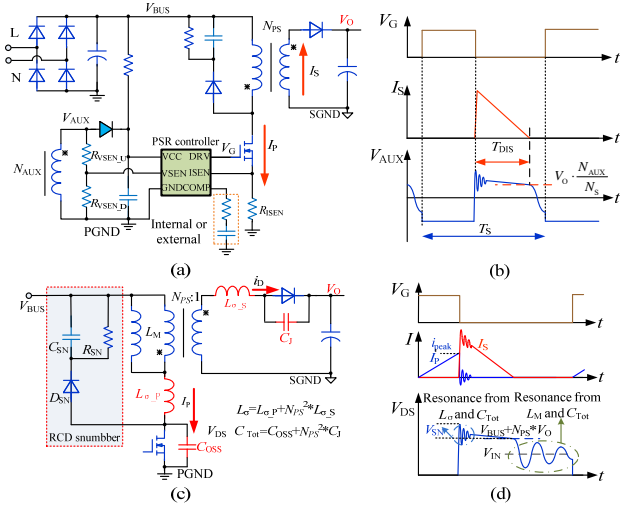


Fig. 1. (a) Ideal PSR flyback converter, (b) Operation waveforms for primary-side sensing, (c) Flyback converter with RCD snubber circuit, and (d) Key waveforms of flyback converter with RCD snubber circuit

performance and easy implementation.

This paper is organized as follows. Section II discusses the motivation of improved CCCV regulation for primary-side converter. Section III describes the mathematical model for blanking time in relation to the transformer leakage inductance and MOSFET output parasitic capacitance. In addition, the improved regulation method is proposed to guarantee the precise sensing. The proposed blanking time strategy IC implementation is presented in Section IV. The experimental results are presented in Section V, and the final section discusses the conclusion.

II. MOTIVATION OF IMPROVING CCCV REGULATION

A. PSR CCCV Regulation Operation Principle

As shown in Fig. 1 (a), the PSR flyback is applied either for charger or LED driver application. Evidently, the opto-coupler and its auxiliary power source are no longer necessary. The V_{BUS} is from the rectified universal AC lines. The output voltage is sensed from the auxiliary winding V_{AUX} and is determined by the voltage divider composed of R_{VSEN_U} and R_{VSEN_D} . The output current is calculated based on the sensed voltage by the ISEN from sensing resistor R_{ISEN} . The feedback CCCV compensation is either externally or internally integrated. The basic principle of PSR control is initially introduced.

As shown in Fig. 1(b), the output voltage in the PSR is sampled from the auxiliary winding and during the OFF time, and the voltage on the auxiliary winding can be deduced by the following:

$$V_{AUX} = (V_{OUT} + V_{D_F}) \frac{N_{AUX}}{N_S}, \quad (1)$$

where N_{AUX} is the turn number of auxiliary winding, N_S is the turn number of the secondary winding, and V_{D_F} is the forward voltage drop of the output rectified diode. At the current zero-crossing point of the output diode, V_{D_F} is nearly zero. Therefore, V_{OUT} is exactly proportional to V_{AUX} . The voltage at this time instant is sampled to be the feedback of the output voltage [1].

The output current is controlled with the primary-side technology when the propagation delay and the parasitic leakage current are neglected [1], [24]. The output current I_{OUT} can be calculated by the following equation:

$$I_{OUT} = \frac{I_{S_pk}}{2} \times \frac{T_{DIS}}{T_S} = I_{P_pk} \times \frac{N_{PS}}{2} \times \frac{T_{DIS}}{T_S}, \quad (2)$$

where I_{S_pk} is the peak current of the secondary side, T_{DIS} is the discharge time of secondary winding energy, T_S is the switching period, and N_{PS} is the transformer turn ratio [1]. The power switch is not immediately turned off, and its current, which is also the primary winding current, continues to rise for some time during the propagation delay.

B. Influence of the Parasitic Parameters and Resistor-Capacitor Diode (RCD) Snubber Circuits

The output voltage is sensed from the auxiliary winding during energy transfer to the secondary winding. Signal discrimination method is included in the feedback signal sampler to guarantee an accurate sample of the output voltage. The reset time of the leakage inductance and the duration of any subsequent leakage inductance ring of the auxiliary winding should be considered to obtain reliable operation.

The reset time of magnetic leakage inductance and the time interval of subsequent rings should be analyzed. The equivalent parasitic capacitance is composed of drain-source non-linear capacitance C_{oss} , various capacitances attributed to the clamped diode, inter-winding capacitances of transformer, and reflected capacitance of the output diode. The elements, which are lump into a ground-referenced capacitor, are designated as C_{Tot} , as shown in Fig. 1(c) [25].

After the primary-side switch turns off, the current flows in C_{Tot} and the drain-source voltage of the MOSFET rapidly increase. The positive slope is not constant due to the MOSFET non-linear capacitance. Thus, the leakage inductance of the transformer will oscillate with the equivalent output capacitance, and the MOSFET drain-source voltage can be represented as follows:

$$V_{A_Spike_1} = V_{DS_Max} = V_{BUS} + N_{PS} \cdot (V_O + V_{D_F}) + i_p \cdot \sqrt{\frac{L_\sigma}{C_{Tot}}} \quad (3)$$

An additional circuit should be applied to protect the main switch by suppressing the overshoot due to the resonance between L_σ and C_{Tot} to an acceptable level. An RCD snubber circuit is generally used, as shown in Fig. 1(c). The key waveforms are shown in Fig. 1(d). The capacitor absorbs the current of the leakage inductance by turning on the snubber diode (D_{sn}) when V_{DS} exceeds $V_{BUS} + N_{PS} \cdot (V_O + V_{D_F})$. The

snubber capacitance is assumed to be sufficiently large; hence, its voltage does not change during one switching period [1], [13], [25].

Considering the leakage current, the worst case is at the minimum input voltage and full-load output condition. The voltage rate of the snubber capacitor should be determined by this worst case. Once V_{SN} is determined, the maximum power dissipated in the snubber circuit is obtained using the following formula:

$$P_{SN} = V_{SN} \frac{i_p \cdot t_s}{2} f_s = \frac{1}{2} L_o i_p^2 \frac{V_{SN}}{V_{SN} - N_{PS} \cdot (V_o + V_{D,F})} f_s, \quad (4)$$

where t_s is the time period of the oscillation ring, and f_s is the switching frequency. In the conventional flyback converter design, the voltage rate of the primary-side power switch is 600 V or 650 V. The margin ratio of the power switch voltage decreases from 90% to 85%. The reflected voltage is designed approximately 80 V in the low output voltage application. Consequently, V_{SN} should be 2–2.5 times the $N_{PS} \times V_o$, N_{PS} is the turn ratio of the power transformer, and i_p is the peak current of the MOSFET [25].

The maximum ripple of the snubber capacitor voltage is obtained as follows:

$$\Delta V_{SN} = \frac{V_{SN}}{C_{SN} \cdot R_{SN} \cdot f_s} \quad (5)$$

Generally, 5%–10% ripple voltage of the snubber capacitor is reasonable. Therefore, the capacitance of the snubber capacitor C_{SN} is calculated based on Equation (5) [1], [25].

C. Traditional blanking method for primary-side sensing

Although the resonant amplitude due to the leakage inductance and parasitic capacitance can be suppressed by the RCD snubber circuit, a long blanking time is adopted to guarantee an accurate sample, as shown in Fig. 2. The time related to the maximum switching frequency is nearly 2–3 μ s [26]–[28]. At the beginning of a MOSFET switching turn-on interval, the primary side sensing is disabled within a blanking time. The feedback signal remains unaffected, and the controller considers the voltage drop and knee point as a voltage spike of resonance in the blanking time. A long blanking time should be designed according to different transformer architectures to guarantee the feedback sampling.

Recently, the μ A level leakage current requirement is increased by cell phone manufacturers to improve the operation stability of touch screen. Moreover, the Y-capacitor is removed to shrink the leakage current. However, such removal results in poor EMI performance. Non-sandwich transformer architecture should be adopted to obtain better EMI performance. This type of architecture has large leakage inductance, which requires long blanking time.

However, the blanking time deteriorates the performance of the system. In addition, this blanking time requires a large dummy load to satisfy the load regulation, thereby constantly

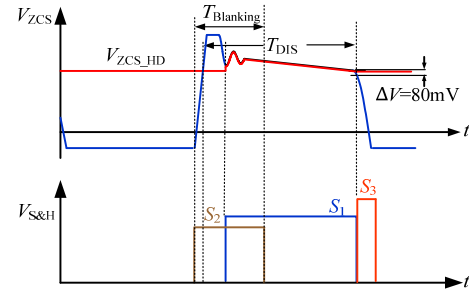


Fig. 2. Traditional long blanking time for primary-side sampling of flyback converter.

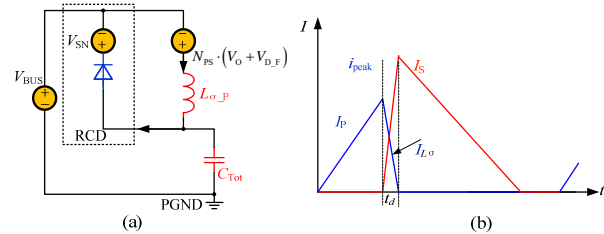


Fig. 3. Primary side sensing of Flyback converter (a) Mathematical model with leakage inductance, (b) Demagnetization of leakage inductance.

causing a considerable amount of power losses in the system. Requirements for the standby power in the DOE Level-VI and COC V5 standard include a standby power less than 75 mW or even 30 mW. The blanking time is not the suitable solution; therefore, finding a better solution for the PSR system is urgent.

III. PROPOSED MATHEMATICAL MODEL AND ADAPTIVE BLANKING TIME STRATEGY

A novel adaptive blanking time strategy is proposed to eliminate the influence of transformer leakage inductance, especially in the Y-capacitorless design, to obtain low leakage current, ultra-low standby power loss, and high efficiency for high power density. The proposed strategy can provide excellent CCCV regulations using any transformer structure.

A. Sampling Blanking Time of Mathematical Model for Flyback Converter with Leakage Inductance

The discriminator block can neglect the leakage inductance reset and ringing to obtain an accurate feedback signal of output voltage from auxiliary winding in the primary-side. Then, sample the auxiliary voltage during the down slope after the ringing is diminished. The error signal at the time when the secondary winding reaches zero current is considered.

An equivalent mathematical model of the flyback converter with leakage inductance is constructed, as shown in Fig. 3(a). A voltage appears across the leakage inductance as

$V_{SN} - N_{PS} \times (V_O + V_{D,F})$ due to the clamp action. The reset time of the leakage inductance begins at the primary-switch turn-off time. When the primary-side switch turns off, the secondary diode net current is zero and then all the primary currents are diverted by the leakage inductance to charge C_{Tot} . As the leakage inductance resets, the secondary current builds up and reaches its peak point with the completion of the reset event. As shown in Fig. 2(c), the leakage inductance delays the occurrence of the secondary current by the time t_d and affects its peak value. The energy stored in the leakage inductance plus the extra energy stolen from the primary inductance is dissipated in the clamping network [28]–[31].

The leakage inductance reset time t_d is determined using the following equation:

$$t_d = \frac{I_p}{V_{SN} - N_{PS} \cdot (V_O + V_{D,F})} = \frac{I_p \cdot L_\sigma}{V_{SN} - N_{PS} \cdot (V_O + V_{D,F})} \quad (6)$$

The resonant t_r can be expressed as follows:

$$t_r = \frac{2\pi}{\sqrt{L_\sigma \times C_{Tot}}} \quad (7)$$

The resonant amplitude can be expressed as follows:

$$V_{A_pike_1} = i_{peak} \cdot \sqrt{\frac{L_\sigma}{C_{Tot}}} \quad (8)$$

The first part is the interval of the leakage inductance reset pedestal, t_d . Maintaining the leakage reset time t_p less than 300 ns for I_{P_Min} and less than 1.5 μ s for I_{P_Max} is important because it can imitate the secondary current wave attenuation, followed by a sharp downward slope [24]–[28]. The second part is the ring amplitude on the auxiliary winding, which follows t_d . The peak-to-peak voltage should be less than the minimum of the distinguished voltage of the primary-side controller. Generally, the leakage energy requires one to three cycles of oscillation. Thus, the minimum blanking time is determined using the following equation:

$$t_{Blk} = t_d + n \cdot t_r, \quad (8)$$

where n is the oscillation period, in which the amplitude is attenuated to less than the distinguished voltage. The oscillation period is related to the load condition and parameter of the RCD snubber circuit.

Therefore, the blanking time model can be expressed as follows:

$$t_{Blk} = \frac{I_p \cdot L_\sigma}{V_{SN} - N_{PS} \cdot (V_O + V_{D,F})} + n \cdot \frac{2 \cdot \pi}{\sqrt{L_\sigma \times C_{Tot}}} \quad (9)$$

Based on the preceding equation, the blanking time is large when the load is heavy and decreases with decreasing load. Simultaneously, the blanking time should be long if the leakage inductance is large.

B. Voltage Spike Resonant Time Relationship with the Load Condition

Considering Equations (3) and (4), the relationship

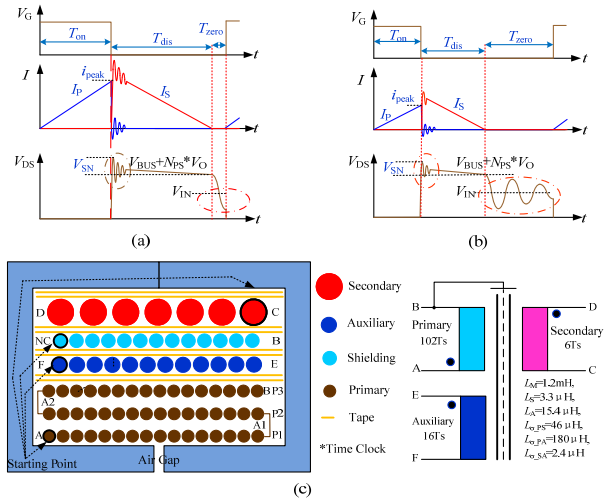


Fig. 4. Flyback converter with RCD circuit (a) Heavy load operation, (b) Light load operation, and (c) Transformer architecture and tested leakage inductance.

between the amplitude of resonant spike and the load is shown in Figs. 4(a) and 4(b).

At the light load condition, the resonant energy is easily damped by the RCD snubber circuit in a short time. However, damping the resonant energy in the heavy load condition is difficult due to the large resonant energy. Thus, a longer blanking time is required in the heavy load than in the light load to avoid the resonant spike.

A Y-capacitorless 5V/2.1 flyback prototype with μ A level leakage current is developed to understand the experimental verification. A non-sandwich architecture transformer is specially designed to obtain better EMI performance, as shown in Fig. 4(c). This transformer has large leakage inductance and causes a large resonant spike.

The measured data in Fig. 4(c) show that the leakage primary-side winding to auxiliary winding leakage inductance is 180 μ H compared with 1.2 mH magnetizing inductance. This value is over 10% and is extremely large; thus, an RCD snubber circuit should be added. The discharge resistance is 470 k Ω , and the clamped capacitor value is 470 pF. A slow recovery diode S1M is also applied. The MOSFET drain-source voltage is recorded at different loads based on the preceding components shown in Figs. 5(a)–(c) to obtain a clear understanding of the operation.

The test waveforms show that the resonant amplitude and time vary with load condition. According to the waveforms, the first resonant spike is increased by the leakage inductance and the total parasitic capacitance. The resonant frequency and the amplitude are obtained using Equations (7) and (8) [25]. The amplitude of the resonant spike is related to the load. As the load increases, the leakage inductance energy from the transformer requires time or a large RCD snubber circuit for damping. The traditional PSR controller requires a long blanking time to avoid the resonant voltage spike on the auxiliary winding [1].

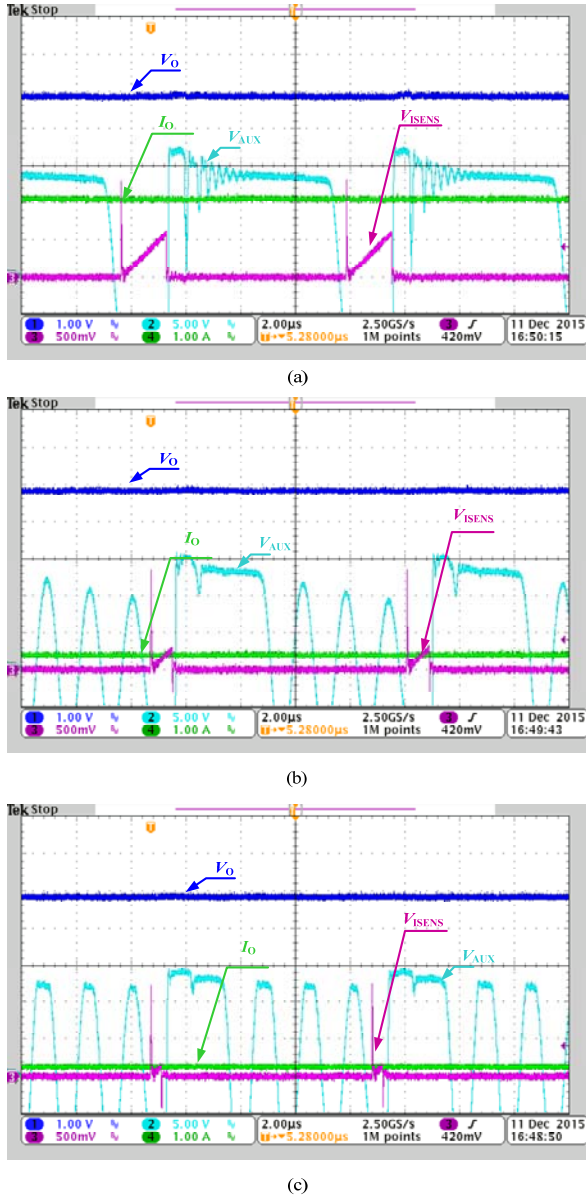


Fig. 5. Flyback operation waveforms at different loads (a) Full load, (b) Medium load, and (c) Light load (CH1: V_O , CH2: V_{AUX} , CH3: V_{SENS} , CH4: I_O).

C. Proposed Adaptive Blanking Time Strategy

The resonant time is obviously long if the load is heavy. The adaptive blanking time, which is related to the load strategy, is proposed as shown in Fig. 6(a), where V_C is the internal compensation voltage that represents the output power.

In heavy load condition, the blanking time is increased to guarantee precise sampling after the resonant spike. The blanking time has the maximum value of 2 μ s. Simultaneously, the switch has a long turn-off time to maintain accurate sampling. When the load decreases, the required blanking time to obtain an accurate feedback also decreases. In extremely light load condition, the blanking

time is decreased to a minimum value to improve the light load and no load efficiency. This minimum blanking time determines the standby power loss and regulations and should be larger than the minimum turn-off time of the converter. Moreover, the minimum turn-off time should be designed according to the blanking time.

The proposed adaptive blanking time controlled curve related to the internal compensation voltage can guarantee an excellent regulation. The proposed curve is especially suitable for the Y-capacitorless converter with non-sandwich transformer structure, which has a large leakage inductance in cellphone chargers or network adapter applications.

With the proposed strategy, the feedback voltage sampler can guarantee an accurate feedback sampling in each switching cycle, and the CC regulation can also be infallibly calculated whatever transformer structure and manufacture process are applied. The proposed strategy can improve the mass production yield, reduce system cost, and improve the MTBF product.

IV. INTEGRATED CIRCUIT IMPLEMENTATION OF PROPOSED STRATEGY

A PSR controller with the proposed strategy for CCCV application is designed and fabricated to verify the proposed technology. The design and operation principles of voltage feedback are described in reference [1] in detail.

The proposed adaptive blanking time strategy is implemented, as shown in Fig. 6(b). An adaptive current source controlled by the constant current feedback V_{IOUT_SEN} is used to charge the constant capacitance. Then, the capacitor voltage is used for comparison with V_{Ref} to obtain S_2 , which is used to implement the adaptive blanking time. The current source curve is shown in Fig. 6(b).

The current source is controlled by the V_{IOUT_SEN} , which is related to the load condition, as follows:

$$I_{BLK}(V_{IOUT_SEN}) = \begin{cases} I_{BLK_1}; V_{IOUT_SEN} \leq V_{IOUT_1} \\ I_{BLK_1} + (I_{BLK_2} - I_{BLK_1}) \cdot \frac{V_{IOUT_SEN} - V_{IOUT_1}}{V_{IOUT_2} - V_{IOUT_1}} \\ ; V_{IOUT_1} \leq V_{IOUT_SEN} \leq V_{IOUT_2} \\ I_{BLK_2}; V_{IOUT_SEN} \geq V_{IOUT_2} \end{cases} \quad (10)$$

Based on the preceding current source mentioned, the blanking time can be adjusted through I_{BLK_1} , I_{BLK_2} , V_{IOUT_1} , and V_{IOUT_2} . The curve can be optimized and designed for improved regulation and ultra-low standby power.

The method samples and holds divided voltage V_{SEN} from the auxiliary winding voltage during the discharge time T_{DIS} . The divided voltage is labeled as V_{ZCS_HD} . Then, it samples and holds the V_{ZCS_HD} at the ending instant of T_{DIS} time interval as V_{ZCS_FB} . The method also filters the V_{ZCS_HD} to obtain V_{ZCS_OVP} . V_{ZCS_FB} is used for feedback signal and

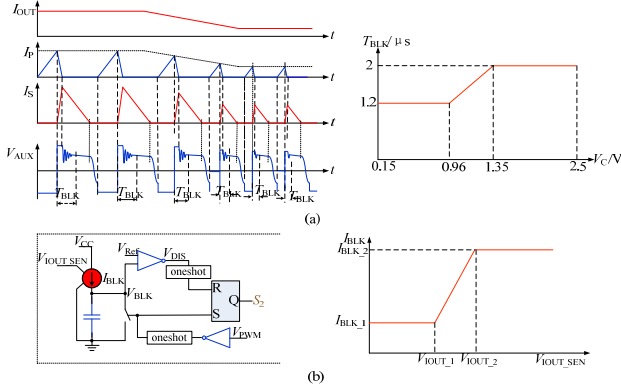


Fig. 6. (a) Proposed adaptive blanking time technology (b) Operation principle of adaptive blanking time.

output voltage regulation.

$$V_{ZCS_FB} = \frac{R_{VSEN_D}}{R_{VSEN_U} + R_{VSEN_D}} \cdot \frac{N_{AUX}}{N_S} \cdot (V_{OUT} + V_{D_F}), \quad (11)$$

where V_{D_F} is the forward voltage drop of the secondary diode. N_S is the turn number of the secondary-side winding. This voltage drop is fixed and sufficiently small. Thus, V_{ZCS_FB} can represent the precise output voltage in real time [1].

V_{ZCS_OVP} is the feedback of the output overvoltage protection. If the V_{ZCS_OVP} is more than $120\% \times V_{VSEN_REF}$, then the OVP is triggered to protect the load equipment.

The output current is deduced in Equation (3). This current samples and holds the peak value of the R_{SEN} voltage to obtain $I_{PP} \times R_{ISEN}$. With the internal T_{DIS} and T_S , the output current can be expressed as follows:

$$V_{IOUT_SEN} = I_{PP} \cdot R_{ISEN} \cdot \frac{T_{DIS}}{T} = 2 \cdot I_{OUT} \cdot R_{ISEN} \cdot \frac{R_{ISEN}}{N_{PS}}, \quad (12)$$

where V_{IOUT_SEN} is the feedback for the output current regulation. The reference of V_{IOUT_SEN} is I_{REF} of 0.42 V.

The PSR is controlled with PWM at the heavy load and PFM at the light load to improve the efficiency. The light load efficiency should be optimized through the frequency control curve. The switching frequency curve is controlled, as shown in Fig. 7(a), and the peak current voltage is controlled, as the curve indicated in Fig. 7(b).

At the heavy load condition, when the COMP voltage is above 1.9 V, the converter operates at the QR mode to obtain high efficiency. When the load decreases and the COMP voltage is between 1.3 and 1.9 V, the peak voltage of ISEN is constant at 0.45 V, and the switching frequency decreases with the load condition. Then, the switching frequency remains constant again, and the peak voltage of ISEN decreases with load when the COMP voltage is between 0.7 and 1.3 V. When the COMP is lower than 0.7 V, the peak voltage of ISEN becomes constant at 0.15 V, and the switching frequency decreases to a minimum value of 500 Hz. If the load increases, then the converter operates at the opposite direction.

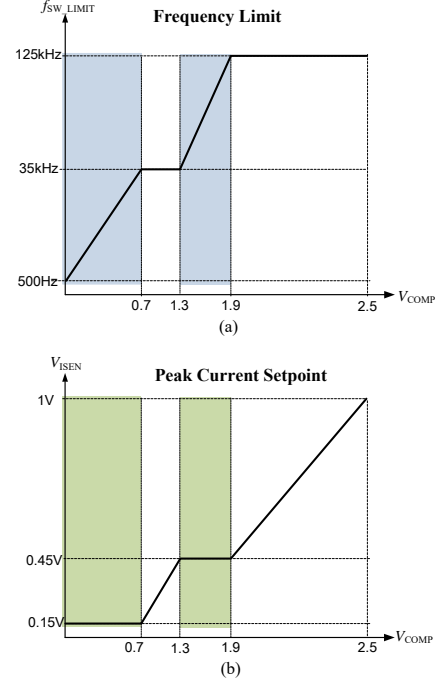


Fig. 7. PWM and PFC control curve (a) Switching frequency control curve and (b) Peak current voltage control curve.

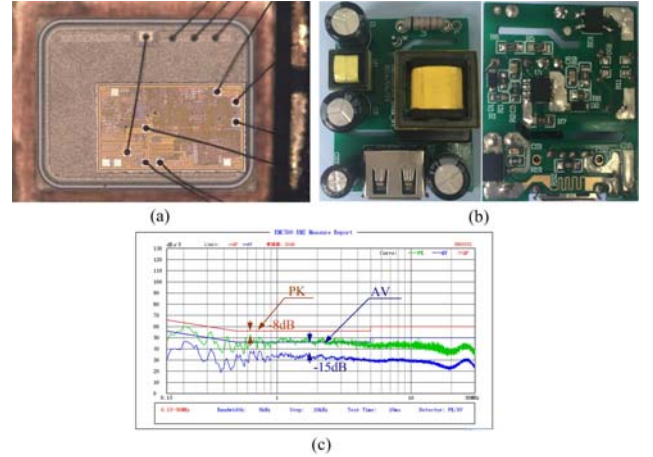


Fig. 8. Proposed strategy (a) Layout of proposed IC with MOSFET co-packaged, (b) 5V/2.1A prototype, and (c) L-line EMI spectrum by the non-sandwich transformer without Y-cap at 230 Vac.

V. EXPERIMENTAL VERIFICATION

A QR PSR flyback controller with the proposed strategy IC is designed in $0.35 \mu\text{m}$ CMOS process. A $0.8 \times 1.6 \text{ mm}^2$ controller and $1.76 \times 2.2 \text{ mm}^2$ 600 V 4.4Ω MOSFET is integrated into the power IC. The layout is shown in Fig. 8(a) and is integrated into an SO8 package.

The newly designed prototype is shown in Fig. 8(b). Owing to the Y-capacitorless for the μA level leakage current, the non-sandwich architecture power transformer is designed based on EE16 core, as shown in Fig. 3(c). The leakage

TABLE I
PROTOTYPE SPECIFICATION

Input	L and N 2-wire, 85Vac–264Vac 47 Hz–63 Hz,
Output	5V/2.1A, $V_{\text{ripple}} < 100 \text{ mV}$ and $I_{\text{OCP}} < 2.3 \text{ A}$ with USB port
Efficiency	Energy star Level 6 and No load loss $< 75 \text{ mW}$
EMC and leakage current	EN55022 Class B limits; Leakage current $< 0.1 \text{ mA}$
Size	$W \times L \times H = 31.5 \text{ mm} \times 40 \text{ mm} \times 19.6 \text{ mm}$
Switching frequency	QR flyback with 70 kHz at full load in 115 Vac

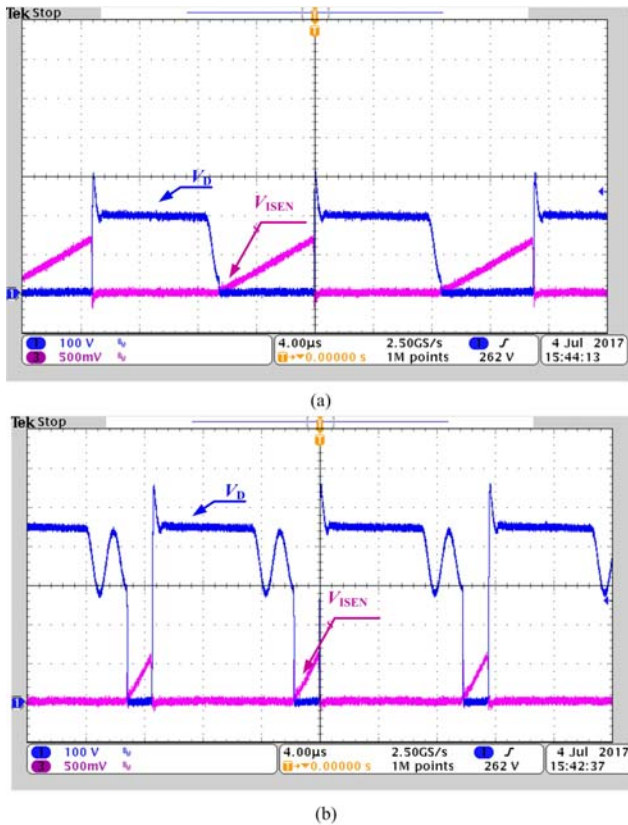


Fig. 9. QR operation of the proposed converter (a) Full load at 90 Vac input, (b) Full load at 264 Vac input (CH1: V_D , CH3: V_{ISENS}).

inductance is also measured and shown in Fig. 3(c). Evidently, this prototype is ample and facilitates easy massive production. With the Y-capacitorless design, the measured leakage current from the primary to the secondary side is approximately 75 μA , which can easily satisfy the cell phone charger requirement. In addition, the prototype is also excellent for EMI performance, as shown in Fig. 8(c).

A 5V/2.1A flyback prototype is developed for smart cell phone or touch pads to verify the proposed control strategy. The specifications of the prototype are shown in Table I.

The converter is implemented by QR operation; thus, the primary-side switch turns on at the valley of oscillation, as shown in Figs. 9(a) and (b) at 90 input and 264 Vac inputs, respectively. The converter can also improve the efficiency by decreasing the turn-on loss.

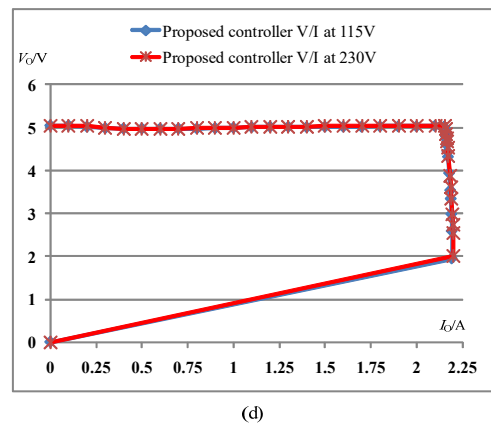
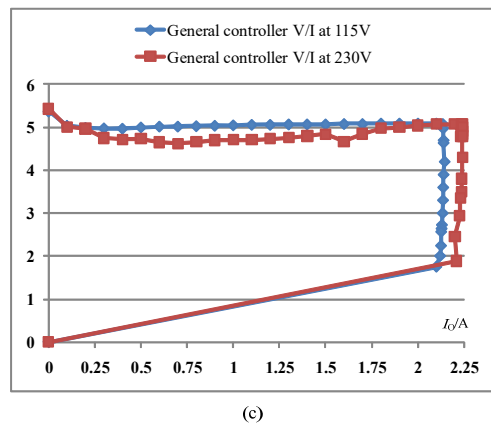
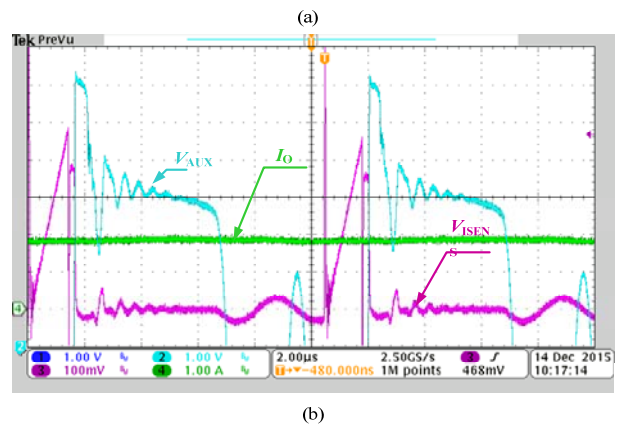
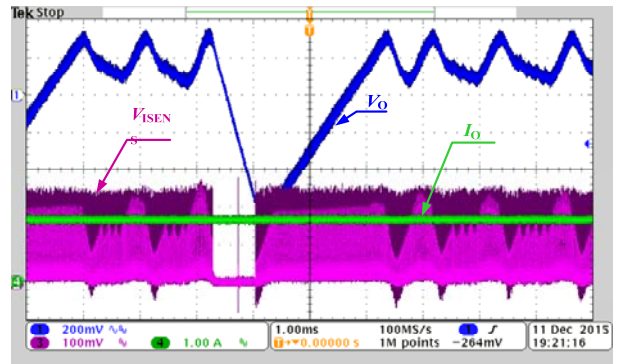


Fig. 10. (a) Unstable waveforms of the traditional method, (b) Zoomed in unstable waveforms (CH1: V_O , CH2: V_{AUX} , CH3: V_{ISENS} , CH4: I_O), (c) Regulations of the traditional method, and (d) Regulations of the proposed method.

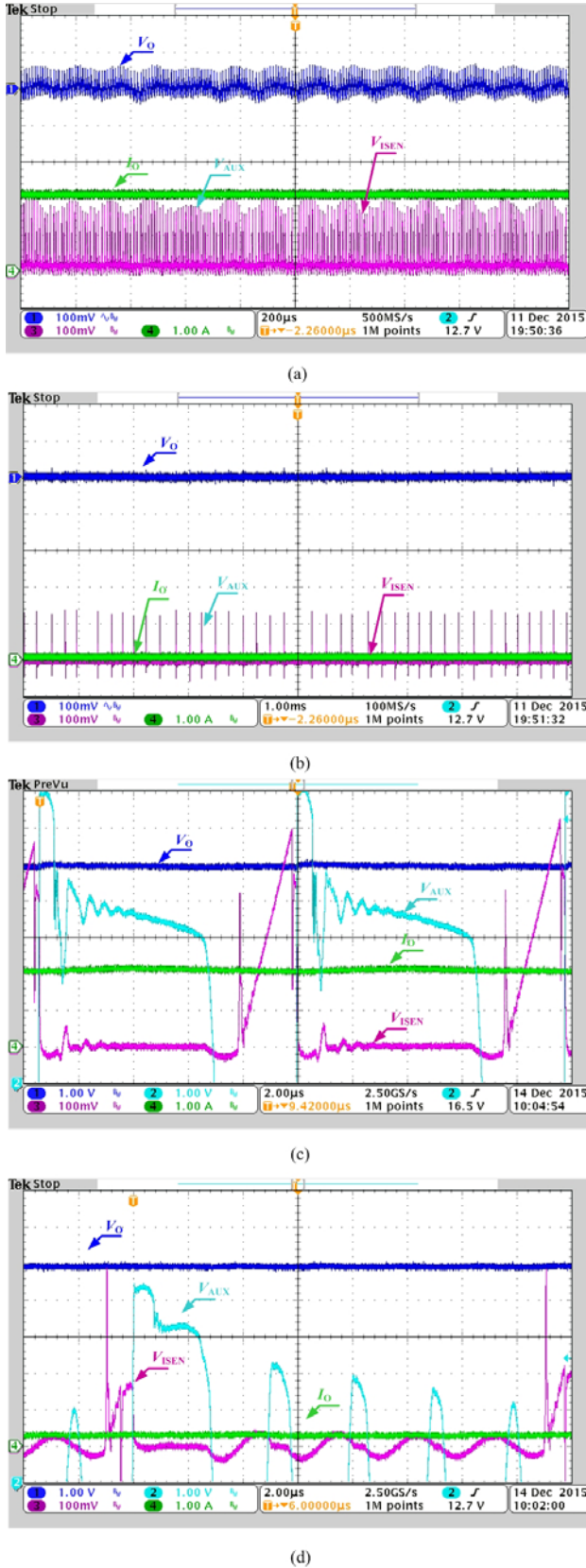


Fig. 11. Operation waveforms of the proposed method (a) 5 V/2.1 A waveforms, (b) No load condition, (c) Heavy load, and (d) No load with minimal blanking time (CH1: V_O , CH2: V_{AUX} , CH3: V_{ISENS} , CH4: I_O).

TABLE II
EFFICIENCY OF CONVERTER AT CABLE END

Input voltage/V	Efficiency performance/%					
	100% Load	75% Load	50% Load	25% Load	Average Efficiency	No Load (mW)
90	77.6	-	-	-	-	21.64
115	79.96	81.00	81.53	82.38	81.22	23.02
230	80.39	81.07	81.32	80.68	80.87	34.82
264	80.08	-	-	-	-	41.09

TABLE III
EFFICIENCY OF CONVERTER AT BOARD END

Input voltage/V	Efficiency performance/%					
	100% Load	75% Load	50% Load	25% Load	Average Efficiency	No Load (mW)
90	82.16	-	-	-	-	21.64
115	84.65	84.6	84.02	83.71	84.24	23.02
230	85.11	84.68	83.8	81.99	83.9	34.82
264	84.79	-	-	-	-	41.09

To understand the cable loss in the system, the board end efficiency without the cable loss is also measured, as shown in Table III.

In the traditional PSR controlled converter with constant blanking time, the control system becomes unstable due to inaccurate sampling, whereas the ring amplitude is above $\Delta V_{AUX} = (R_{ZCD_U} + R_{ZCD_D}) / R_{ZCD_D} \times \Delta V = 0.95$ V due to large leakage inductance.

The resonant time is larger than the conventional controller's constant blanking time of $1.3 \mu\text{s}$ due to the large leakage inductance; therefore, the sample time is in the valley of the ring, and the sampled voltage and calculated current are inaccurate. Then, the system becomes unstable. The output ripple is shown in Fig. 10(a), and the auxiliary winding voltage is also measured, as shown in Fig. 10(b). As shown in Fig. 10(c), the output ripple has poor regulation. However, using the proposed solution, the CCCV regulation is improved by 1%–2% in the same design, as shown in Fig. 10(d).

Compared with the traditional method, the proposed method has smaller output ripple. The output voltage ripple and ISENS voltage are measured. The waveforms of the proposed method are shown in Fig. 11(a), which demonstrates stability and low ripple noise. A low-frequency ripple noise of approximately 6 kHz, which is due to the frequency modulation for good EMI performance, is observed. The no-load waveforms are shown in Fig. 11(b), which demonstrates stability and low ripple noise.

VI. CONCLUSIONS

An adaptive blanking scheme is proposed in this paper for the CC and CV regulations to acquire accurate detection among full-load range in each switching cycle. Considering

the transformer leakage inductance, regulation influence factors of the primary-side control are analyzed. A mathematical model for the blanking time related to the transformer leakage inductance and the MOSFET parasitic capacitance is established to obtain improved standby power and light-load efficiency. With the proposed strategy, the fabricated control IC provides excellent load regulations and ultra-low no-load power loss.

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