Analysis of RF-DC Conversion Efficiency of Composite Multi-Antenna Rectifiers for Wireless Power Transfer

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Abstract

This paper studies the radio frequency to direct current (RF-DC) conversion efficiency of rectennas applicable to wireless power transfer systems, where multiple receive antennas are arranged in serial, parallel or cascaded form. To begin with, a 2.45 GHz dual-diode rectifier is designed and its equivalent linear model is applied to analyze its output voltage and current. Then, using Advanced Design System (ADS), it is shown that the rectifying efficiency is as large as 66.2% in case the input power is 15.4 dBm. On the other hand, to boost the DC output, three composite rectennas are designed by inter-connecting two dual-diode rectifiers in serial, parallel and cascade forms; and their output voltage and current are investigated using their respective equivalent linear models. Simulation and experimental results demonstrate that all composite rectennas have almost the same RF-DC conversion efficiency as the dual-diode rectifier, yet the output of voltage or current can be significantly increased; in particular, the cascade rectenna obtains the highest rectifying efficiency.

***Keywords*:** RF-DC conversion efficiency, series rectenna, parallel rectenna, cascade rectenna, wireless power transfer

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1. Introduction

With the rapid development of Internet of Things (IoT) technology, numerous wireless terminals with low-power consumptions are widely deployed in practice, e.g., sensors and radio frequency identification (RFID) tags. To resolve the painstaking power charging problem inherent in wireless terminals and the shortage of battery endurance, wireless power transfer (WPT) technique has received extensive attention from both academia and industry communities. To realize WPT in reality, many techniques like inductive coupling, resonant coupling, laser beaming and RF-based WPT have emerged in recent years. However, neither near-field coupling nor laser beaming is suitable for long-distance wireless power transfer, because of limited propagation distance and potential human safety concerns [1]. To speed up the application of RF-based WPT, improving the efficiency of RF power transfer is imperative.

The efficiency of a RF-based WPT system depends upon three parts: transmit (Tx) efficiency at the transmitter, free space propagation efficiency and receive (Rx) efficiency at the receiver [2]. In general, a rectenna consists of an Rx antenna and a rectifier and thus the Rx efficiency can be further decomposed into the antenna's Rx efficiency and rectifier's efficiency. To improve the antenna's Rx efficiency, there have been many publications focused on antenna quantity, polarization characteristic and/or array layout. For instance, in [3] a folded dipole antenna and a 3×3 array was designed and the effect of the number of antenna elements on Rx efficiency was explored. In [4], the performance of dual-patch, six-patch, and 16-patch antennas was extensively compared. In [5], a right-hand circularly polarized (RHCP) antenna and a left-hand circularly polarized (LHCP) antenna were designed, and the effect of polarization on antenna's Rx efficiency was investigated. For array layout, the effect of flat and random dispositions of rectifying antenna on the Rx efficiency was studied in [6]. Recently, interference inherent in wireless applications was seen as a new energy source which can be harvested by rectenna to improve the Rx efficiency [7][8].

To analyze the performance of rectifiers, several analytical models were proposed in the open literature, mainly including linear and nonlinear models. As for the linear one, there are two different approaches: one is to establish the relationship between input and output powers by use of the turn-on angle [9][10]; the other is to analyze the current by using the small signal model of diode [11]. Clearly, both approaches need to determine the optimal load prior to simulation experiments. On the other hand, for the nonlinear model, Ritz–Galerkin technique was widely used to investigate the closed-form of output voltage and it outperforms linear one in terms of accuracy at the cost of complexity [12][13]. In practice, if the load is already known, the linear rather than nonlinear mode is preferred.

As for the analytical linear models of composite rectennas, in [14] several kinds of rectenna arrays were analyzed, such as H-H series, H-H parallel, H-L series, H-L parallel, L-L series and L-L parallel, where "H" denotes the rectenna with higher output while "L" means the rectenna with lower output. The authors of [15] computed the resistance and inductance of transmission wire between the first stage and the second stage in cascade rectenna so as to explore the difference between cascade and series or parallel connection.

To perform theoretical analysis with equivalent circuit, simple linear models are developed in this paper to describe the output characteristics of two-stage series/parallel/cascade rectennas. We start with a basic dual-diode rectifier and then three composite rectennas are developed, by arranging two dual-diode rectifiers in serial, parallel and cascaded forms. Our analytical and experimental results show that the rectifying efficiency of the dual-diode

rectifier can reach as high as 73.9%, and the composite arrays enables boost the output current or voltage without degrading the rectifying efficiency. In particular, series rectenna gets its maximum conversion efficiency as high as 76.7%, and exports twice of voltage than the single rectenna while they have almost the same output current. The maximum conversion efficiency of parallel rectenna is 78%, and it has double output current than the single rectenna while they have almost the same output voltage. Among the four rectennas under study, the cascade rectenna obtains the highest conversion efficiency being 79.2%.

The rest of this paper is organized as follows. In Section 2, after introducing the small signal model of diode, the performance of dual-diode rectifying circuit is analytically investigated. Then, Section 3 analyzes the rectifying efficiency of three composite multi-antenna rectifying circuits, including series, parallel and cascade rectennas. Both simulation results in ADS and physical experimental results collaborate the analysis. Finally, Section 4 concludes the paper.

2.RF-DC Conversion Efficiency of Dual-Diode Rectifying Circuit

Since dual-diode rectifier is a basic composition unit of composite multi-antenna rectennas to be investigated later, this section is dedicated to analyzing the rectifying efficiency of dual-diode rectifier, based on the small signal model of diode.

2.1 The Small Signal Model of Diode

As illustrated in **Fig. 1**, the small signal model of diode consists of four parts: an ideal diode D_i, a serial resistance R_s, a parallel capacitance C_j, and a parallel resistance R_j. Compared with R_j, the voltage drop on R_s is generally very small and can be ignored in practice [11]. To establish the relationship between the input and output voltages, the currents through D_i, C_j and R_j are explicitly computed as follows.

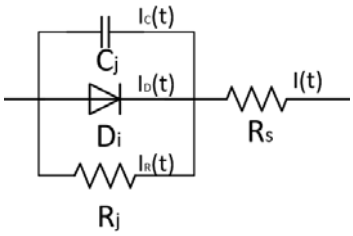

Fig. 1. The small signal model of diode.

To begin with, recalling that the volt-current (V-I) characteristic of an ideal diode is given by

$$I_D(t) = I_S\left(\exp\left(\frac{V_D(t)}{NV_T}\right)-1\right), \tag{1}$$

where $I_D(t)$ denotes the current through D_i, I_S means the saturation current, $V_D(t)$ stands for the applied voltage, N is the ideal factor of the diode and V_T represents the thermal voltage [16], the value of C_j can be determined by

$$C_j(t) = C_{j0}\left(1-\frac{V_D(t)}{V_J}\right)^{-M}, \tag{2}$$

where C_{j0} stands for the zero-bias barrier capacitance, V_J is the built-in voltage, M is the capacitance gradient factor with a default value being 0.5. By expressing the barrier capacitance with respect to its harmonic components, we have

$$C_j(t) = C_{j0} + C_1 \cos(\omega t - \phi) + C_2 \cos(2\omega t - \phi) + \cdots, \tag{3}$$

where ϕ denotes the shift of incident power phase. In practice, to suppress the harmonic ones, a microstrip transmission line with a length L mm is generally strung at the end of the diode. As a result, (3) reduces to

$$C_j(t) = C_{j0} + C_1 \cos(\omega t - \phi). \tag{4}$$

On the other hand, it is straightforward that the current through barrier capacitance can be expressed as

$$I_C(t) = \frac{\mathrm{d}(C_j(t)V_D(t))}{\mathrm{d}t}. \tag{5}$$

Afterwards, the current through R_j is readily given by

$$I_R(t) = \frac{V_D(t)}{R_j}. \tag{6}$$

Finally, the current over R_s is given by

$$I(t) = I_D(t) + I_C(t) + I_R(t).$$

2.2 The Model of Dual-Diode Rectifier

Fig. 2 shows the circuit model of dual-diode rectifier. When the circuit reaches steady state, the voltage drop on the storage capacitor C_1 is known as equilibrium voltage, which is to be analyzed in the following.

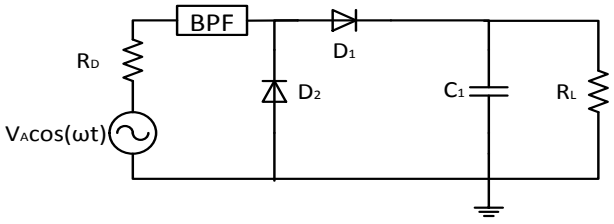

Fig. 2. Circuit model of dual-diode rectifier.

As shown in **Fig. 2**, the incoming RF voltage source is usually expressed as a cosine signal. In its positive half-cycle, diode D_1 turns on whereas D_2 cuts off. Consequently, the charges that enter C_1 can be computed by integration as

$$\Delta Q_{in} = \int_0^{\frac{T}{2}} I_D(t)dt + \int_0^{\frac{T}{2}} I_C(t)dt + \int_0^{\frac{T}{2}} I_R(t)dt, \tag{7}$$

where T denotes the cycle of RF signals and I_D, I_C and I_R are previously given by (1), (5) and (6), respectively. Since R_j is usually as large as hundreds of megaohm, $I_R(t)$ can be approximated to zero and, thus, the third term on the right-hand side (RHS) of (7) is negligible. The first term on the RHS of (7) is

$$\begin{aligned}\int_0^{\frac{T}{2}} I_D(t)dt &= \int_0^{\frac{T}{2}} I_S\left(\exp\left(\frac{V_D(t)}{NV_T}\right)-1\right)dt \\ &= I_S\exp\left(-\frac{V_C}{NV_T}\right)\int_0^{T/2}\exp\left(\frac{V_A\cos(\omega t)}{NV_T}\right)dt+\frac{TI_S}{2} \\ &= \frac{I_S T}{2}\left(\exp\left(\frac{-V_C}{NV_T}\right)\mathrm{I}_0\left(\frac{V_A}{NV_T}\right)-1\right),\end{aligned} \tag{7}$$

where $\mathrm{I}_0(z)$ denotes the zero-order modified Bessel function of first kind [17]. Finally, the second term on the RHS of (7) is readily computed as

$$\int_0^{\frac{T}{2}} I_C(t)dt = 2C_{j1}V_C - 2V_{j0}V_A. \tag{9}$$

In the negative half-cycle of the source, diode D_1 cuts off whereas D_2 turns on. At this time, the impedance of D_1 is very large so as to reject current released from storage capacitor. Therefore, the entire current will flow towards the terminal, and the charges released from the capacitor in this half-cycle is computed as

$$\Delta Q_{out} = \int_{\frac{T}{2}}^{T}\frac{V_C}{R_L}dt = \frac{V_C T}{2R_L}. \tag{10}$$

When the charges entering the capacitor equals those leaving it, it reaches steady state, and we use $\tilde{V}_C$ instead of V_C to represent the output voltage in the steady state. In other words, we have

$$\Delta Q_{in} = \Delta Q_{out}, \tag{11}$$

which implies

$$\frac{I_S T}{2}\left(\exp\left(\frac{-\tilde{V}_C}{NV_T}\right)\mathrm{I}_0\left(\frac{V_A}{NV_T}\right)-1\right)+2C_{j1}\tilde{V}_C-2C_{j0}V_A=\frac{\tilde{V}_C T}{2R_L}. \tag{12}$$

After performing some algebraic manipulations, (12) can be simplified as

$$\frac{\frac{I_S T}{2}\exp\left(\frac{-\tilde{V}_C}{NV_T}\right)\mathrm{I}_0\left(\frac{V_A}{NV_T}\right)}{2C_{j0}V_A+\frac{I_S T}{2}}=\frac{\tilde{V}_C\left(\frac{T}{2R_L}-2C_{j1}\right)}{2C_{j0}V_A+\frac{I_S T}{2}}+1. \tag{13}$$

Taking natural logarithm on both sides of (13) yields

$$\ln\frac{I_S T}{2}+\ln\mathrm{I}_0\left(\frac{V_A}{NV_T}\right)-\ln\left(2C_{j0}V_A+\frac{I_S T}{2}\right)+\frac{-\tilde{V}_C}{NV_T}=\ln\left(\frac{\tilde{V}_C\left(\frac{T}{2R_L}-2C_{j1}\right)}{2C_{j0}V_A+\frac{I_S T}{2}}+1\right). \tag{14}$$

Next, taking proper values of parameters as specified in the next subsection, the first term involved in the logarithm function on the RHS of (14) can be approximately given by

$$\tilde{V}_C\left(\frac{T}{2R_L}-2C_{j1}\right)\Big/\left(2C_{j0}V_A+\frac{I_S T}{2}\right)\approx 2\times 10^{-3}<<1. \tag{15}$$

Finally, by using Taylor's series approximation to the RHS of (14), i.e., $\log(1+x)\approx x$, the equilibrium voltage can be finally obtained:

$$\tilde{V}_C=\frac{2C_{j0}V_A NV_T}{\left(\frac{T}{2R_L}-2C_{j1}\right)NV_T+2C_{j0}V_A+\frac{I_S T}{2}}\ln\left(\frac{\frac{I_S T}{2}\mathrm{I}_0\left(\frac{V_A}{NV_T}\right)}{2C_{j0}V_A+\frac{I_S T}{2}}\right). \tag{16}$$

Notice that (16) corresponds to the case that an ideal BPF is applied in Fig. 2. In practice, however, microstrip BPF is generally exploited**,** which may have the characteristics of capacitance due to its in-built physical structure. In such a case, (16) can be rewritten as

$$\tilde{V}_C=\alpha\times\frac{2C_{j0}V_A NV_T}{\left(\frac{T}{2R_L}-2C_{j1}\right)NV_T+2C_{j0}V_A+\frac{I_S T}{2}}\ln\left(\frac{\frac{I_S T}{2}\cdot\mathrm{I}_0\left(\frac{V_A}{NV_T}\right)}{2C_{j0}V_A+\frac{I_S T}{2}}\right), \tag{17}$$

where $\alpha>1$ denotes the voltage amplification factor. When the capacitance of microstrip BPF equals C_1, the circuit shown in **Fig. 2** is equivalent to a double-voltage rectifier with $\alpha=2$.

2.3 Simulation Results

To investigate the output performance of dual-diode rectifier, simulation tests are performed in ADS.

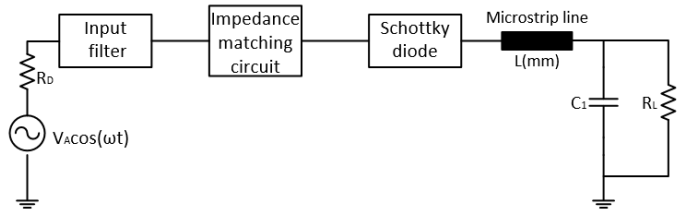

Fig. 3. Rectenna structure

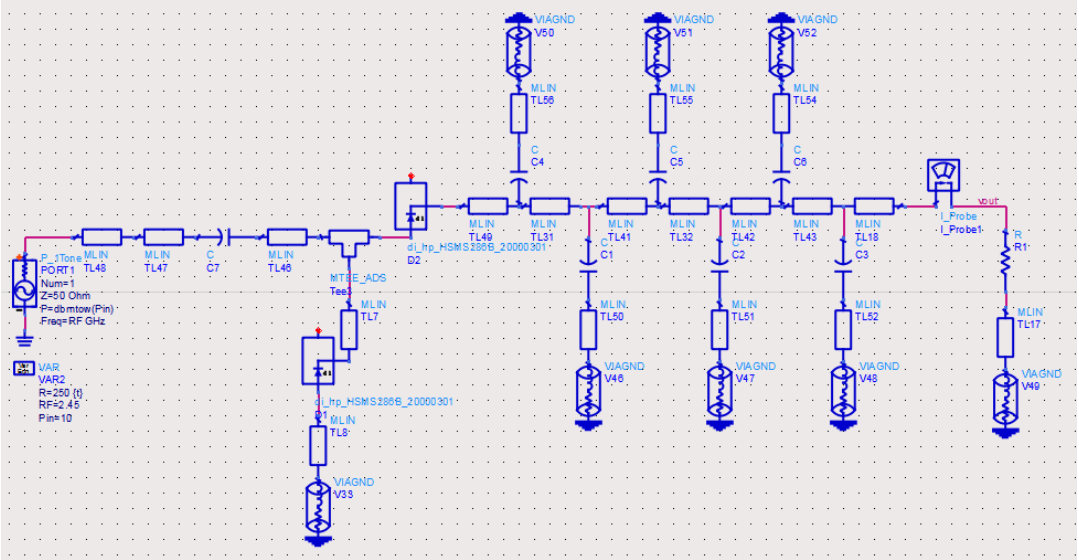

Fig. 4. The layout of a basic dual-diode rectifier in ADS.

Fig. 3 shows the structure of a basic single-element rectenna used in our simulation tests, which consists of eight parts: an RF source $V_A\cos(\omega t)$, an equivalent resistance of antenna R_D, an input filter, an impedance matching circuit, a Schottky diode (which is implemented by double diodes), an microstrip transmission line, a storage capacitor C_1 and a load resistance R_L [18]. With proper choice of frequency 2.45 GHz, dielectric substrate (F4B), Schottky diode (HSMS-286B), storage capacity (100 pF), and load resistance (250 Ohm), the PCB layout of the circuit is shown in **Fig. 4**. After performing some design optimization, our simulation results show that the maximum RF-DC conversion efficiency is 66.2% in the case of the input power being 15.4 dBm (cf. **Fig. 9**). Correspondingly, the DC output voltage and current are 2.395 V and 10 mA, respectively, (cf. **Figs. 10-11**).

For comparison purposes, **Table 1** records the numerical results computed as per (16) compared with simulation results. In the simulation tests, the parameter setting includes $C_{j0}=0.18\,\text{pF}$, $C_{j1}=0.01\,\text{pF}$, $N=1.08$, $V_T=26\,\text{mV}$, $I_S=24.5\,\text{nA}$ and $T=1/(2.45\,\text{GHz})$. It is observed that, when the input power is smaller than 10 dBm, the numerical results agree very well with simulation results. When the input power takes larger values, the difference between them becomes larger, due to the voltage amplification factor whose value change with different physical circuits and varied input powers.

Table 1. Comparison of numerical and simulation results.

Pin (dBm)	V_A (V)	Numerical Results (V)	Simulation Results (V)
7	0.737	0.7009	0.766
8	0.831	0.8726	0.836
9	0.935	1.0651	1.020
10	1.051	1.2822	1.171
11	1.179	1.5240	1.342
12	1.322	1.7962	1.534

3. RF-DC Conversion Efficiency of Composite Rectifying Circuits

To improve the DC output, in this section three composite rectenna arrays are formed by series, parallel and cascade combinations, respectively. Simulation and experimental results show that the outputs of composite rectennas are significantly promoted, compared with the single dual-diode rectenna previously discussed.

For ease of subsequent comparison, the output current and voltage of the basic dual-diode rectifier shown in **Fig. 2** are firstly given. Specifically, if the load is R_L, the output current and voltage, are easily expressed as

$$I = \frac{V_0}{R + R_L}, \tag{18}$$

$$V = \frac{V_0 R_L}{R + R_L}, \tag{19}$$

where V_0 and R are the equivalent voltage and resistance of rectifying circuit, respectively. When the rectifier achieves its maximum RF-DC conversion efficiency, R must be equal to R_L. Next, the output current and voltage of three composite rectennas are examined, starting with the series combination.

3.1 Series Combination

Figs. 5-6 illustrate the model of series dual-diode rectenna combination and its equivalent linear circuit, respectively.

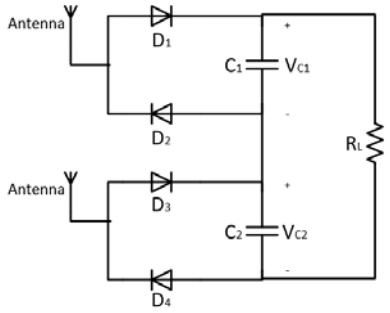

Fig. 5. The series combination of two rectennas.

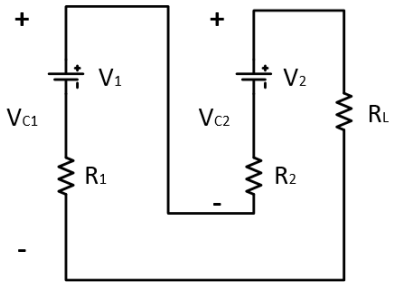

Fig. 6. The equivalent linear circuit of two serially combined rectennas [4]

Throughout this paper, it is assumed that two component dual-diode rectennas used to construct a composite rectenna (c.f. **Fig. 5**) are identical. With such an assumption, it is clear that $V_1 = V_2$ and $R_1 = R_2$. To maximize the output current, we must set $R_L = R_1 + R_2$ and, thus, (20) - (21) can be rewritten as

$$I_S = \frac{1}{2}(I_1 + I_2) = I_1, \tag{22}$$

$$V_S = V_{C1} + V_{C2} = 2V_C. \tag{23}$$

3.2 Parallel Combination

Figs. 7-8 illustrate the model of parallel dual-diode recetenna combination and its equivalent linear circuit, respectively. By using a similar approach as above, the output current and voltage dropped on the load can be expressed as

$$I_P = \frac{V_1 + V_2}{2R_L} = I_1 + I_2 = 2I_1 \,, \tag{24}$$

$$V_P = \frac{1}{2}\left(V_{C1} + V_{C2}\right) = V_C \,, \tag{25}$$

respectively, where $R_L = R_1 = R_2$ was set to attain the maximum RF-DC conversion efficiency.

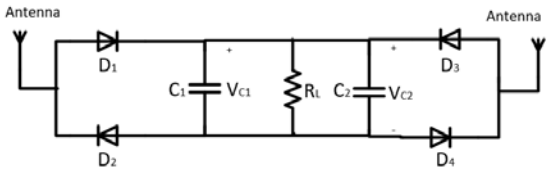

Fig. 7. The parallel combination of two dual-diode rectennas.

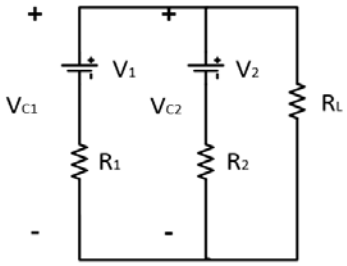

Fig. 8. The equivalent linear circuit of two rectennas combined in parallel.

3.3 Cascade Combination

Figs. 9-10 illustrate the model of cascade dual-diode recetenna combination and its equivalent linear circuit, respectively. Comparing **Fig. 9** with **Figs. 5** and **7** finds that the major difference between the cascade and series or parallel combination lies in that the output of the first stage serves as the source of the next stage. In this regards, the lower band pass filter (BPF) explicitly shown in **Fig. 9** benefits preventing DC rectified by the upper stage flowing through the lower antenna. On the other hand, the low pass filter (LPF) in **Fig. 9** is to ensure one-way transmission of the rectified energy. This LPF prevents the RF energy harvested by the lower antenna leaking to the upper stage without affecting DC produced by the upper stage. In practice, a non-ideal LPF with proper cutoff frequency benefits improving the rectifying efficiency by passing through a few residual harmonic components from the first stage to second stage. Those harmonic ones could be rectified again, thereby improving the DC output.

In theory, the cascade rectenna can be viewed as a composite series/parallel circuit [4]. In light of **Fig. 10**, the output current and voltage dropped on the load can be expressed as

$$I_C = I_{dc2} + I_{hc} \,, \tag{26}$$

$$V_C = V_{C2} = I_C \times R_L \,, \tag{27}$$

where I_{dc2} denotes the DC produced by the second stage and I_{hc} refers to the harmonic components flowing towards the second stage due to the non-ideal characteristic of the LPF. In particular, it is straightforward that $I_{dc1} = I_{dc2}$ in ideal cases, namely, two identical rectennas are employed (cf. **Fig. 9**).

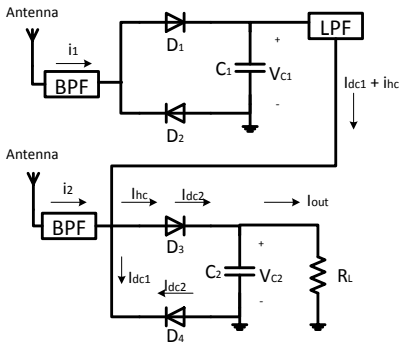

Fig. 9. The cascade combination of two dual-diode rectennas.

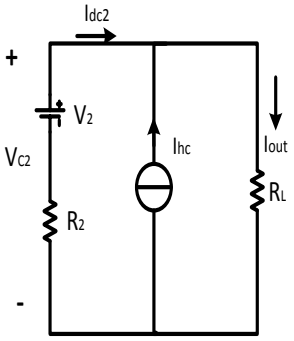

Fig. 10. The equivalent linear circuit of two rectennas combined in cascade.

It is remarkable that, in **Fig. 9**, the DC produced by the first-stage has no contribution to the final output since it will flow towards the ground via D_4. This observation is verified in subsequent physical experiments by using a current detection probe.

3.4 Simulation Results

To verify the relationship shown in (22)-(27), three composite rectennas mentioned above are extensively simulated in ADS. In simulation setting, the parameters pertaining to RF source, dielectric substrate, Schottky diode, and storage capacity are identical to those listed in Section 2.3. The optimal loads of series, parallel and cascade rectenna are 400 Ω, 150 Ω and 250 Ω, respectively.

Figs. 11-13 shows the rectifying efficiency, output voltage and current versus the input power P_{in} in the unit of dBm, respectively. It is observed from **Fig. 11** that, for the series combination, the maximum RF-DC conversion efficiency is 57% in the case of the input power being 15.8 dBm. Meanwhile, **Figs. 12-13** show that the output voltage and current are 4.163 V and 10 mA, respectively.

On the other hand, for the parallel combination, it is observed from **Fig. 11** that the maximum conversion efficiency is 61.6% given that the input power is 16.1 dBm. Accordingly, the optimal output voltage and current are 2.24 V and 22 mA, respectively (cf. **Figs. 12-13**).

As for the cascade rectenna, **Fig. 11** shows that its rectifying efficiency performs the same as the other two in the low input power region, and the maximum conversion efficiency reaches 62.3% in the case of the input power being 15.4 dBm. Meanwhile, the DC output voltage and current are 3.287 V and 13 mA, respectively (cf. **Figs. 12-13**).

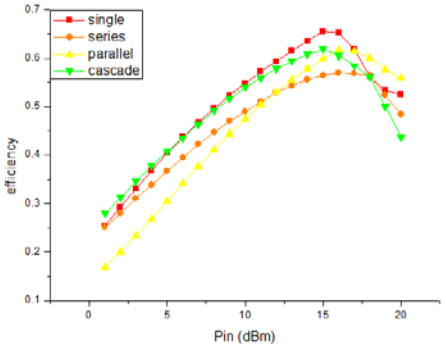

Fig. 11. Rectifying efficiency by simulation.

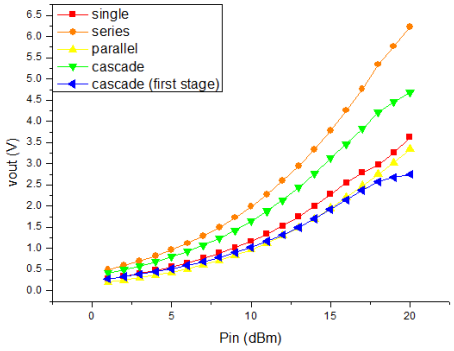

Fig. 12. Output voltage by simulation.

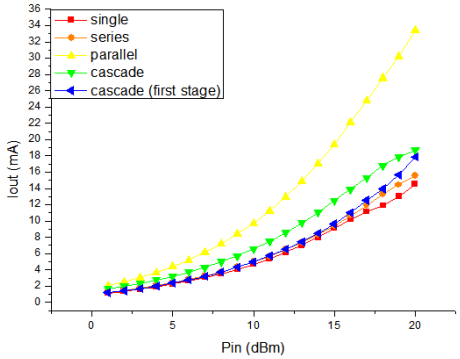

Fig. 13. Output current by simulation.

The blue curves shown in **Fig. 12** and **Fig. 13** represent the output voltage and current produced by the first-stage in a two-stage cascade rectenna. When the rectifying efficiency reaches the maximum, i.e., the input power is about 15.4 dBm, our simulation results show that the DC output current produced by the first-stage is 10 mA while the output at the second stage is 13 mA, this additional 3 mA is due to harmonic components at the first stage, which corroborates the preceding analysis in Section 3.3.

3.5 Experimental Results

Apart from the preceding simulation results in ADS, to further verify the performance analysis of the developed rectennas, their PCBs are produced (as shown in **Figs. 14-17**) and extensive experimental tests are carried out.

Figs. 18-20 show the experimental results pertaining to the rectifying efficiency, DC output voltage and current versus the input power P_{in} in the unit of dBm, which are coincident with the simulation results shown in **Figs. 11-13**, respectively. In particular, the maximum rectifying efficiencies obtained in experimental tests are a bit larger than their respective simulation results. For instance, for the basic dual-diode rectenna, the maximum experimental rectifying efficiency is 73.92% in the case of the input power being 18 dBm (cf. **Fig. 19**) whereas it is 56.1% by simulation (cf. **Fig. 11**). This is because the real-world PCB is optimized using a thin cover of copper foil. At the same time, the experimental output voltage and current of the basic dual-diode rectenna are 2.221 V and 21 mA, respectively (cf. **Figs. 19-20**).

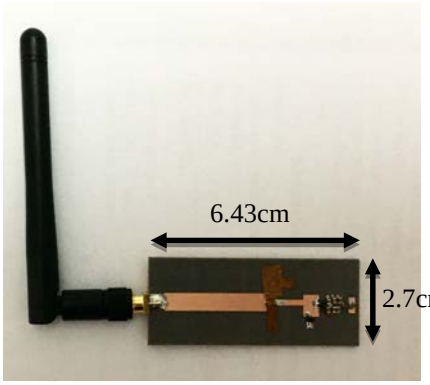

Fig. 14. PCB of single rectenna.

Fig. 15. PCB of serial rectenna.

Fig. 16. PCB of parallel rectenna.

Fig. 17. PCB of cascade rectenna.

For the series rectenna, **Fig. 18** shows that its maximum rectifying efficiency is 76.7% in the case of the input power being 18 dBm. At the same time, the output voltage and current are 4.27 V and 23 mA, respectively (cf. **Figs. 19-20**). Clearly, this DC output voltage is almost twice of the basic dual-diode rectenna.

For the parallel rectenna, the maximum rectifying efficiency is 78% given that the input power is 19 dBm. Accordingly, the optimal DC output voltage and current are 2.58 V and 48 mA, respectively (cf. **Figs. 19-20**). Clearly, its DC output current is almost twice of the single one.

As far as the cascade rectenna is concerned, its maximum rectifying efficiency is 79.2% in the case of the input power being 17.2 dBm (cf. **Fig. 18)**, which is 3.2% higher than that reported in [4]. Meanwhile, the DC output voltage and current are 2.771 V and 30 mA, respectively (cf. **Figs. 19-20**). Therefore, it is obvious that the cascade rectenna outperforms the others in terms of the maximum rectifying efficiency.

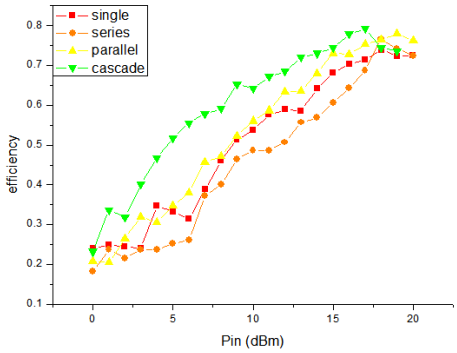

Fig. 18. Rectifying efficiency by experiment.

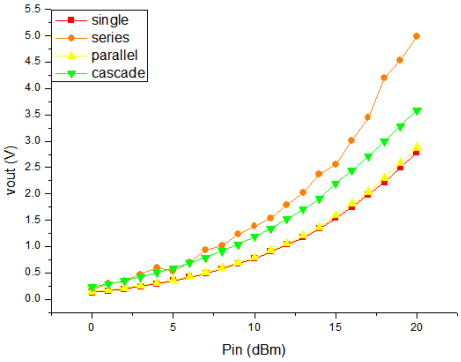

Fig. 19. DC output voltage by experiment.

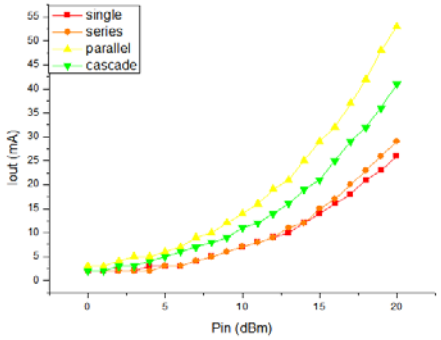

Fig. 20. DC output current by experiment.

4. Conclusion

In this paper, the rectifying efficiency of composite multi-antenna rectennas applicable to wireless power transfer was analytically studied. To start with, the output voltage and current of a basic dual-diode rectifier was firstly analyzed using the small signal model of diode. Then, a dual-diode rectenna operating at 2.45 GHz was developed. To further boost the output current and/or voltage without degrading the rectifying efficiency, three composite rectennas were developed, by using series, parallel and cascaded combinations of two dual-diode rectifiers, our simulation and experimental results show that the series rectenna has the highest output voltage, the parallel rectenna gets the highest output current, while the cascade rectenna obtains the highest rectifying efficiency. These rectennas find extensive applications in wireless power transfer and/or energy harvesting terminals of low-power consumption, such as sensors and RFID tags.

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