J Electr Eng Technol.2017; 12(6): 2278-2288
http://doi.org/10.5370/JEET.2017.12.6.2278

ISSN(Print) 1975-0102
ISSN(Online) 2093-7423

A Fault Diagnosis Method in Cascaded H-bridge Multilevel Inverter Using Output Current Analysis

June-Hee Lee*, June-Seok Lee and Kyo-Beum Lee†**

Abstract – Multilevel converter topologies are widely used in many applications. The cascaded H-bridge multilevel inverter (CHBMI), which is one of many multilevel converter topologies, has been introduced as a useful topology in high and medium power. However, it has a drawback to require a lot of switches. Therefore, the reliability of CHBMI is important factor for analyzing the performance. This paper presents a simple switch fault diagnosis method for single-phase CHBMI. There are two types of switch faults: open-fault and short-fault. In the open-fault, the body diode of faulty switch provides a freewheeling current path. However, when the short-fault occurs, the distortion of output current is different from that of the open-fault because it has an unavailable freewheeling current flow path due to a disconnection of fuse. The fault diagnosis method is based on the zero current time analysis according to zero-voltage switching states. Using the proposed method, it is possible to detect the location of faulty switch accurately. The PSIM simulation and experimental results show the effectiveness of proposed switch fault diagnosis method.

Keywords: Multilevel converter, Cascaded H-bridge multilevel inverter (CHBMI), Open-circuit switch fault, Short-circuit switch fault, Fault diagnosis, Reliability

1. Introduction

Large electric drives and utility applications require advanced power electronics converter to meet the high power demands. Multilevel power converter structure has been researched as an alternative in high power and medium voltage level [1-3]. The multilevel inverter topologies have been proposed such as diode clamped multilevel inverter, capacitor clamped inverter, cascaded H-bridge multilevel inverter [4-6]. The main concept of diode clamped multilevel inverter is to use diodes and provides the multiple voltage levels through the different phases to the capacitor which are in series. A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices. The maximum output voltage is half of the input DC voltage. It is the main drawback of the diode clamped multilevel inverter [7]. The main concept of capacitor clamped inverter is to use capacitors. The capacitors transfer the limited amount of voltage to electrical devices. The output is half of the input DC voltage. It is drawback of the capacitor clamped multilevel inverter. It also has the switching redundancy within phase to balance the capacitors [8]. The cascaded H-bridge multilevel inverter (CHBMI) has several advantages that have made it attractive in medium to high-power applications. The first one is its modularity. Each DC source is fed into an individual H-bridge inverter so it is easy to plug into more separate DC sources without changing the dimension of the system. Moreover, the output voltage waveform is nearly sinusoidal which decrease the cost of the passive filters [9-11]. The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations [12, 13]. Both modulation schemes can be applied to the CHBMI.

Recently, much research have conducted on CHBMI systems such as development of pulse width modulation (PWM), switch fault diagnosis method and reduction of output current harmonic distortions [14-16]. Among these research topics, switch fault diagnosis is a major one, because it reflects the reliability of power electronic systems.

The fault of switching device can be classified as a short-circuit switch fault and an open-circuit switch fault. The open-circuit switch fault, usually called the open-fault, can occur due to the several reasons such as a damaged inner wire, a momentary short circuit and gate driver fault. It causes a change in the current shape and can generate secondary problems that cause other parts to break down [17]. The short-circuit switch fault, usually called the short-fault, can occur due to the several reasons such as overvoltage, overcurrent, breakdown of the protection components and wrong gate signal [18]. The short-circuit switch fault is difficult to handle because an abnormal overcurrent which can cause serious damage to other parts is produced immediately if the short-circuit switch fault

† Corresponding Author: Dept. of Electrical and Electronic Engineering, Ajou University, Korea. (kyl@ajou.ac.kr)
* Dept. of Electrical and Electronic Engineering, Ajou University, Korea. (ljh20609@ajou.ac.kr)
** Railroad Safety Research Division, Korea Railroad Research Institute, Uiwang, Korea. (ljs@krri.re.kr)
Received: December 28, 2016; Accepted: September 14, 2017

occurs. Therefore, most methods for short-circuit switch fault diagnosis and tolerant control are based on hardware circuits [19, 20]. Generally, the body diode of IGBT module can be used in open-fault occurs because the switch is more weakness than the body diode. Hence, the body diode of fault switch can provide a freewheeling current path. However, when breakdown of the protection component for the CHBMI, such as a fuse, is occurred by the short-circuit fault, the current does not flow through the body diode of fault switch because the disconnection of fuse. Hence, the output current distortion of short circuit switch open fault is different from that of the general open-circuit switch fault and the detection of both faults is necessary to prevent the destruction of other devices and to improve the reliability of systems.

The short-fault usually lead to overcurrent protection and shut down the whole systems, and open-fault will not generate over current, but it will induce noise and vibrations of the systems. It will cause secondary problems of system or the load. Therefore, it is necessary to detect the faulty switch and identify the device in which the fault has occurred to reduce the cost of repairs and to improve reliability of the systems [9-11, 14] and [15]. To detect both the open-fault and short-fault, several researchers introduced fault diagnosis method for the CHBMI [21-23]. In [21], the microcontroller (MCU) uses the fault signal from the switch gate drivers. In this case, since the switch gate driver must operate sensitively, it must consist of the expensive components. In [22], by comparing the output reference voltage with the output voltage, the fault diagnosis method is implemented. However, this method requires additional voltage sensors. In [23], the method bypasses the faulty converter by using the additional components and changes the modulation method which does not use the faulty cell. It requires additional components such as IGBTs, fuses, diodes, etc.

In the multilevel power converter topologies with many power switches, the fault of one or more power switches can occur due to the abnormal signal of the gate driver, the surge currents, the electro-magnetic interference (EMI), and so on [24-26]. In order to diagnose the fault of many power switches, fundamentally, it is necessary to diagnose the location of faulty switch in the only one switch fault. This paper assumes that the only one switch has open- or short-fault. For example, if the power supply of the gate driver isolated from other power supply has the noise signal, it is possible to be damaged the gate driver. In this case, the open-fault occurs in one switch. Moreover, if the switch ON state is longer due to the malfunction of the gate driver, it is possible to breakdown the protection component because the surge current instantaneously flows through the protection component and power switch. In this case, the short-fault occurs in one switch. Therefore, this paper has validated the proposed method for these situations.

This paper presents a fault diagnosis method for both open-fault and short-fault in the CHBMI using rotating level-shifted PWM (RLS-PWM). There are some assumptions about the proposed fault diagnosis method as follows:

1) The topology is a seven-level single-phase cascaded H-bridge multilevel inverter.

2) The output current has configured on unity power factor.

3) The short-fault can be described by disconnecting the fuse.

4) The number of faulty switch is only one.

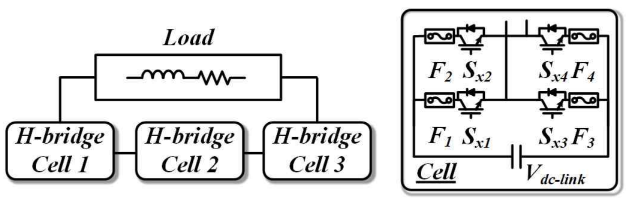
In this paper, the short-fault represents the breakdown of the protection component and switch a short-circuit. Hence, the anti-parallel diode of the faulty switch becomes unavailable. The proposed method uses the RLS-PWM and the zero-switching sequence method to distribute the power and detect the location of both the faulty cell and switch. The proposed method has been verified through PSIM simulation and experimental results.

2. Description of Cascaded H-bridge Multilevel Inverter

Fig. 1(a) shows a seven-level CHBMI composed of multiple units of H-bridge power cells connected in series to produce high voltages, while Fig. 1(b) shows the H-bridge inverter for each cell. Each cell consists of a DC-link capacitor and four switches. In general, many industrial fields avoid the damage of short-circuit by adding protection circuits or components to the power conversion systems. In particular, a system, that uses many switches, such as the CHBMI, certainly requires protection circuits or components, due to issues of reliability. When switches S_{x1} and S_{x4} are conducted, the output voltage of the H-bridge cell is the positive DC-link voltage (+E). Similarly, with S_{x2} and S_{x3} switch-ON, the output voltage is the negative DC-link voltage (-E). The phase voltage of the inverter is the summation of the two output voltages. For 0<MI<1, the output voltage has fundamental frequency of f and it is termed the reference voltage (V_{ref}). This is determined by:

$$V_{ref} = N \cdot V_{dc-link} \cdot MI \cdot \sin(\theta)\,. \tag{1}$$

where N refers to the number of cells. The seven-level



(a) (b)

Fig. 1. 7-level CHBMI with protection components

Table 1. Rotation sequence for the modulation index

# of Rotation sequence	Rotation sequence for Modulation index		
	0<*MI*<0.33	0.33<*MI*<0.66	0.66<*MI*< 1
0	Cell 1	Cell 2	Cell 3
1	Cell 2	Cell 3	Cell 1
2	Cell 3	Cell 1	Cell 2

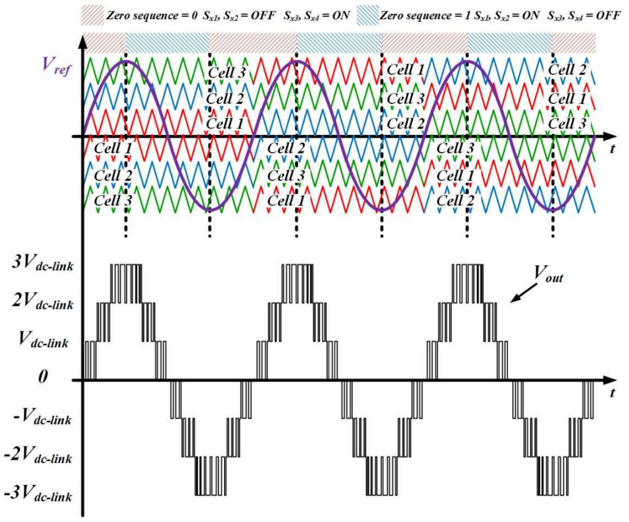


Fig. 2. Carriers of the RLS-PWM method and output voltage of 7-level CHBMI

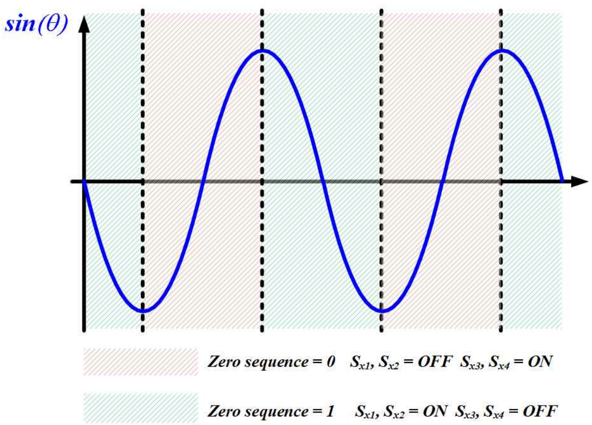


Fig. 3. Zero voltage switching state

CHBMI using a level-shifted multicarrier modulation scheme requires six-triangular carriers, all having the same amplitude and frequency. The six-triangular carriers are vertically disposed in bands. The level-shifted PWM can be generally classified into three types: in-phase disposition (IPD), alternative phase opposite disposition (APOD), and phase opposite disposition (POD). Among them, the CHBMI uses the IPD and the rotating PWM method. The rotating PWM method can balance the power distribution of each cell. Additionally, it is possible to easily detect the faulty switch using the RLS-PWM method. Fig. 2 shows the carriers of the RLS-PWM and the output voltage of the 7-level CHBMI. Table 1 shows the rotation sequence depending on the modulation index.

Table 2. Two types of zero-voltage switching states

S_{x1}	S_{x2}	S_{x3}	S_{x4}	V_H
OFF	OFF	ON	ON	0 V
ON	ON	OFF	OFF	0 V

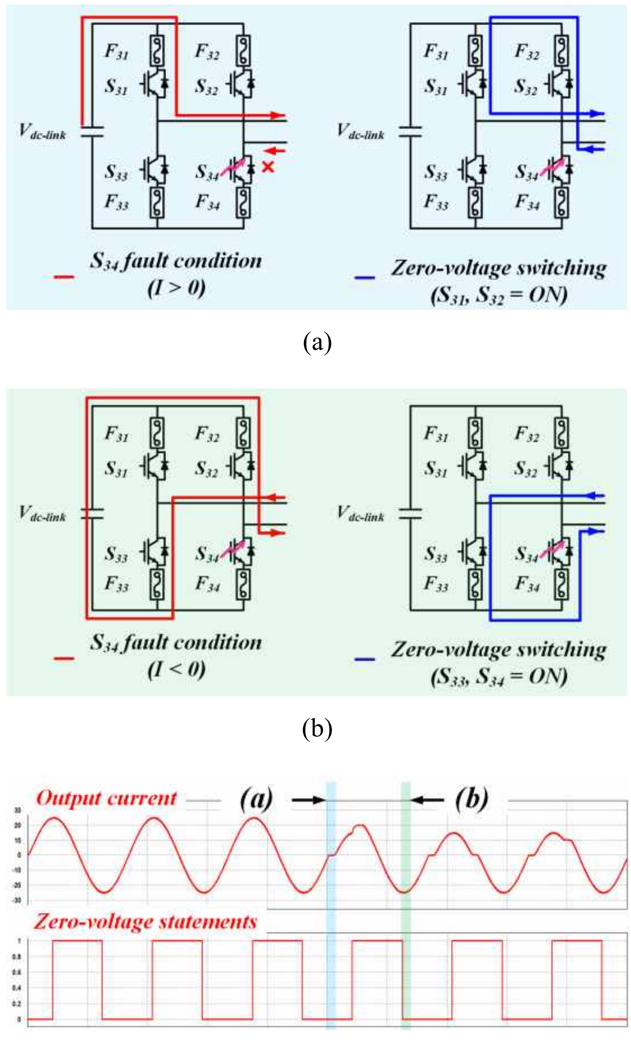


Fig. 4. Current flow path and output current waveforms in open-circuit switch fault

To accurately detect the location of the fault cell and switch, the zero-voltage switching state must be considered. Table 2 shows that the zero-voltage switching state can be determined as either of two types. When the phase voltage is $+E$, one cell is operated by the PWM for the reference voltage, and the other cells are operated by the zero-voltage switching state. Fig. 3 shows that if the zero-voltage switching state is exchanged for the peak value of the fundamental sinusoidal waveforms, it is possible to correctly detect the fault cell and switch.

3. Output Current Analysis for Two types of Switch Fault Situation

3.1 Open-circuit switch fault situation

Fig. 4(a) shows the examples of current flow path under the open-fault of S_{34} when the output current is positive. If the number of rotation sequence is 0, S_{31} and S_{32} are ON for the zero-voltage switching and S_{34} is a fault switch (*A block* in Fig. 4(c)), then the output current is to be zero because the power of *Cell 3* does not transfer to the load. Therefore, when the modulation index is low, output current distortion can occur.

Fig. 4(b) shows an example of when the output current is negative (*B block* in Fig. 4(c)). In this case, even though S_{34} is in the open-fault situation, it is possible to operate zero-voltage switching, because the anti-parallel diode of the open-fault switch can be used. Therefore, both types of zero-voltage switching can apply for the CHBMI. In addition, Fig. 4(c) shows the rotation sequence changes the location of the output current distortion.

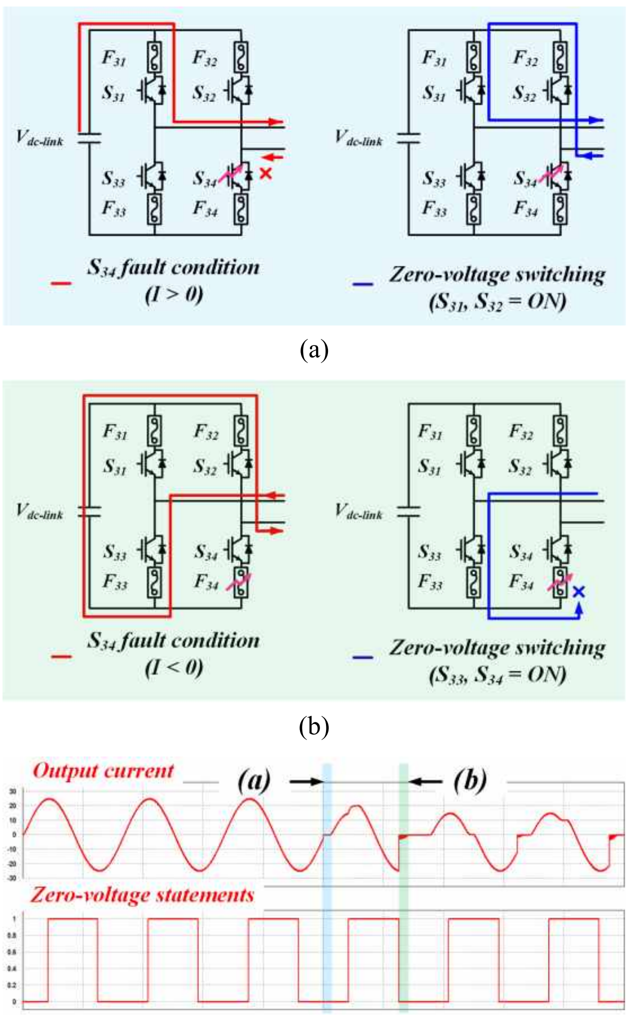


Fig. 5. Current flow path and output current waveforms in short-circuit switch fault

3.2 Short-circuit switch fault situation

Fig. 5 shows the current flow path, I_{out} and the zero-voltage switching statements in S_{34} short-fault. The short-fault can occur for many reasons: e.g., wrong gate signal or dead-time [18]. Compared with the open-circuit switch fault, the same location of output current distortion occurs by the rotation sequence and zero-voltage switching. However, if S_{x1} and S_{x3} are in a state of turn-on at the same time, the current flows through the DC-link capacitor, F_1, S_{x1}, S_{x3} and F_3. This is sufficient to breakdown the components. In the case of a short-circuit, a momentary surge current can cut the fuse. Because the anti-parallel diode of the switch can no longer be used, it cannot provide a freewheeling current path.

For example, if the number of rotation sequence is 0, S_{31} and S_{32} are ON for zero voltage switching and S_{34} is a fault switch (*B block* in Fig. 5(c)), then because the output current cannot flow through the freewheeling current path of anti-parallel diode, the output current is not precisely generated. The blue line in Fig. 5(b) shows the blue line is the current path without the anti-parallel diode of the faulty switch.

4. Proposed Fault Diagnosis Method for Two types of Switch Fault Situation

If the open- and short-circuit switch fault occurs, the switching state does not reach the desired state. This state causes a change in the output phase voltage and distortion of the output current. Therefore, the fault condition can be diagnosed through analysis of the output current [10]. As explained in the previous section, the type of switch fault is separated, whether it uses the freewheeling current path or not.

First of all, to detect the exact location of both the open-circuit switch fault and the short-circuit switch fault situations, the detection method must distinguish between those fault situations. Fig. 6 shows the waveforms of the output current, the tilt of output current and the angle of output current in the open-circuit switch fault situation, while Fig. 7 shows the same waveforms as Fig. 6 in the short-circuit switch fault situation. The fault condition is the same as in Section III. Fig. 6 and 4 show that when the tilt of output current is calculated nearby zero, T_{zero} starts increasing. In the open-circuit switch fault, the fault period is always fixed, because it is possible to use the freewheeling current path of the fault switch. Therefore, even if any switch has the fault, the tilt of the output current is zero during the fixed time. However, in the short-circuit fault shown in Fig. 7, the time that the tilt of output current is zero is longer than the open-circuit switch fault.

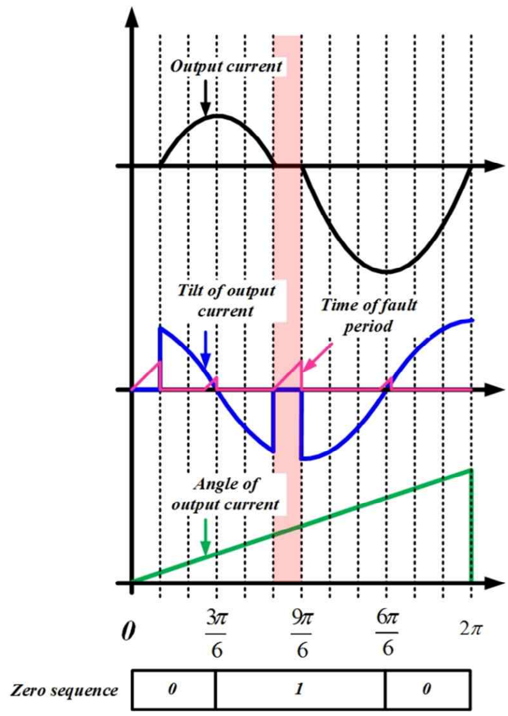


Fig. 6. Characteristics when the open-circuit switch fault

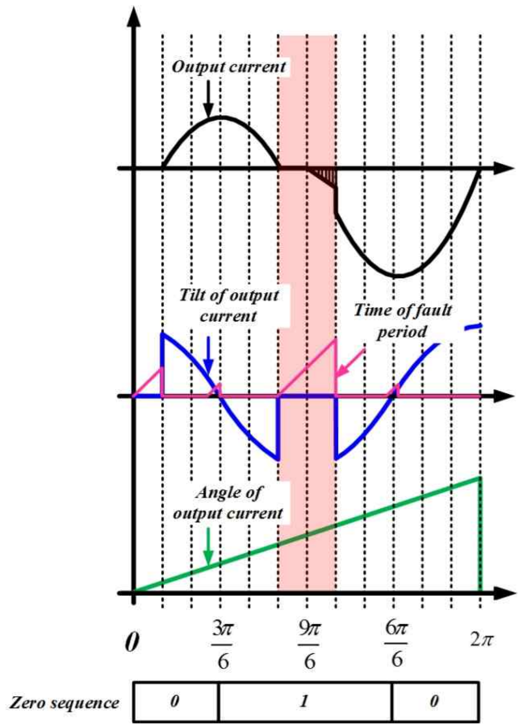
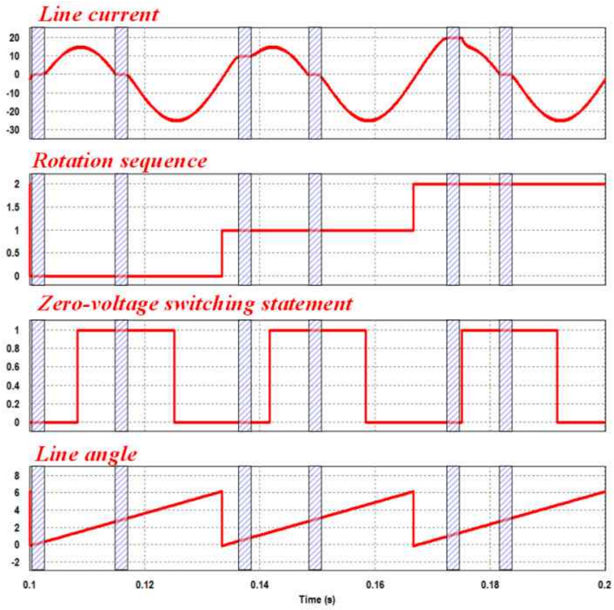


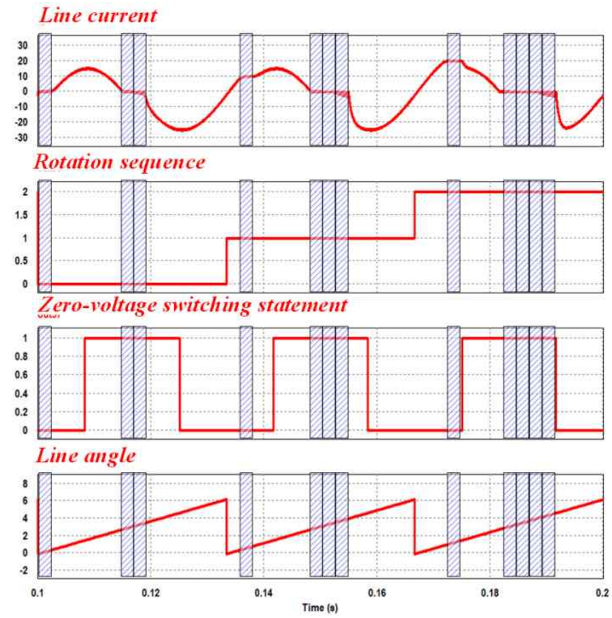
Fig. 7. Characteristics of the short-circuit switch fault

In addition, T_{zero} is related by the sampling time of the MCU. T_{zero} can be determined by:

$$T_{zero} < \frac{1}{2 \times (N_{level} - 1)} \times \frac{1}{f} \times \frac{1}{T_{samp}}. \tag{2}$$



(a)



(b)

Fig. 8. Detection method using the current analysis: (a) Open-fault; (b) Short-fault

where, N_{level} refers to the number of levels, f refers to the fundamental frequency and T_{samp} refers to the sampling time of the MCU.

After distinguishing the faulty type, the CHBMI diagnoses the location of faulty cell and faulty switch using the proposed detection method. In the proposed detection method, the location of the zero tilt period and the time of the zero period T_{zero} are used to detect the location of the faulty switch. Among the means of analysis of the output current, using the output current derivation (*tilt*) is suitable for the CHBMI. To exactly diagnose the location of faulty switch, the tilt of the output current from the current sensor compares with the tilt of the normalized output current calculated by the load conditions. The normalized tilt of the output current can be determined by:

$$I_{tilt,N} = \frac{(I_{out} - I_{out\_old})}{dt} \times \frac{1}{2\pi f \times |I_{out}|}. \quad (3)$$

The open- and short-circuit switch fault can be detected when the normalized tilt is smaller than the factor (C_{fault}) through the comparing the normalized tilt from Eq. (2) with the current tilt of the non-fault situation.

$$I_{tilt,N} < C_{fault} \cdot I_{tilt,N} \Rightarrow switch\ is\ fault. \quad (4)$$

Fig. 8 shows the proposed detection method using the current analysis in the open- and short-fault. As shown in Fig. 8, the angle location of distortion is correlated by the number of rotation sequence and zero-voltage switching statements. Using the angle location which is the zero-tilt of output current, it is possible to accurately detect the location of faulty switch. The proposed method can confirm the different location of output current distortion according to the fault types during the 3 times fundamental frequency shown in Fig. 8.

The proposed detection method can detect the exact location of both the open-fault switch and the short-fault switch, using the time of the fault period, and the angle location where the tilt of the output current is zero. Fig. 9 shows a block diagram of the proposed detection method.

5. Simulation Results

In this paper, the simulations are performed using the PSIM tool. The open-circuit switch fault situation can be simulated by a turn-off gate signal. However, the short-circuit fault situation cannot be simulated by a turn-off gate signal, because of the anti-parallel diode of the fault switch. Hence, Fig. 10 shows that the auxiliary switch connects to the collector side of the faulty switch. The magnitude of

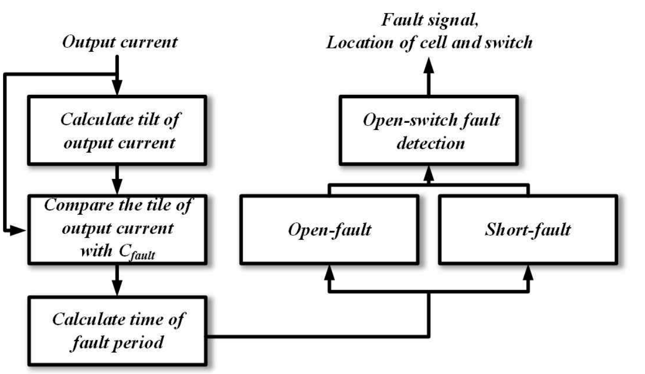


Fig. 9. Block diagram of proposed detection method

the $V_{DC\text{-}link}$ is 100 V, the capacitance of the DC-link is 2200 μF, the inductance of load is 5 mH, the load resistance is 10 Ω, the sampling frequency is 10 kHz and the modulation index is 0.833.

Fig. 11 shows the simulation results of the CHBMI. As explained in the previous section, the CHBMI is operated in RLS-PWM and zero-voltage switching to share the power consumption and detect the exact location of the open-fault switch. In comparison with LS-PWM, the output voltage of each cell has the fundamental frequency.

Fig. 12 shows the simulation results of the proposed switch fault detection method under the open-circuit switch fault in S_{11} of cell 1. Once the open-circuit switch fault occurs, it is evident that the current waveform has different shapes. When the open-fault occurs, the tilt of the output current rapidly decreases to zero. The proposed method still checks the time of fault period. The boundary between the open-fault and short-fault is 27.78 from Eq. (4). Hence, because the time of fault period is always smaller than T_{zero}, the fault signal is zero. In the non-fault state, the fault detection signal of each cell is set as zero. However, after 3

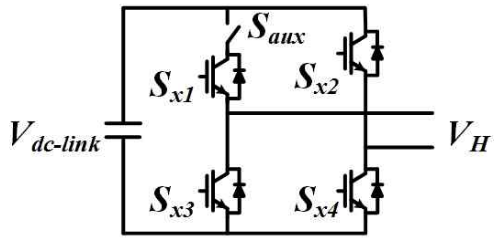


Fig. 10. H-bridge inverter cell for short-circuit open-fault detection

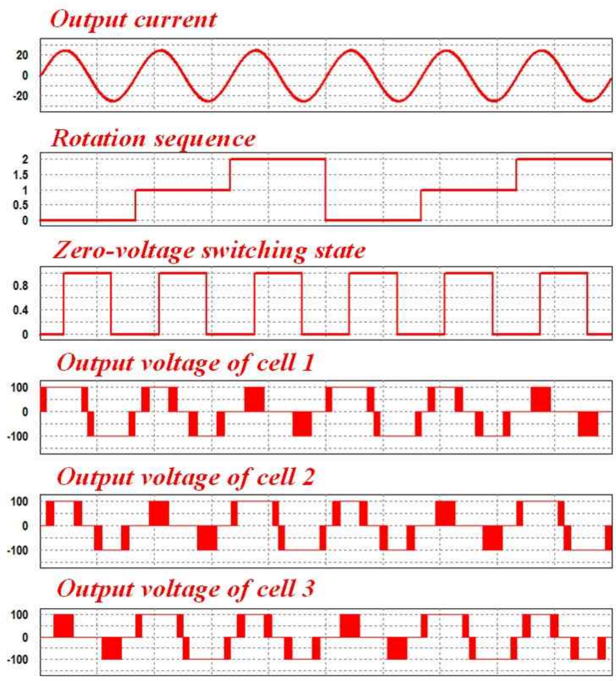


Fig. 11. Simulation results of CHBMI

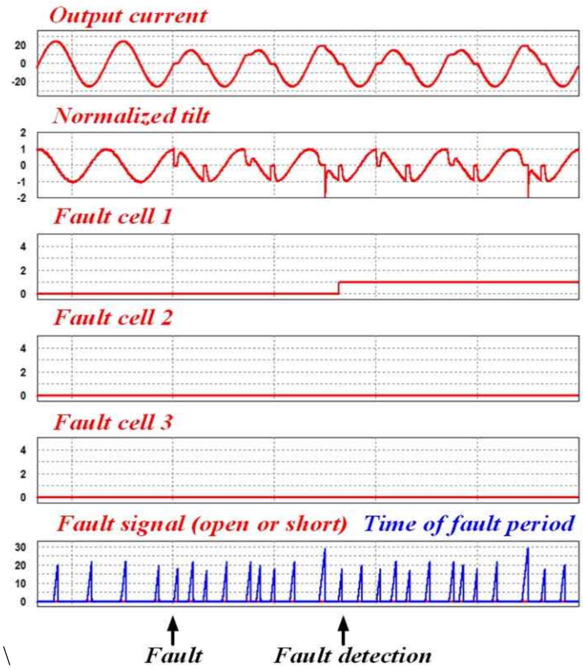


Fig. 12. Simulation results of the proposed detection method in open-circuit switch fault

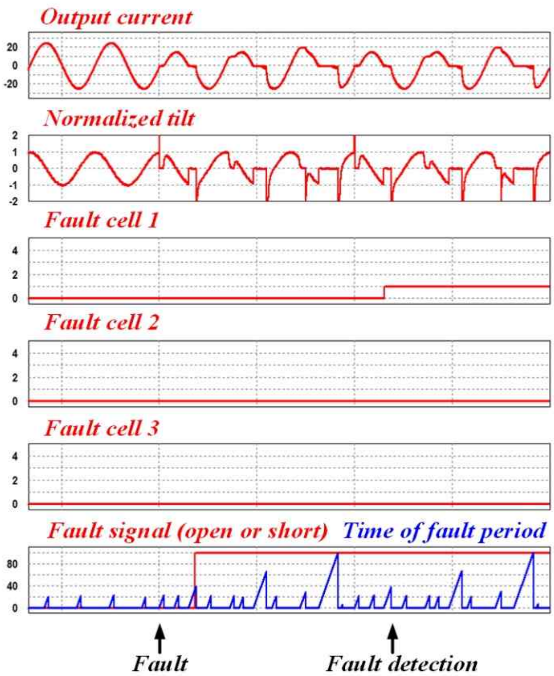


Fig. 13. Simulation results of the proposed detection method in short-circuit switch fault

times of the fundamental frequency, the CHBMI exactly detects the open-fault switch. In this case, flag of the fault cell 1, which is the third waveform of Fig. 12, becomes one. Therefore, When the open-switch fault occurs, it is possible to detect the location of both the cell, and the open-fault switch.

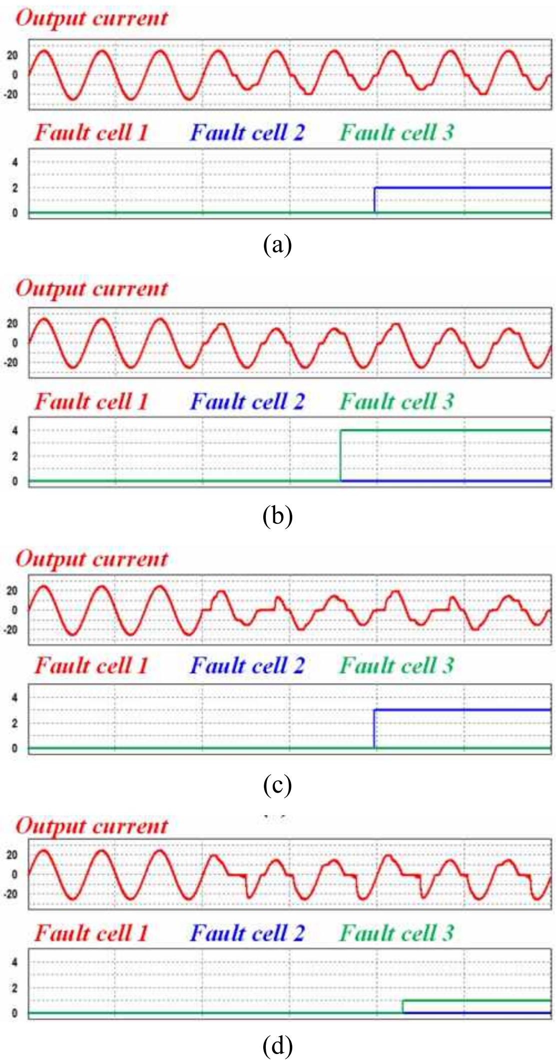


Fig. 14. Simulation results where several types of fault

Fig. 13 shows the simulation results of the proposed switch fault detection method under the short-circuit switch fault in S_{11} of cell 1. Once the open-switch fault occurs, it is evident that the current waveform has different shapes, compared with when the open-circuit switch fault occurs. Due to the unusable anti-parallel diode of the open-circuit fault switch, the freewheeling current does not flow to the load, which causes the longer time of the fault period. Hence, the fault signal is one, because the time of the fault period is always higher than T_{zero}. Then, after 3 times of the fundamental frequency as soon as the fault signal becomes one, the CHBMI exactly detects the open-fault switch. Therefore, it is possible to detect the location of both the cell and fault switch under the short-fault occurs.

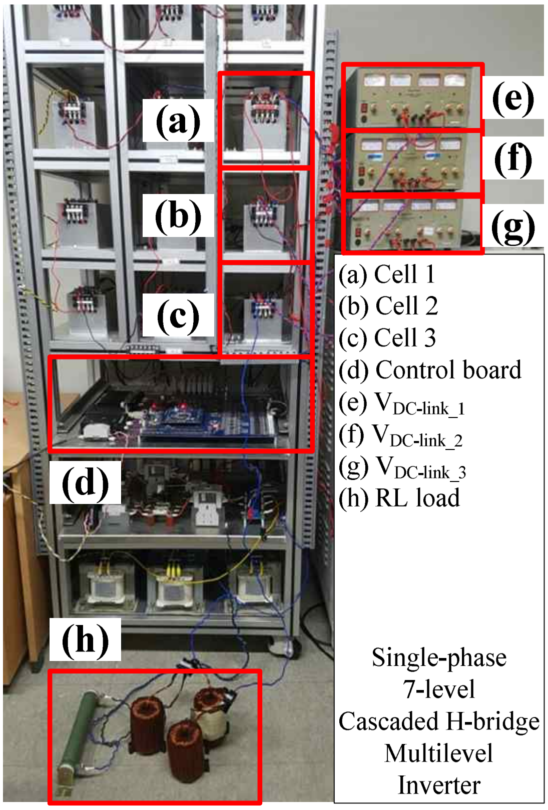
Fig. 14 shows the simulation results of the proposed detection method. Fig. 14(a) simulates when an open-fault occurs, and the faulty switch is S_{22}. Fig. 14(b) simulates when an open-fault occurs, and the faulty switch is S_{34}. Fig. 14(c) simulates when a short-fault occurs, and the faulty switch is S_{24}. Fig. 14(d) simulates when a short-fault occurs, and the faulty switch is S_{31}. In each case, the proposed detection method detects the precise location of both the open-fault switch, and the short-fault switch.

6. Experimental Results

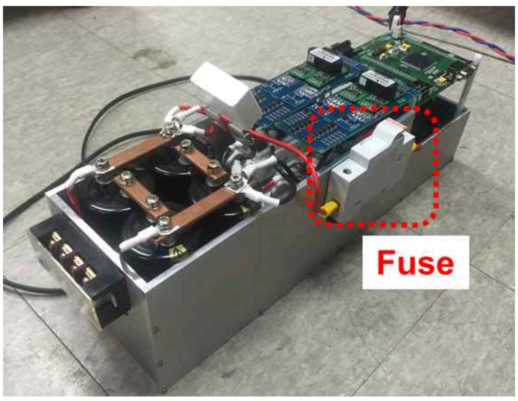
Fig. 15(a) shows the entire experimental set, while Fig. 15(b) shows each H-bridge cell experimental set. The main microcontroller unit (MCU) is TMS320C28346 for Texas Instruments (TI), as the FPGA is known, and each cell has the TMS320F28335 for the same reason. Table 3 shows the experimental parameters, while Table 4 shows the detection method parameters.

The open-circuit switch fault can be simulated by the gate signal of the faulty switch always operating in OFF-state by the MCU, while the short-circuit switch fault can be simulated by disconnecting the fuse.

Fig. 16 shows the experimental results of the proposed fault detection method under an open-fault in S_{14} of cell 1. If an open-circuit switch fault occurs in S_{14} of cell 1, it is evident that the output current waveform has distortions.



(a)



(b)

Fig. 15. Experimental set

Table 3. Experiment parameters

$C_{DC-link}$	2200 μF	$f_{switching}$	10 kHz
$V_{DC-link}$	50 V	T_{samp}	100 μs
L_{load}	6 mH	f_{line}	60 Hz
R_{load}	20 Ω	MI	0.833

Table 4. Detection method parameter

T_{zero}	22.78
C_{fault}	0.5

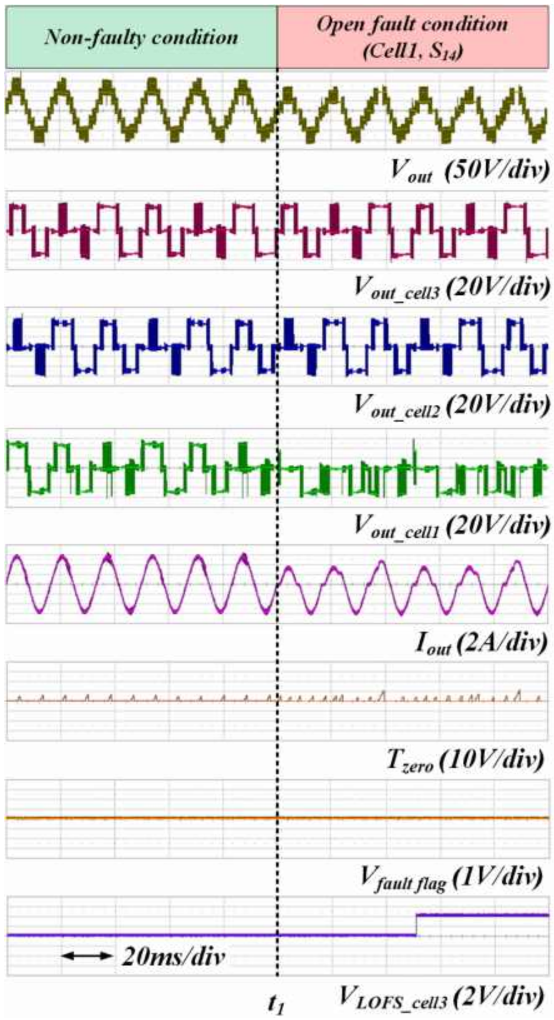


Fig. 16. Experimental results of the proposed fault detection method under an open-fault in S_{14} of cell 1

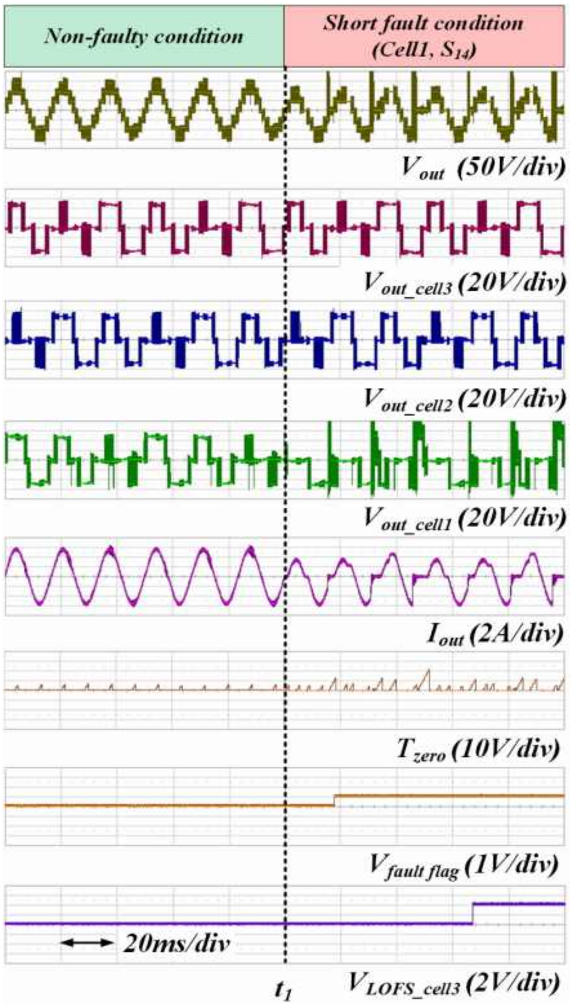


Fig. 17. Experimental results of the proposed fault detection method under an short-fault in S_{14} of cell 1

The proposed method still checks the time of the faulty period. Hence, the signal of distinguishing the fault types is still zero because the time of fault period is always smaller than T_{zero}. The tilt of the output current is compared with the normalized tilt. After three periods of the fundamental frequency, the detection method diagnoses the position of the faulty switch.

Fig. 17 shows the experimental results of the proposed fault detection method under the short-fault in S_{14} of cell 1.

If the open-circuit switch fault occurs in S_{14} of cell 1, it is evident that the output current distortion has different shapes compared with the open-fault. Owing to the unusable anti-parallel diode of the faulty switch, the freewheeling current does not flow to the load, and causes a longer time of the fault period. Hence, the signal of distinguishing fault types is one, because the time of the fault period is longer than T_{zero}. The tilt of the output current is compared with the normalized tilt. After 3-time fundamental frequency, the detection method diagnoses the position of the faulty switch.

7. Conclusion

This paper presents an improved method of detection of both an open-fault and a short-fault in CHBMI using analysis of the output current. The reliability of the CHBMI is an important factor for analyzing the performance. Using the proposed detection method, it is possible to detect a fault, and identify the location of the fault switch when the open-fault or short-fault occurs without any additional auxiliary circuits or devices. The simulation results and experimental results confirm the performance of the proposed fault detection method.

Acknowledgements

This work was supported by the Korea Institute of Energy Technology Evaluation and Planning(KETEP) and the Ministry of Trade, Industry & Energy(MOTIE) of the Republic of Korea (no. 20174030201660) and in part by the R&D Program of the Korea Railroad Research Institute, Republic of Korea.

References

[1] J. Rodriguez, J-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[2] M. A. Sayed, M. Ahmed, M. G. Elsheikh, and M. Orabi, "PWM control techniques for single-phase multilevel inverter based controlled DC cells," *J. Power Electron.*, vol. 16, no. 2, pp. 498-511, Mar. 2014.

[3] U.-M. Choi, H.-G. Jeong, K.-B. Lee, and F. Blaabjerg, "Method for detecting an open-switch fault in a grid-connected NPC inverter system," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2726-2739, June 2012.

[4] S. Kouro et al., "Recent advances and industrial application of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 58, pp. 2553-2580, Aug. 2010.

[5] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197-2206, Jul. 2010.

[6] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, W. Bin, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[7] M. Marchesoni and P. Tenca, "Diode-clamped multi-level converters: A practicable way to balance DC-

link voltages," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 752-765, Aug. 2002.
[8] S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of 4-kv neutral-point-clamped, flying-capacitor, and series-connected h-bridge multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1032-1040, Jul. 2007.
[9] K. Mylsamy, R. Vairamani, G. C. R. Irudayaraj, and H. T. R. Lawrence, "Experimental validation of a cascaded single phase H-bridge inverter with a simplified switching algorithm," *J. Power Electron.*, vol. 14, no. 3, pp. 507-518, May 2014.
[10] H.-W. Sim, J.-S. Lee, and K.-B. Lee, "Detecting open-wwitch faults: Using asymmetric Zero-voltage switching states," *IEEE Ind. Appl. Mag.*, vol. 22, no. 2, pp. 27-37, Mar-Apr. 2016.
[11] B. K. Kwon, S. K. Jung, and T. H. Kim, "Enhancement of cell voltage balancing control by zero sequence current injection in a cascaded H-bridge STATCOM," *The Transactions of the Korean Institute of Power Electronics*, vol. 20, no. 4, pp. 321-329, Aug. 2015.
[12] V. Singh, S. Pattnaik, S. Gupta, and B. Santosh, "A single-phase cell-based asymmetrical cascaded multilevel inverter," *J. Power Electron.*, vol. 16, no. 2, pp. 532-541, Mar. 2016.
[13] J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. Negroni, "Energybalance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 98-111, Jan. 2013.
[14] J.-S. Lee and K.-B. Lee, "An open-switch fault detection method and tolerance controls based on SVM in a grid-connected T-type rectifier with unity power factor," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 7092-7104, Dec. 2014.
[15] I. G. Kim and S. S. Kwak, "An algorithm for even distribution of loss, switching frequency, power of model predictive control based cascaded H-bridge multilevel converter," *The Transactions of the Korean Institute of Power Electronics*, vol. 20, no. 5, pp. 448-455, Oct. 2015.
[16] P. Lezana, J. Pou, T. A. Meynard, J. Rodriguez, S. Ceballos, and F. Richardeau, "Survey on fault operation on multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2207-2218, Jul. 2010.
[17] B. Mirafzal, "Survey of fault-tolerance techniques for three-phase voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5192-5202, Oct. 2014.
[18] X. Huang, G. Wang, Y. Li, A. Q. Huang, and B. Baliga, "Short-circuit capability of 1200V SiC MOSFET and JFET for fault protection," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2013, pp. 197-200.
[19] K. Ambusaidi, V. Pickert, and B. Zahawi, "New circuit topology for fault tolerant H-bridge dc-dc converter," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1509-1516, Jun. 2010.
[20] U.-M. Choi, K.-B. Lee, and F. Blaabjerg, "Diagnosis and tolerant strategy of an open-switch fault for t-type three-level inverter systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 495-508, Jan./Feb. 2014.
[21] M. Ma, L. Hu, A. Chen, and X. He, "Reconfiguration of carrier-based modulation strategy for fault tolerant multilevel inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 2050-2060, Sep. 2007.
[22] S. Ouni, J. Rodriguez, M. Shahbazi, M. Zolghadri, H. Oraee, P. Lezana, and A. U. Schmeisser, "A fast simple method to detect short circuit fault in cascaded H-bridge multilevel inverter," in *Proc. IEEE ICIT*, pp. 866-871, Mar. 2015.
[23] W. Song and A. Huang, "Fault-tolerant design and control strategy for cascaded h-bridge multilevel converter-based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2700-2708, Aug. 2010.
[24] J.-S. Lee and K.-B. Lee, "Tolerance control for inner open-switch faults of a T-type three-level rectifier," *J. Power Electron.*, vol. 14, no. 6, pp. 1157-1165, Nov. 2014.
[25] V. Gomathy and S. Selvaperumal, "Fault detection and classification with optimization techniques for a three-phase single-inverter circuit," *J. Power Electron.*, vol. 16, no. 3, pp. 1097-1109, Jun. 2016.
[26] N. Q. T. Vo, H.-C. Choi, and C.-H. Lee, "Short-circuit protection for the series-connected switches in high voltage applications," *J. Power Electron.*, vol. 16, no. 4, pp. 1298-1305, Jul. 2016.

June-Hee Lee He received his B.S. degree in Electrical and Computer Engineering from Ajou University, Suwon, Korea, in 2013. He is currently working toward his Ph.D. degree in Electrical and Computer Engineering at Ajou University, Suwon, Korea. His research interests include power conversion and grid-connected systems.

June-Seok Lee He received the BS, MS, and PhD degrees in electrical and computer engineering from the Ajou University, Korea, in 2011, 2013, and 2015, respectively. He is currently working at Korea Railroad Research Institute. His research interests include grid-connected systems, multilevel inverter, and reliability.

Kyo-Beum Lee He received the B.S. and M.S. degrees in electrical and electronic engineering from the Ajou University, Suwon, Korea, in 1997 and 1999, respectively. He received the Ph.D. degree in electrical engineering from Korea University, Seoul, Korea, in 2003. From 2003 to 2006, he was with the Institute of Energy Technology, Aalborg University, Aalborg, Denmark. From 2006 to 2007, he was with the Division of Electronics and Information Engineering, Chonbuk National University, Jeonju, Korea. In 2007, he joined the Department of Electrical and Computer Engineering, Ajou University, Suwon, Korea. His research interests include electric machine drives, renewable power generations, and electric vehicle applications.

Dr. Lee is an Associated Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, *the Journal of Power Electronics*, and *Journal of Electrical Engineering and Technology*.