TRANSACTIONS ON ELECTRICAL AND ELECTRONIC MATERIALS
Vol. 18, No. 5, pp. 257-260, October 25, 2017

Regular Paper

pISSN: 1229-7607 eISSN: 2092-7592
DOI: https://doi.org/10.4313/TEEM.2017.18.5.257
OAK Central: http://central.oak.go.kr

# Low Dropout Voltage Regulator Using 130 nm CMOS Technology

Mohammad Marufuzzaman, Mamun Bin Ibne Reaz, Labonnah Farzana Rahman†, Norhaida Binti Mustafa, and Araf Farayez
*Department of Electrical, Electronic and Systems Engineering, Faculty of Engineering and Built Environment, Universiti Kebangsaan Malaysia, 43600, UKM Bangi, Malaysia*

**Received November 9, 2016; Revised March 20, 2017; Accepted March 23, 2017**

In this paper, we present the design of a 4.5 V low dropout (LDO) voltage regulator implemented in the 130 nm CMOS process. The design uses a two-stage cascaded operational transconductance amplifier (OTA) as an error amplifier, with a body bias technique for reducing dropout voltages. PMOS is used as a pass transistor to ensure stable output voltages. The results show that the proposed LDO regulator has a dropout voltage of 32.06 mV when implemented in the130 nm CMOS process. The power dissipation is only 1.3593 mW and the proposed circuit operates under an input voltage of 5V with an active area of 703 $\mu m^2$, ensuring that the proposed circuit is suitable for low-power applications.

**Keywords :** LDO regulator, Operational transconductance amplifier, CMOS, Low power

## 1. INTRODUCTION

A linear voltage regulator is used to power an integrated circuit, which is inductor-less, ripple-less, and has a low-noise power converter with a bulk line frequency transformer [1]. There is an ever-increasing demand for portable, handheld batteries for use in smart phones, tablet PCs, cameras, MP3 players and PDAs. The use of efficient power management systems to prolong the battery life and operating time of a device, and which provide a reliable, stable and constant voltage, are becoming increasingly important [2–4]. Low dropout (LDO) voltage regulators can operate at a low supply voltage and can provide a nearly constant dc voltage. LDO regulators are thus suitable for single-cell and two-cell battery applications since the ground current is load-current independent. To regulate the performance (line and load regulation), the transient overshoot and undershoot are required. Furthermore, during design process the output current, quiescent current, input and output voltage, power and current efficiency, and transient settling time are considered as important parameters [2,5].

LDO regulators fall into a class of linear voltage regulators with improved power efficiency. Efficiency is improved over conventional linear regulators by replacing the common-drain pass element with a common-source pass element, which reduces the minimum required voltage drop across the control device [6]. The basic LDO voltage regulator topology usually consists of a voltage reference, an error amplifier, a pass device, an external load capacitor with a small value of internal resistance (ESR), and a feedback network.

Figure 1 shows the overall topology of a LDO voltage regulator. An error amplifier, in a negative feedback condition, detects an error signal when there is a difference between the feedback voltage and reference voltage. The error signal will control the gate of the pass transistor, which maintains constant output voltage, and will supply a variable current to the load circuit. An operational transconductance amplifier (OTA) is the best option as an error amplifier because the output is used to drive the gate of the pass transistor [7].

Several types of pass transistors have been proposed using NMOS and PMOS [8,9]. The NMOS as a pass transistor has a large dropout voltage. Hence, a PMOS pass transistor is the best choice due to its lower dropout voltage, quiescent current flow, output current and speed [8]. The pass device also influences loop gain, bandwidth, and stability. To drive the maximum load current and achieve low dropout performance, the pass transistor should have a large ratio of width and length. However, if the pass transistor is too large, the gate

† Author to whom all correspondence should be addressed:
E-mail: : khong@gmail.com

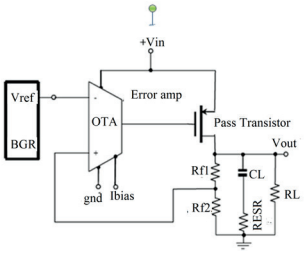


Fig. 1. Basic topology of a low dropout voltage regulator [7].

capacitance will increase, causing instability in the system [9]. The voltage reference provides the nominal output voltage. In Fig. 1, $R_{f1}$ and $R_{f2}$ are the resistors, which set the output voltage $V_{out}$.

In this paper, a two-stage OTA, as the error amplifier, with body bias technique has been proposed for the130nm CMOS technology in a Mentor Graphics environment. The body bias technique will be applied only to a transistor in the error amplifier. While designing the LDO regulator, and to improve its performance, the optimized output voltage $V_{out}$ is 4.5 V, and the dropout voltage is reduced.

## 2. METHODOLOGY

In this paper, a two-stage cascaded OTA as an error amplifier is developed. A PMOS pass transistor and body bias voltage are used to improve the dropout voltage of the LDO voltage regulator. The drop out voltage is the minimum differential voltage between the output and the input voltage at the point where the circuit stops to regulate. It also defined as the minimum voltage drop across the pass device to maintain regulation. The dropout voltage is typically specified at the maximum load current. The maximum load current specifications determine the size of the pass device, dropout voltage, and power dissipation constraints. When the specified maximum load current increases; the overall die area of the pass device, the control circuitry and the ground pin current, must also increase in order to drive the additional parasitic capacitances for the increased device size.

Figure 2 shows the proposed two-stage OTA using the body-driven technique in 130 nm CMOS technology. In the proposed design, the voltage body bias is applied to a p-channel transistor $m_{13}$, with 0.4 V to reduce the dropout voltage in the LDO regulator. It is operated at only at a positive voltage and the reference point $V_{ss}$, is changed by using the ground. A PMOS was used in this paper as the pass transistor, to increase the stability performance of LDO. In the proposed design; ($m_4$, $m_5$) and ($m_{13}$, $m_{12}$); ($m_3$, $m_6$) and ($m_{11}$, $m_{14}$); and, ($m_{15}$, $m_{16}$) and ($m_7$, $m_8$), form the cascaded pairs with current

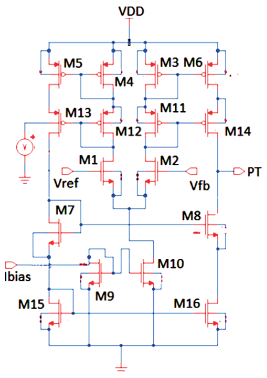


Fig. 2. Proposed two stage OTA with body driven technique.

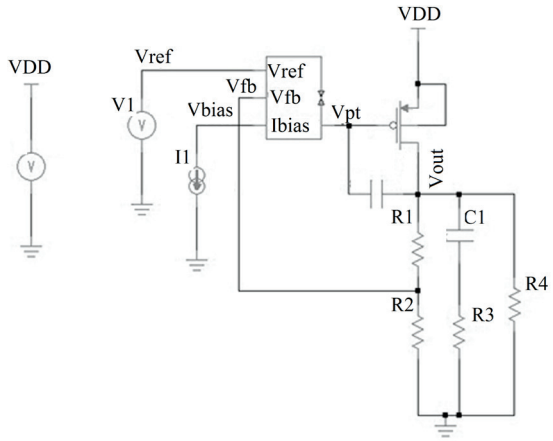


Fig. 3. Proposed LDO regulator.

Table 1. The output sequence of LFSR.

| Component | *Value* |
|---|---|
| $R_{f1}$ | 14.8 kΩ |
| $R_{f2}$ | 2.5 kΩ |
| $R_{ESR}$ | 0.05 Ω |
| $C_L$ | 400 pF |
| $C_1$ | 40 pF |
| $R_L$ | 1 MΩ |

Table 2. Output sequence of the LFSR.

| Component | *Value* |
|---|---|
| $R_{f1}$ | 14.8 kΩ |
| $R_{f2}$ | 2.5 kΩ |
| $R_{ESR}$ | 0.05 Ω |
| $C_L$ | 400 pF |
| $C_1$ | 40 pF |
| $R_L$ | 1 MΩ |

mirroring. The main design criterion of the proposed OTA is same as the classical OTA designs.

Figure 3 shows a schematic of the test bench. The optimized values for obtaining $V_{out}$ = 4.5 V are listed in Table 1, which also shows the output sequence generated by a 4-bit linear feedback shift register (LFSR) with a seed value of [1 1 1 1]. This is related to the Fibonacci function assuming an external or simple type of LFSR (SLFSR) [19].

In this paper, $R_{ESR}$ is set to 0.05 Ω. According to Kayal et al.(2006), the optimum range of $R_{ESR}$ is 0.05–10 Ω [10] because if $R_{ESR}$ is too large, the overshoot will increase drastically. The dimensions of the transistors in the proposed LDO regulator are listed in Table 2.

## 3. RESULTS AND DISCUSSION

The circuit is designed using the Design Architect of Mentor Graphics EDA tool in 130 nm CMOS technology and the simulation is performed using the ELDO software of "Silterra 130 nm Kit." After completing the schematic design, a testbench is created to test and verify the design output. A constant output voltage can be achieved by controlling the load current flow through the pass device. By choosing the appropriate value of the resistor and reference voltage, the output voltage can be set to

$$V_0 = V_{ref} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

According to Equation 1, to obtain a value of $V_{out}$ = 4.5 V, $R_{f1}$ = 14.8 kΩ, and $R_{f2}$ = 2.5 kΩ have been selected. The (Miller) capacitor $C_1$is set to 40 pF, and is attached to two high impedance points in the circuit, ensuring a good phase margin in the design. The load capacitance $C_L$ is set to 0.4 nF. The values for the voltage and current bias used in the simulation are listed in Table 3.

The two-stage OTA using the body bias technique, shown in Fig. 2, was designed using the transistor parameter values in Table 2. A body bias technique of 0.4 V was applied to transistor $m_{13}$ in the two-stage OTA. This LDO regulator was simulated in a test bench, shown in Fig. 3, with $V_{in}$ ranging from 3.3 V to 5.2 V. The designed circuit satisfied the specifications of Table 3. Figure 4 shows the waveform results for $V_{out}$, $V_{PT}$, and $I_{load}$ at the pass transistor; and Fig. 5 shows the settling time of the proposed LDO circuit.

The two-stage OTA using the body bias technique, shown in Fig. 2, was designed using the transistor parameter values in Table 2. A body bias technique of 0.4 V was applied to transistor $m_{13}$ in the two-stage OTA. This LDO regulator was simulated in a test bench, shown in Fig. 3, with $V_{in}$ ranging from 3.3 V to 5.2 V. The designed circuit satisfied the specifications of Table 3. Figure 4 shows the waveform results for $V_{out}$, $V_{PT}$, and $I_{load}$ at the pass transistor; and Fig. 5 shows the

Table 3. Design specification for the proposed LDO regulator.

| Parameter | *Value* |
|---|---|
| Variation output voltage ($\Delta V_{out}$) | 500 mV |
| Reference voltage ($V_{ref}$) | 650 mV |
| Bias current ($I_{bias}$) | 50 μA |

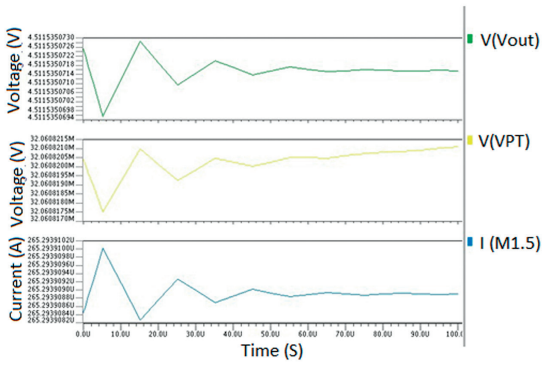


Fig. 4. Waveforms for $V_{out}$, $V_{PT}$, and $I_{load}$.

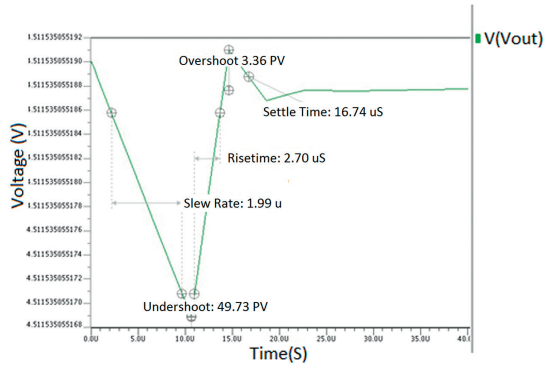


Fig. 5. Settling time for $V_{out}$ of the proposed circuit.

Table 4. Performance comparison of low dropout voltages for two-stage classical OTA.

| Research Works | $V_{out}$ / V | VPT / mV | $V_{fb}$ / mV | $P_{diss}$ / mV |
|---|---|---|---|---|
| Classical 2-Stage OTA | 4.5081 | 89.5785 | 651.4587 | 1.358 |
| 2-Stage OTA [7] | 4.5123 | 33.063 | 651.0729 | 1.3593 |
| This Research | 4.5115 | 32.06 | 651.9559 | 1.3593 |

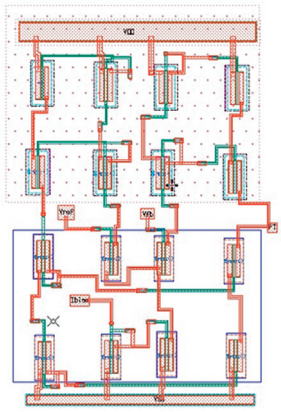

Fig. 6. Layout for the proposed two-stage OTA.

Table 5. LDO voltage regulator performance comparison.

| Performance | *2014 [2]* | *2014 [13]* | *2014 [12]* | *2013 [11]* | *2013 [7]* | *This work* |
|---|---|---|---|---|---|---|
| Technology (nm) | 180 | 180 | 180 | 180 | 350 | 130 |
| Supply voltage (V) | 1.8 | 1.8 | 1.45 | 1.8 | 5 | 5 |
| Output voltage (V) | 1.6 | 1.6 | 1.4 | 1.64 | 4.5 | 4.5 |
| Dropout voltage (mV) | 200 | 200 | 200 | 160 | 60 | 32.060 |

settling time of the proposed LDO circuit.

In Fig. 5, the settling time for the proposed circuit is 16.744 μs. This is faster than that of both the OTA circuit, 29.275 μs, proposed by Garcia [7], and the classical OTA, 89.243 μs, for analyses of 130 nm CMOS technology. Regarding stabilization, after 25 μs, $V_{out}$ is constant, whereas the results of Garcia [7] show that even after 25 μs the output voltage is still increasing. Simulations of the classical and two-stage OTA proposed by Garcia [7] were performed using 130 nm CMOS technology, and the comparisons of these techniques are summarized in Table 4. According to Table 4, it is can be seen that by using body bias technique 0.4 V at transistor $m_{13}$, the low drop out voltage in the proposed circuit is better. The drop out voltage difference is 1 mV between this research and the circuit designed by Garcia [7].

Figure 6 shows the layout of the proposed two-stage OTA. The total layout area for the proposed OTA is 16.75 × 42 μm$^2$, which is significantly smaller compared with previous work in this field. The performance comparisons of the LDO regulator, designed using various techniques, are shown in Table 5. Compared with other research, it is shown that the two-stage OTA in the LDO regulator, with body bias technique, provides the lowest dropout voltage of 32.060 mV.

## 4. CONCLUSIONS

An LDO voltage regulator, based on a two-stage cascaded OTA with body bias technique, was investigated in this paper. The circuit was designed using 130 nm CMOS technology and simulated in

Mentor Graphic software with the TSMC library. An OTA was used as the error amplifier. An input voltage of 5 V was used to provide a regulated output voltage of 4.5 V. The LDO regulator has a drop out voltage of 32.06 mV at the full load condition, which is significantly lower than those of other recently published works. The power dissipation of the proposed design is only 1.3593 mW, and with a much smaller layout area, this design is suitable for low-power applications.

## REFERENCES

[1] M. Marufuzzaman, M.B.I. Reaz, and M.A.M. Ali, *Proc. of the Int. Conf. on Computer Applications and Industrial Electronics* (IEEE, Kuala Lumpur, Malaysia, 2010) p. 600-603.

[2] S. Kumar, P. Jay, and R. Prasad, *Int. J. Res. Eng. Technol.*, **3**, 2319 (2014). [DOI: http://dx.doi.org/10.15623/ijret.2014.0304168]

[3] A. Saberkari, E. Alarcón, and S. B. Shokouhi, *Integration, the VLSI Journal*, **46**, 165 (2013). [DOI: http://dx.doi.org/10.1016/j.vlsi.2012.02.001]

[4] L. F. Rahman, M.B.I. Reaz, M.A.M. Ali, and M. Marufuzzaman, *Elektronika ir Elektrotechnika*, **120**, 113 (2012). [DOI: http://dx.doi.org/10.5755/j01.eee.120.4.1466]

[5] W. Oh and B. Bakkaloglu, *IEEE Transactions on Circuits and Systems*, **54**, 922 (2007). [DOI: http://dx.doi.org/10.1109/tcsii.2007.901621]

[6] R. J. Milliken, J. Silva-Martinez, and E. Sanchez-Sinencio, *IEEE Trans. on Circuits and Systems I: Regular Papers*, **54**, 1879 (2007). [DOI: http://dx.doi.org/10.1109/TCSI.2007.902615]

[7] H. Martínez-García, *Proc. the 2014 IEEE Emerging Technology and Factory Automation (ETFA)* (IEEE, Barcelona, Spain, 2014) p. 1. [DOI: http://dx.doi.org/10.1109/etfa.2014.7005343]

[8] A. Hicham and H. Qjidaa, *Proc. 2012 IEEE International Conference on Complex Systems (ICCS)* (IEEE, Agadir, Morocco, 2012) p. 1–4. [DOI: http://dx.doi.org/10.1109/ICoCS.2012.6458540]

[9] K. Kim, W. Park, D. Kim, J. Park, B. Song, and Y. Koo, *Proc. TENCON 2012 IEEE Region 10 Conference* (IEEE, Cebu, Philippines, 2012) p. 1–5. [DOI: http://dx.doi.org/10.1109/tencon.2012.6412315]

[10] M. Kayal, F. Vaucher, and P. Deval, *Proc. 2006 Proceedings of the 32nd European Solid-State Circuits Conference* (IEEE, Montreux, Switzerland, 2006) p. 536–539. [DOI: http://dx.doi.org/10.1109/ESSCIR.2006.307508]

[11] E. Abiri, M. R. Salehi, and S. Mohammadalinejadi, *Proc. 2013 21st Iranian Conference on Electrical Engineering (ICEE)* (IEEE, Mashhad, Iran, 2013) p. 1–5. [DOI: http://dx.doi.org/10.1109/IranianCEE.2013.6599866]

[12] D. Dwibedy, S. Alapati, S. Patri, and K. Ksr, *Proc. TENCON 2014 - 2014 IEEE Region 10 Conference* (IEEE, Bangkok, Thailand, 2014) p. 1-5. [DOI: http://dx.doi.org/10.1109/TENCON.2014.7022398]

[13] S. R. Patri, S. Alapati, S. Chowdary, and K. Prasad, *18th Int. Symp. VLSI Des. Test* (Coimbatore, 2014) p. 1-5.