JPE 17-5-22

https://doi.org/10.6113/JPE.2017.17.5.1349
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

An Interleaved Converter for 12-pulse Rectifier Harmonic Suppression

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Abstract

In order to further improve the harmonic suppression capability of conventional 12-pulse rectifiers, this paper proposes a low harmonic 12-pulse rectifier using an Active Inter-Phase Reactor (AIPR). Through a detailed analysis of the relationship between the input current, output current and circulating current of the DC side, the mechanism where the AC grid side current harmonics can be suppressed by the DC side circulating current is revealed. On this basis, an interleaved APFC controlled by a DSP is designed and used as an AIPR along with an interphase reactor. A simulation is carried out with MATLAB/Simulink and an experiment is performed on a 9-kVA prototype. The obtained results verify the feasibility and validity of the proposed approach. Compared with a traditional 12-pulse rectifier, the THD can be reduced to 1/5 of the original value, and the capacity of the AIPR is only 2% of the load power. Thus, it is suitable for high-power applications.

Key words: 12-pulse rectifier, AIPR, Interleaved APFC, THD

I. INTRODUCTION

In high-power AC-DC converters, owing to the advantages of simple structure, low cost, and high reliability, 12-pulse rectifiers are often used to restrain AC grid side current harmonics and DC output side voltage ripples [1]-[5]. In theory, they can completely eliminate the 5th and 7th harmonics and the THD of the input line current is around 15%. However, this value is still unable to meet several of the compulsory harmonic current standards or guidelines, such as IEEE-519 and IEC 1000-3. Therefore, scholars have proposed various methods to further improve the harmonic suppression capability of multi-pulse rectifiers (MPRs) [6]-[13].

An application of the current injection method to 12-pulse rectifiers has been reported [6], and the current injection network is composed of passive components. As a result, the actual selection is inconvenient due to the fact that the calculated value is nonstandard. The harmonic suppression effect is also affected by the aging of elements. Miyairi et al. [7] have used an inter-phase reactor (IPR) with a tap changer for harmonic elimination. Pan et al. [8] have discussed the critical value of the IPR with a tap changer. However, the decrease of the ac mains current THD is limited, and the two additional switching devices linked with the taps of the IPR are in series with the load. All of the load current flows through the switching devices. Villablanca et al. [9] have reported a 12-pulse rectifier with high quality current waveforms from the ac mains. However, the proposed rectifier suffers from the losses generated by switches, which are in series with the outputs of the bridge rectifiers. Raju et al. [10] have reported a 12-pulse rectifier for harmonic reduction through a dc bus modulation. However, it lacks further analysis and experimental verification. Choi et al. [11] have proposed a unity power factor rectifier that actively shapes the input current by means of two boost converters operating at the CCM, which is suitable for occasions with a higher voltage level. Because the two boost converters are connected in the main circuit, the volt-ampere (VA) rating is high and the loss is serious in high-power occasions. The authors of [12] have provided another power factor rectifier that actively shapes the input current by means of two full bridge converters operating at the CCM, which is suitable for occasions with a low-voltage and a high-current. However, the complexity of the circuit topology and the number of components restrict the expansion of applications. Lee et al. [13] have proposed a 12-pulse rectifier topology with a lower component count. A PWM current source is employed to shape the input current for a clean input power. However, the VA rating of the PWM current source is 15.26% of the output power, and the energy

Manuscript received Sep. 9, 2016; accepted Apr. 18, 2017
Recommended for publication by Associate Editor Trillion Q. Zheng.
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flow direction of the PWM current source is not clear.

On the basis of the above analysis, it is known that harmonic suppression techniques for 12 pulse rectifiers can be divided into two kinds, namely the active mode and passive mode. The active mode is more popular because of its outstanding practical value and excellent harmonic suppression capability. However, in the active mode, the active current modulation circuit suffers from a high VA rating and serious losses.

In order to overcome these imperfections, this paper presents a novel low harmonic 12-pulse rectifier with an active current modulation circuit at the DC side. The advantages of the proposed method are highlighted as follows.

1) A low VA rating (2.35% P_o) PWM converter is enough to shape the input line current as a sine wave.
2) The PWM converter and a conventional 12-pulse rectifier are connected in parallel rather than in series, which makes the current stress and losses very low.
3) A digital control mode for the PWM converter using a Piccolo TMS320F2802x series microcontroller enables the design and implementation to be simpler and easier.
4) The proposed novel rectifier is robust. If the PWM converter malfunctions, the proposed rectifier can still operate in the conventional 12-pulse mode with the 5th and 7th harmonics completely eliminated.

Therefore, this research further enhances the application level of MPRs. The proposed rectifier is discussed in detail in the following sections.

II. The Harmonic Suppression Principle of 12 Pulse Rectifier Systems

Fig. 1 shows the proposed configuration of the main circuit, which includes a delta-connected auto-transformer, two three-phase bridges, a ZSBT, a two-winding AIPR, and a PWM converter. The auto-transformer offers two sets of three-phase voltages for the three-phase bridges. They are denoted as RecI and RecII, respectively. The negative terminals of the three-phase bridges are connected through ZSBT, while the positive terminals of the three-phase bridges are connected to the primary winding of the AIPR through the ZSBT. A PWM Converter is in series with the secondary winding of the AIPR. The output of the PWM Converter is directly connected to the load resistance R_d.

Fig. 2 illustrates the delta-connected autotransformer. Fig. 2(a) shows the winding configuration of the autotransformer. N_1 is the triangle winding, and N_2 is the tapped winding. The auto-transformer tap position coefficient K_1 satisfies:

$$K_1 = \sqrt{3}N_2 : N_1 = \tan 15° \quad (1)$$

Two sets of equal amplitude three-phase voltages with a 30° phase shift can be supplied to the rectifier bridge. Therefore, the outputs of the rectifier bridge are two sets of equal amplitude 6-pulse DC voltages with a 30° phase shift. Fig. 2(b) shows a voltage vector diagram of the autotransformer.

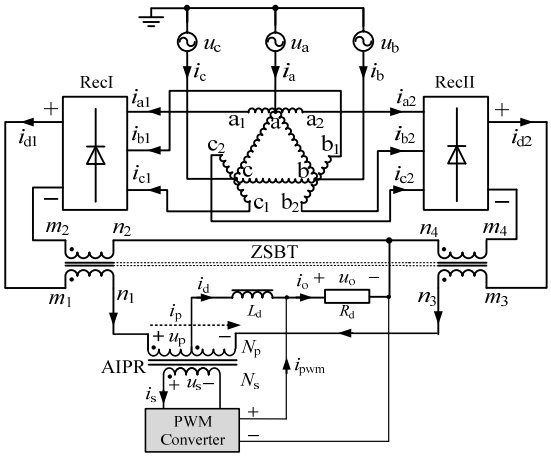
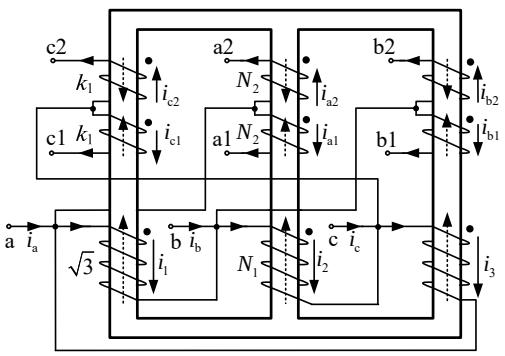
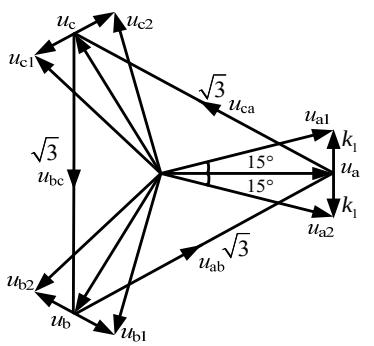


Fig. 1. Proposed main circuit configuration of the 12-pulse auto-transformer rectifier.



(a)



(b)

Fig. 2. Delta-connected autotransformer. (a) Winding configuration. (b) Voltage vector diagram.

Compared with an isolated transformer, the adopted autotransformer has a smaller volume, lower cost, higher efficiency and reduced weight.

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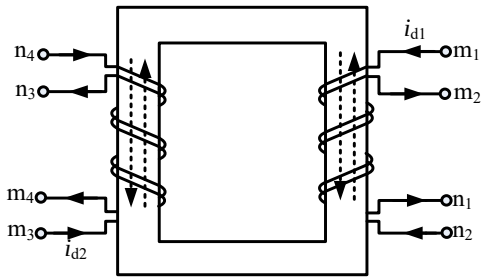
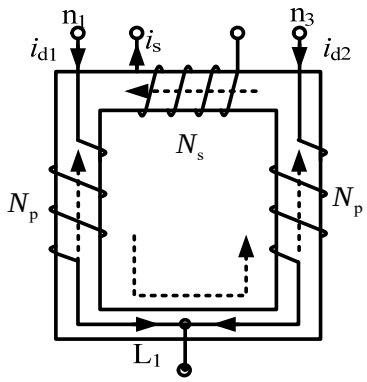


(a)



(b)

Fig. 3. ZSBT and AIPR. (a) Winding configuration of the ZSBT. (b) Winding configuration of the AIPR.

Due to the non-isolation of the autotransformer, a ZSBT is added to the proposed main circuit. Because the ZSBT exhibits a high impedance to zero sequence currents and promotes a 120° conduction for each of the rectifier diodes, it can ensure that the system works properly. The winding configuration of the ZSBT is shown in Fig. 3(a). In order to achieve the two rectifier bridge parallel operation, the AIPR is used to balance the two bridge rectifier instantaneous difference of the output voltage. Fig. 3(b) shows the winding configuration of the AIPR.

In order to facilitate the analysis system current characteristics, assume that the system output is a large inductance load, namely the load current i_d is constant DC I_d, and the autotransformer, ZSBT and AIPR are all ideal magnetic devices. From Fig. 1, Fig. 2, and the magnetic potential balance equation, the input line currents can be expressed as:

$$\begin{cases} i_a = i_{a1} + i_{a2} + K_1/\sqrt{3}\,(i_{c2} - i_{b2} + i_{b1} - i_{c1}) \\ i_b = i_{b1} + i_{b2} + K_1/\sqrt{3}\,(i_{a2} - i_{c2} + i_{c1} - i_{a1}) \\ i_c = i_{c1} + i_{c2} + K_1/\sqrt{3}\,(i_{b2} - i_{a2} + i_{a1} - i_{b1}) \end{cases} \tag{2}$$

In order to analyze the current relationship between the two sides of the rectifier bridge, the rectifier bridge switching function is defined as $S_{a1}(\omega t) = i_{a1}/i_{d1}$.

According to the three-phase rectifier system theory, the current relationship between the input and output of a rectifier bridge satisfies Eq. (3).

$$\begin{cases} i_{a1} = S_{a1} i_{d1} \\ i_{b1} = S_{b1} i_{d1} \\ i_{c1} = S_{c1} i_{d1} \end{cases}, \quad \begin{cases} i_{a2} = S_{a2} i_{d2} \\ i_{b2} = S_{b2} i_{d2} \\ i_{c2} = S_{c2} i_{d2} \end{cases} \tag{3}$$

where S_{a1}, S_{b1}, S_{c1}, S_{a2}, S_{b2} and S_{c2} are switching functions of the rectifier bridge. According to the direction of the circulation i_p marked in Fig. 1, the output currents of RecI and RecII can be calculated as:

$$\begin{cases} i_{d1} = 0.5 I_d + i_p \\ i_{d2} = 0.5 I_d - i_p \end{cases} \tag{4}$$

From Eqs. (2) to (4), the relationship between the input line currents of the 12-pulse rectifier, the load current and the DC side circulation should satisfy:

$$\begin{cases} i_a = 0.5 A_1 I_d + A_2 i_p \\ i_b = 0.5 B_1 I_d + B_2 i_p \\ i_c = 0.5 C_1 I_d + C_2 i_p \end{cases} \tag{5}$$

where:

$$\begin{cases} A_1 = S_{a1} + S_{a2} + K_1(S_{b1} - S_{c1} + S_{c2} - S_{b2})/\sqrt{3} \\ A_2 = S_{a1} - S_{a2} + K_1(S_{b1} - S_{c1} + S_{b2} - S_{c2})/\sqrt{3} \\ B_1 = S_{b1} + S_{b2} + K_1(S_{c1} - S_{a1} + S_{a2} - S_{c2})/\sqrt{3} \\ B_2 = S_{b1} - S_{b2} + K_1(S_{c1} - S_{a1} + S_{c2} - S_{a2})/\sqrt{3} \\ C_1 = S_{c1} + S_{c2} + K_1(S_{a1} - S_{b1} + S_{b2} - S_{a2})/\sqrt{3} \\ C_2 = S_{c1} - S_{c2} + K_1(S_{a1} - S_{b1} + S_{a2} - S_{b2})/\sqrt{3} \end{cases}$$

Obviously the AIPR primary side circulation i_p can affect the input current. Therefore, a suitable circulation can achieve the purpose of suppressing the input current harmonics. When the input line currents are standard sine waves, the input current harmonics are completely suppressed. Namely, the input current satisfies:

$$\begin{cases} i_a = A\sin(\omega t) \\ i_b = A\sin(\omega t - 2\pi/3) \\ i_c = A\sin(\omega t + 2\pi/3) \end{cases} \tag{6}$$

From Eq. (5) and (6), it can be seen that the circulation i_p should satisfy:

$$i_p = \frac{0.5 I_d [B_1 \sin(\omega t) - A_1 \sin(\omega t - 2\pi/3)]}{A_2 \sin(\omega t - 2\pi/3) - B_2 \sin(\omega t)} \tag{7}$$

Because each item in this formula is a Fourier series expression, it is difficult to directly derive the specific expression of i_p. However, the waveform of i_p can be drawn by Matlab, which is shown in Fig. 4.

Through observation, it can be seen that the waveform of the circulating current i_p is not a standard triangular wave. In order to facilitate the theoretical analysis, the waveform is approximated to a standard symmetrical triangle wave. Its frequency is $6*f_L$ (line/grid frequency) and its amplitude is

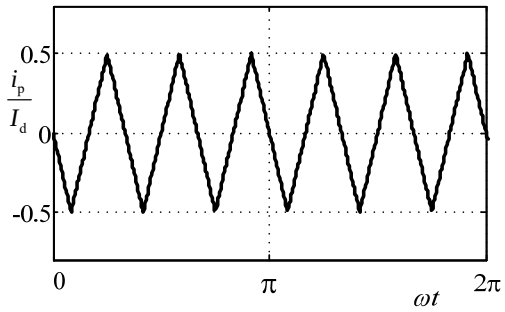


Fig. 4. Calculated waveform of i_p.

$0.5*I_d$. In addition, the zero-crossing points are at the same time as the zero-crossing points of the phase voltage. Thus, the formula for the standard symmetrical triangle i_p satisfies:

$$i_p = I_d \sum_{n=1}^{\infty} \frac{4}{n^2\pi^2} \sin\frac{3n\pi}{2} \sin(6n\omega t) \tag{8}$$

When the ratio of $2N_P$ to N_S of the AIPR is not equal to 1, the secondary winding current of the AIPR satisfies:

$$i_s = \frac{2N_p}{N_s} I_d \sum_{n=1}^{\infty} \frac{4}{n^2\pi^2} \sin\frac{3n\pi}{2} \sin(6n\omega t) \tag{9}$$

Because the voltage of the AIPR secondary winding u_s is determined by the voltage characteristic of the 12-pulse diode bridge rectifier, and according to the configuration of the 12-pulse rectifier, it can be seen that the secondary winding voltage of AIPR satisfies:

$$u_s = \frac{N_s}{2N_p} U_{out} \sum_{n=1}^{\infty} \frac{4}{36n^2-1} \sin\frac{3n\pi}{2} \sin(6n\omega t) \tag{10}$$

where U_{out} is the average value of the output voltage of the rectifier system.

From (4) and (8), it can be seen that the output currents of the two rectifier bridges satisfy:

$$\begin{cases} i_{d1} = I_d(\frac{1}{2} + \sum_{n=1}^{\infty} \frac{4}{n^2\pi^2} \sin\frac{3n\pi}{2} \sin 6n\omega t) \\ i_{d2} = I_d(\frac{1}{2} - \sum_{n=1}^{\infty} \frac{4}{n^2\pi^2} \sin\frac{3n\pi}{2} \sin 6n\omega t) \end{cases} \tag{11}$$

Their corresponding waveforms are shown in Fig. 5.

It can be concluded that the outputs of the rectifier bridges are in the critical continuous state. According to the theory of the three-phase bridge rectifier, it is possible to obtain the waveforms of the input currents of i_{a1} and i_{a2}, which are shown in Fig. 6.

Their Fourier series expression should satisfy:

$$\begin{cases} i_{a1} = I_d \sum_{n=1}^{\infty} \frac{24}{(n\pi)^2} \sin\frac{n\pi}{2} (2\cos\frac{n\pi}{6} - \cos\frac{n\pi}{3} - 1) \sin n(\omega t + \frac{\pi}{12}) \\ i_{a2} = I_d \sum_{n=1}^{\infty} \frac{24}{(n\pi)^2} \sin\frac{n\pi}{2} (2\cos\frac{n\pi}{6} - \cos\frac{n\pi}{3} - 1) \sin n(\omega t - \frac{\pi}{12}) \end{cases} \tag{12}$$

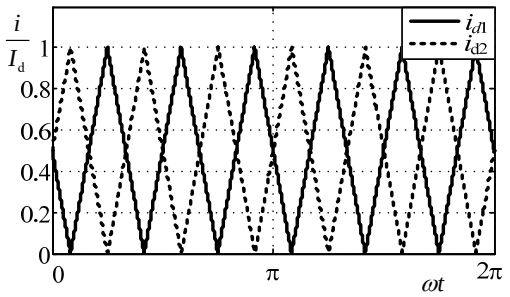


Fig. 5. Output currents of RecI and RecII.

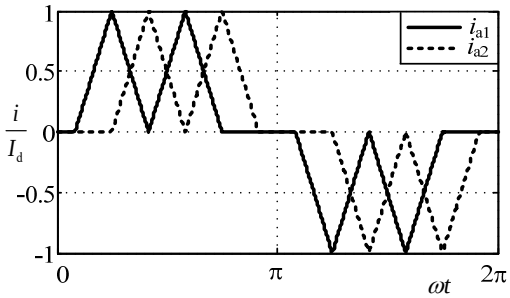


Fig. 6. Input currents of i_{a1} and i_{a2}.

Then according to formula (2), the input currents can be expressed as:

$$\begin{cases} i_a = \sum_{n=1}^{\infty} B_n \sin(n\omega t) \\ i_b = \sum_{n=1}^{\infty} B_n \sin[n(\omega t - 2\pi/3)] \\ i_c = \sum_{n=1}^{\infty} B_n \sin[n(\omega t + 2\pi/3)] \end{cases} \tag{13}$$

where:

$$B_n = \frac{48I_d}{(n\pi)^2}[\sin(\frac{n\pi}{2})(2\cos(\frac{n\pi}{6}) - \cos(\frac{n\pi}{3}) - 1)] \times[\cos(\frac{n\pi}{12}) + \frac{2k_1}{\sqrt{3}} \sin(\frac{2n\pi}{3}) \sin(\frac{n\pi}{12})]$$

The analysis above shows that the circulating current i_p can completely eliminate the 5th and 7th harmonics in the input current, and effectively eliminate the 11th and 13th harmonics. Thus, through the installation of a suitable active circuit that is paralleled with the secondary winding of AIPR and reasonable control of its current waveform, it is possible to eliminate the harmonic pollution of 12-pulse rectifiers. Fig. 7 shows voltage and current waveforms of the secondary winding of the AIPR under the related reference direction with the ratio of $2N_p$ to N_s being equal to 1.

It can be seen that the secondary winding of the AIPR can be view as a power source, and that the frequency of u_s and i_s is $6*f_L$. Therefore, the active circuit in series with the secondary winding works in the unit power factor state, and it can be equivalent to a pure resistance Rs. Its value satisfies:

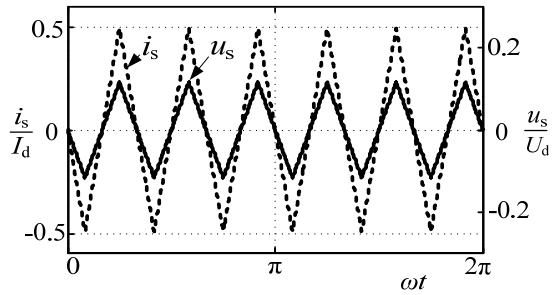


Fig. 7. Voltage and current of the secondary winding of the AIPR.

$$R_S = 0.0705\left(\frac{N_s}{N_p}\right)^2 \frac{U_d}{I_d} \tag{14}$$

The kVA rating of the AIPR should satisfy:

$$P_S = |u_s||i_s| = 0.0235 U_d I_d = 0.0235 P_o \tag{15}$$

III. Realization of the AIPR

Through the above analysis, it can be seen that the circulation of the AIPR primary winding is the key to restrain the harmonics of the input current.

APFC technology can meet the basic requirements since it can guarantee that the input voltage and current have the same frequency and phase. Because the kVA rating of the secondary winding is about 2% of the system capacity, in order to avoid a waste of harmonic energy, the output of the APFC circuit is directly parallel to the load resistance R_d for realizing the harmonic energy re-use. In addition, the output voltage of the APFC circuit is determined by the voltage characteristic of the 12-pulse rectifier system. From Eq. (10), it can be seen that the output voltage u_{out} is higher than the peak voltage of u_s. Therefore, the Boost APFC circuit topology is chosen.

However, the frequencies of u_s and i_s are both $6*f_L$, and the inductor current rising rate provided by the Boost APFC converter is very small near the input voltage zero-cross point. As a result, it is difficult to track the reference current signal. This situation leads to zero crossing distortion, and this distortion phenomenon becomes even more serious with an increase of the operating frequency [14]. Therefore, the traditional single phase Boost APFC circuit cannot meet the system control requirements.

To improve the current zero crossing distortion, scholars have put forward many measures in terms of control strategies, topology structure and other aspects, such as initial phase correction, duty-ratio-feedforward control, predictive control, bridgeless PFC, interleaved PFC, etc. [15]-[19]. The staggered parallel structure can run in interleaved parallel with multiple power units, which can effectively reduce the working time of the circuit in the discontinuous current mode (DCM) or the critical conduction mode (CRM). Although the inductor current rise rate of each element is constant, the current rise of the input current is significantly reduced. In addition, the inductance value is equivalently reduced, when the input current ripple is reduced. Therefore, interleaving parallel technology can make it easier to track the reference current [20], [21]. It should be noted that the larger the number of power units connected in parallel, the smaller the input current ripple becomes. In addition, the current tracking effect is better, but the cost and complexity of system increase, while the reliability and efficiency of the system decline. The double interleaved Boost APFC circuit is used under comprehensive considerations.

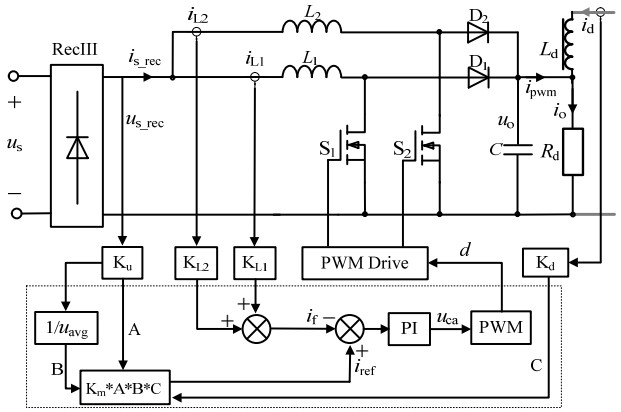


Fig. 8. System block diagram of the designed interleaved Boost PFC.

In summary, Fig. 8 shows the designed circuit system scheme. In order to realize the control of the secondary winding current of the AIPR, sampling of the following signals is required, including the input rectification voltage u_{s_rec}, the two inductor currents i_{L1} and i_{L1}, and the load current of the 12 pulse rectifier system i_d. The gain for each of the sampled signals is represented by a module. They are K_u, K_{L1}, K_{L2} and K_d. At the same time, in order to get the shape of u_{s_rec}, regardless of the magnitude of u_{s_rec}, the voltage feed-forward link is introduced. Thus, the reference signal amplitude of i_{ref} is determined by the magnitude of i_d only. The outputs of A, B and C are sent into the multiplier to produce the required current reference signal i_{ref}. The current feedback signal i_f and the reference signal i_{ref} are fed into the comparison link. The output of the comparison link is sent to the PI controller link. Then the output of the PI controller u_{ca} is sent into the PWM module to generate two staggered 180° PWM pulse signals, where d represents the duty cycle. These two signals are amplified by the PWM drive circuit to control the turn-on and turn-off of S_1 and S_2.

For the purposes of analysis and control design, the designed interleaved Boost PFC small signal model $G_{id}(s)$ in the current loop is derived. This is due to the high switching frequency of the circuit. In order to simplify the analysis, the input and output voltage are considered to be not changed in a switching cycle.

Assume that the switch devices in the circuit are ideal, and that the inductors of L_1 and L_2 have the same value, namely L_1=L_2=L, there are only two states in one switching cycle. When the switch is on, the following equation can be concluded:

$$L\frac{\mathrm{d}i_{\mathrm{s\_rec}}}{\mathrm{d}t}=u_{\mathrm{s\_rec}} \tag{16}$$

When the switch is off, the following equation can be concluded:

$$L\frac{\mathrm{d}i_{\mathrm{s\_rec}}}{\mathrm{d}t}=u_{\mathrm{s\_rec}}-u_{\mathrm{o}} \tag{17}$$

Therefore, in a switching cycle, according to the state-space averaged method, the following equation can be concluded:

$$\begin{aligned}L\frac{\mathrm{d}i_{\mathrm{s\_rec}}}{\mathrm{d}t}&=du_{\mathrm{s\_rec}}+(1-d)(u_{\mathrm{s\_rec}}-u_{\mathrm{o}})\\&=u_{\mathrm{s\_rec}}-(1-d)u_{\mathrm{o}}\end{aligned} \tag{18}$$

Applying a small-signal perturbation to the above equation, the following equations can be obtained:

$$L\frac{\mathrm{d}\hat{i}_{\mathrm{s\_rec}}}{\mathrm{d}t}=\hat{d}u_{\mathrm{o}} \tag{19}$$

Using Laplace transforms, the small signal model $G_{id}(s)$ can also be obtained:

$$G_{\mathrm{id}}(s)=\frac{\hat{i}_{\mathrm{s\_rec}}}{\hat{d}}=\frac{u_{\mathrm{o}}}{sL} \tag{20}$$

In order to facilitate the future loss analysis of the AIPR, the loss calculation formulas are derived in detail as the theoretical basis of the loss analysis.

For the sake of convenience when it comes to the formula derivation, the calculation of the duty cycle is necessary. Because the boost inductor works in the CCM, the switch duty ratio can be obtained by the volt second balance, and it can be expressed as:

$$\left|u_s\right|\times T_{on}=(u_o-\left|u_s\right|)\times T_{off} \tag{21}$$

where T_{on} and T_{off} are the turn-on and turn-off time of the switch, respectively.

Therefore, the duty ratio d can be represented as:

$$d(t)=1-\frac{\left|u_s\right|}{u_o} \tag{22}$$

A. The Loss of the Rectifier Bridge in the AIPR

For the rectifier bridge in the AIPR, there are only two diodes at any moment in the conduction state. Since the frequency of i_s is 300Hz, the frequency of $|i_s|$ is 600Hz after rectification. Therefore, the conduction loss of each diode in the rectifier bridge in a cycle T_{AIPR} can be expressed as:

$$P_{rec}=\frac{1}{\mathrm{T_{AIPR}}}\int_0^{T_{AIPR}/2}V_{rec}\times\left|i_s\right|dt \tag{23}$$

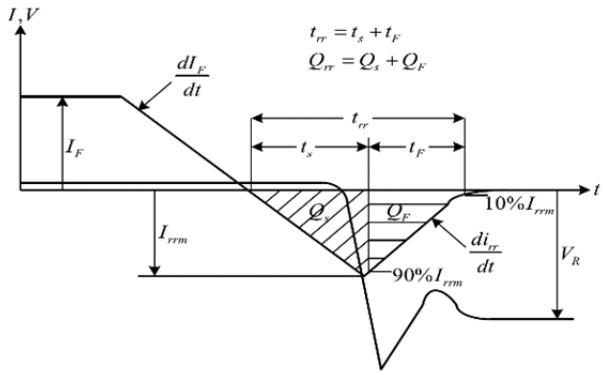


Fig. 9. The voltage and current waveforms during the turn-off time.

where V_{rec} is the forward conduction voltage drop for the internal diode of the rectifier bridge.

B. The Loss of the Fast Recovery Diode in the AIPR

1) The Conduction Loss of the Fast Recovery Diode: For interleaved parallel circuits, it is assumed that a good current sharing is achieved between the two phases of Boost. In addition, during the conduction period of the MOSFET, the current is approximately satisfied.

$$i_{mos}=i_L=\frac{i_s}{2} \tag{24}$$

Therefore, the conduction loss for each of the fast recovery diodes in a cycle TAIPR can be expressed as:

$$P_{dio\_con}=\frac{1}{T_{AIPR}}\int_0^{T_{AIPR}/2}V_{dio}\times\left|i_{mos}\right|\times[1-d(t)]dt \tag{25}$$

where V_{dio} is the forward conduction voltage drop for the internal diode of the rectifier bridge.

2) The Switching Loss of the Fast Recovery Diode: The turn-on loss for each of fast recovery diodes is very small. As a result, it can be ignored. Then the turn-off loss of each fast recovery diode is derived. Fig. 9 illustrates the voltage and current waveforms of the fast recovery diode during the turn-off time.

In order to facilitate the analysis, the assumption for Fig. 9 is given below.

$$t_s=t_f=\frac{1}{2}t_{rr} \tag{26}$$

In addition, the reverse recovery current peak I_{rrm} is proportional to the forward current I_F. The current I_{rrm} approximately satisfies:

$$I_{rrm}=K_f\times I_F=K_f\times\left|i_{mos}\right| \tag{27}$$

where K_f is the scale coefficient.

Therefore, the turn-off loss for each of the fast recovery diodes in a cycle TAIPR can be expressed as:

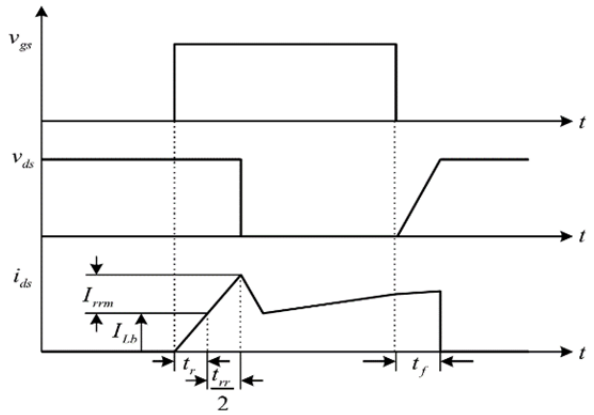


Fig. 10. Voltage and current waveforms of the MOSFETs during the turn-on and turn-off time.

$$P_{dio\_turn-off} = \frac{1}{T_{AIPR}} \int_0^{T_{AIPR}/2} \frac{1}{2} I_{rrm} \times u_o \times \frac{t_{rr}/2}{T_s} dt \tag{28}$$

C. The loss of the MOSFETs in the AIPR

1) The Conduction Loss of the MOSFETs: In a switching cycle T_s, the effective value of the power tube current is:

$$I_{mos} = i_{mos} \sqrt{d(t)} = \frac{i_s}{2} \sqrt{d(t)} \tag{29}$$

In a switching cycle T_s, the conduction loss for each of the MOSFETs can be expressed as:

$$P_{T_{S\_con}} = I^2_{mos} \times R_{ds(on)} \tag{30}$$

where $R_{ds(on)}$ is the conduction resistance of the MOSFETs.

Therefore, the conduction loss for each of the MOSFETs in a cycle T_{AIPR} can be expressed as:

$$\begin{aligned} P_{mos\_con} &= \frac{1}{T_{AIPR}} \int_0^{T_{AIPR}/2} P_{T_{S\_con}} dt \\ &= \frac{1}{T_{AIPR}} \int_0^{T_{AIPR}/2} I^2_{mos} \times R_{ds(on)} dt \end{aligned} \tag{31}$$

2) The Switching Loss of the MOSFETs: Fig. 10 shows voltage and current waveforms of the MOSFETs during the turn-on and turn-off time.

In a switching cycle T_s, the turn-on loss for each of the MOSFETs can be expressed as:

$$P_{T_{S\_turn-on}} = \frac{1}{2} (|i_{mos}| + I_{rrm}) \times u_o \times \frac{(t_{rr}/2 + t_r)}{T_s} \tag{32}$$

Therefore, the turn-on loss for each of the MOSFETs in a cycle T_{AIPR} can be expressed as:

$$\begin{aligned} P_{mos\_turn-on} &= \frac{1}{T_{AIPR}} \int_0^{T_{AIPR}/2} P_{T_{S\_turn-on}} dt = \frac{1}{T_{AIPR}} \\ &\times \int_0^{T_{AIPR}/2} \frac{1}{2} (|i_{mos}| + I_{rrm}) \times u_o \times \frac{(t_{rr}/2 + t_r)}{T_s} dt \end{aligned} \tag{33}$$

In a switching cycle T_s, the turn-off loss for each of the MOSFETs can be expressed as:

$$P_{T_{S\_turn-off}} = \frac{1}{2} |i_{mos}| \times u_o \times \frac{t_f}{T_s} \tag{34}$$

Therefore, the turn-off loss for each of the MOSFETs in a cycle T_{AIPR} can be expressed as:

$$\begin{aligned} P_{mos\_turn-off} &= \frac{1}{T_{AIPR}} \int_0^{T_{AIPR}/2} P_{T_{S\_turn-off}} dt \\ &= \frac{1}{T_{AIPR}} \int_0^{T_{AIPR}/2} \frac{1}{2} |i_{mos}| \times u_o \times \frac{t_f}{T_s} dt \end{aligned} \tag{35}$$

Accordingly, in a cycle T_{AIPR}, the total loss of the switching devices in the AIPR can be expressed as:

$$\begin{aligned} P_{loss} &= 4 \times P_{rec} + 2 \times (P_{dio\_con} + P_{dio\_turn-off}) \\ &+ 2 \times (P_{mos\_con} + P_{mos\_turn-on} + P_{mos\_turn-off}) \end{aligned} \tag{36}$$

IV. Sensitivity Analysis

Mismatching in the control loop or voltage unbalance in the AC grid side are possible situations in a 12-pulse rectifier with the AIPR. Therefore, it is necessary to conduct some analyses.

Firstly, the influence of the mismatching of the circulating current in the control loop on the input current of the system to determine the relationship between harmonic suppression effects and circulating current parameters.

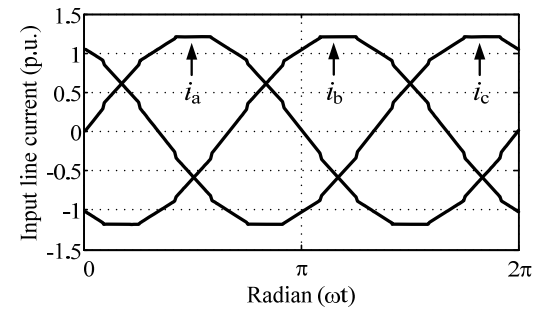
The circulating current amplitude i_{pm} satisfies:

$$i_{pm} > 0.5 I_d \tag{37}$$

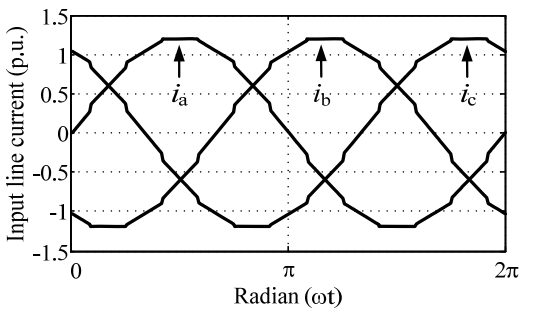
From Eq. (11) and Fig. 5, it is know that the rectifier output current is negative, and the diode rectifier bridge current can only have a one-way flow. At this time, the bridge works in the discontinuous state, and the system does not work properly. Therefore, in order to ensure normal operation of the system, it is necessary to ensure that the circulating current amplitude i_{pm} satisfies:

$$i_{pm} \le 0.5 I_d \tag{38}$$

Hence, under the condition of a constant circulating current phase, the harmonic suppression effect of the input current is given under different values of i_{pm}, which satisfies Eq. (38). Fig. 11 (a) and (b) illustrates two cases of the three-phase input current waveform and their THD values. Fig. 12 shows the change rule curve of the input current THD value when the circulation amplitude i_{pm} changes from $0.25I_d$ to $0.5I_d$. From Fig. 11, when the circulating current amplitude decreases, the harmonic suppression effect becomes worse and the THD value increases. From Fig. 12, when the circulating current amplitude becomes lower, the THD value becomes larger, and the harmonic suppression effect becomes



(a)



(b)

Fig. 11. input current waveforms under different values of i_{pm}. (a) i_{pm}/I_d=0.45, THD=1.7%. (b) i_{pm}/I_d =0.4, THD=2.8%.

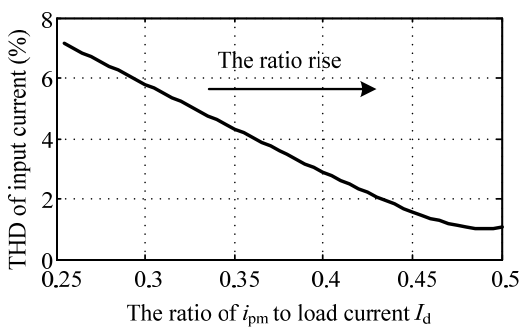


Fig. 12. THD curve of the input current under different values of i_{pm}.

worse. When i_{pm} is equal to $0.5I_d$, the system achieves the best harmonic suppression effect.

Then, under the condition of a i_{pm} that is equal to $0.5I_d$, the harmonic suppression effect of the input current is given under different phases of the circulating current, which is based on the zero crossing of the phase voltage. Fig. 13 illustrates six cases of three-phase input current waveforms and their THD values. Fig. 14 shows the change rule curve of the input current THD value when the phase of the circulating current changes from -π/12 to π/12. From Fig. 13, the lead or lag of the circulation phase can lead to a distortion of the input current waveform, and the THD value increases. In addition, it leads to input line current phase lead or lag, which reduces the power factor of the rectification system. From Fig. 14, it can be seen that with an increase of the phase lead or phase lag of the circulation phase, the distortion becomes more serious.

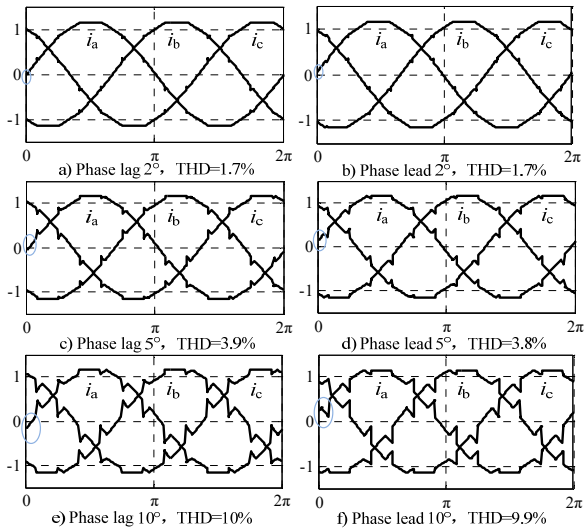


Fig. 13. Input current waveforms under different phases of i_p.

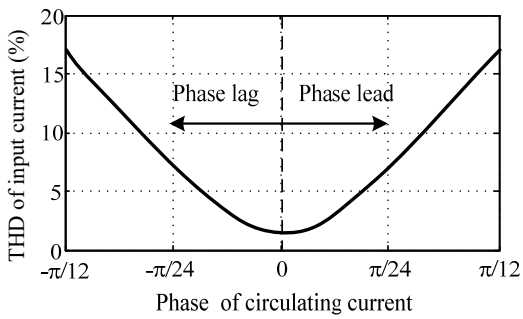


Fig. 14. THD curve of input current under different phases of i_p.

Secondly, the influence of the voltage unbalance in the AC grid side on the input current of the system is analyzed to determine the relationship between the harmonic suppression effect and the supply voltage parameters.

Under ideal conditions, the AC grid side voltages are balanced, namely the input voltage satisfies:

$$\begin{cases} u_a = U_m \sin(\omega t) \\ u_b = U_m \sin(\omega t - 2\pi/3) \\ u_c = U_m \sin(\omega t + 2\pi/3) \end{cases} \tag{39}$$

where U_m is the peak amplitude of the input voltage.

However, for various reasons, the voltage is sometimes unbalanced. Hence, under the condition of the input voltage phase balance, the harmonic suppression effect of the input current is given under the condition that the amplitude of phase A is out-off-balance. Assume the input voltage as:

$$\begin{cases} u_a = (U_m + u)\sin(\omega t) \\ u_b = U_m \sin(\omega t - 2\pi/3) \\ u_c = U_m \sin(\omega t + 2\pi/3) \end{cases} \tag{40}$$

where u is a amplitude variable.

Fig. 15 (a) and (b) illustrate two cases of three-phase input current waveforms and their THD values. Fig. 16 shows the

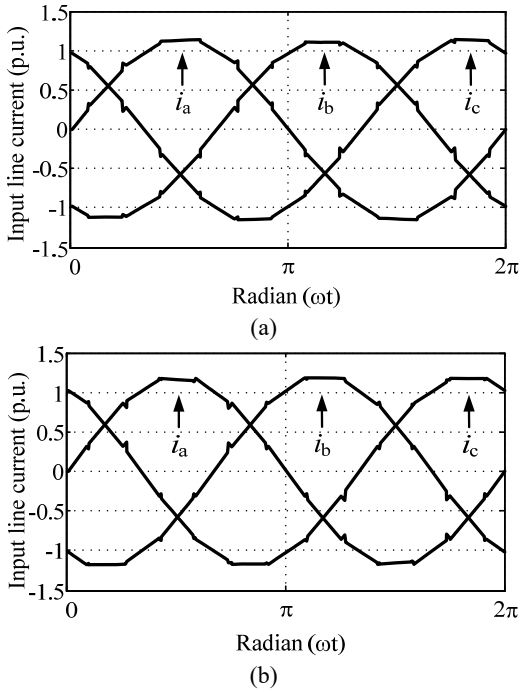


Fig. 15. Input current waveforms under different values of u. (a) u=0.15U_m, THD=2.51%. (b) u=-0.15U_m, THD=2.51%.

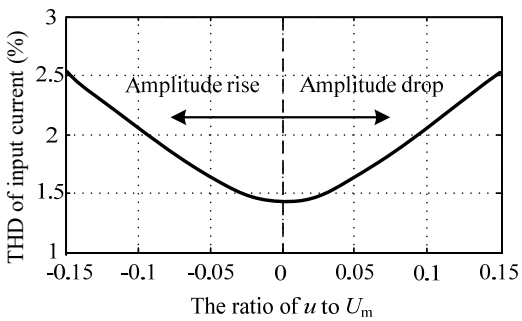


Fig. 16. THD curve of the input current under different ratios of u to U_m.

change rule curve of the input current THD value when the ratio of u to U_m changes from -0.15 to 0.15. From Fig. 15, the rise or drop of the amplitude of phase A can lead to a distortion of the input current waveform, and the THD value increases. From Fig. 16, it can be seen that both the amplitude rise and amplitude drop lead to distortions of the input line current, and that the greater the amplitude rise or amplitude drop, the more serious the distortion becomes. When the amplitudes of the AC grid side voltage are balanced, the system achieves the best harmonic suppression effect.

Then, under the condition of input voltage amplitude balance, the harmonic suppression effect of the input current is given under the condition that the phase of phase A is out-off-balance. Assume the input voltage as:

$$\begin{cases} u_a = U_m \sin(\omega t + \theta) \\ u_b = U_m \sin(\omega t - 2\pi/3) \\ u_c = U_m \sin(\omega t + 2\pi/3) \end{cases} \quad (41)$$

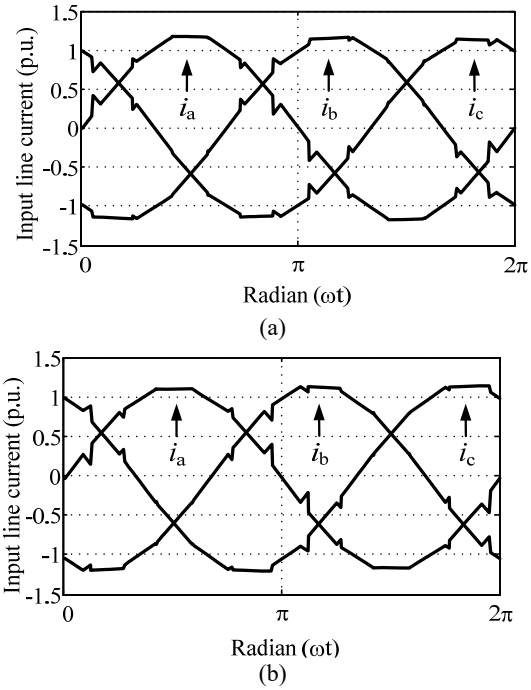


Fig. 17. The input current waveforms under different θ. (a) θ =π/18, THD=3.7%. (b) θ=-π/18, THD=3.7%.

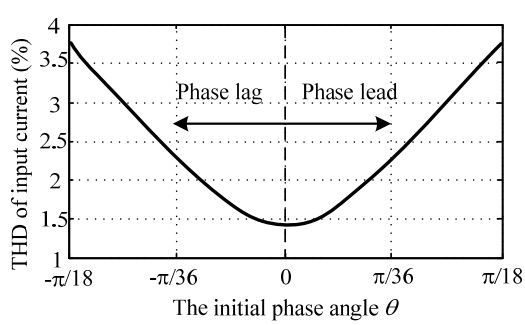


Fig. 18. The THD curve of input current under different θ.

where θ is an initial phase angle variable.

Fig. 17 (a) and (b) illustrate two cases of three-phase input current waveforms and their THD values. Fig. 18 shows the change rule curve of the input current THD value when θ changes from -π/18 to π/18. From Fig. 17, the lag or lead of the phase of phase A can lead to a distortion of the input current waveform, and the THD value increases. From Fig. 18, it can be seen that both the phase lag and phase lead result in distortions of the input line current, and that the greater the phase lag and phase lead, the more serious the distortion becomes. When the phases of the AC grid side voltage are balanced, the system achieves the best harmonic suppression effect.

V. Simulation and Experimental Verification

The proposed system is simulated with SIMULINK and a 9kW prototype is built to verify the validity of the proposed

TABLE I
PARAMETERS FOR THE SIMULATIONS AND EXPERIMENTS

Parameter	Value	Parameter	Value
Output voltage U_o	530V	Turn ratio of AIPR	1:3
Load current I_d	17A	switching frequency f_{sw}	100kHz
Input line voltage U	380V	sampling frequency f_{sa}	100kHz
Line frequency f_L	50Hz	RecI and RecII	MDS30-12 1200V/30A
Output power P_o	9kW	RecIII	RS406 600V/4A
Load inductance L_d	10mH	S_1 and S_2	IRFPE50 800V/7.8A
Load resistance R_d	30Ω	D_1 and D_2	MURS260 600V/2A
Boost inductance L_1 and L_2	300μH		

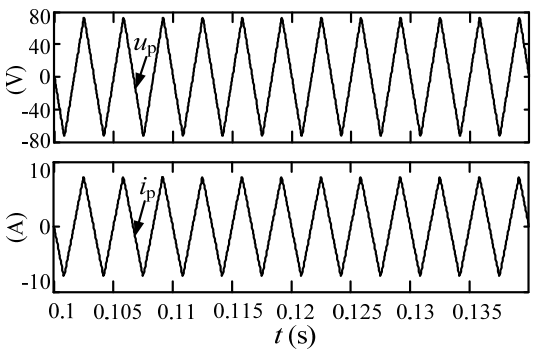


Fig. 19. Voltage and current of the primary winding of the AIPR.

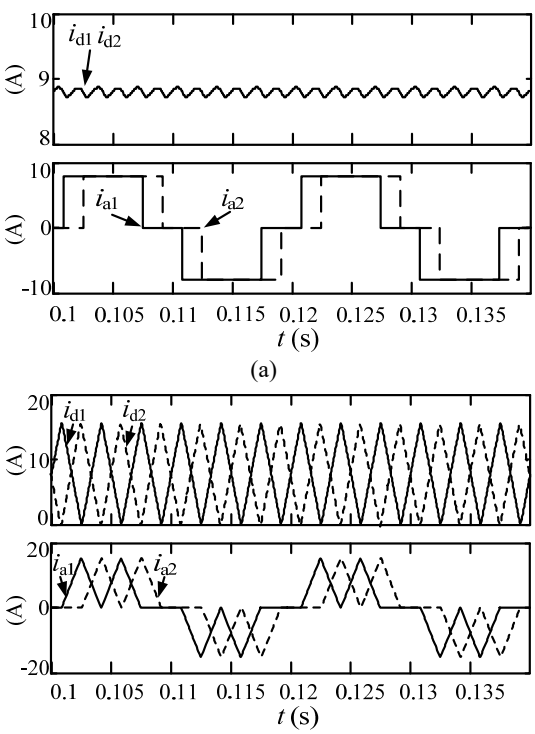


Fig. 20. Current comparison of both sides of the rectifier bridge: (a) before modulation; (b) after modulation.

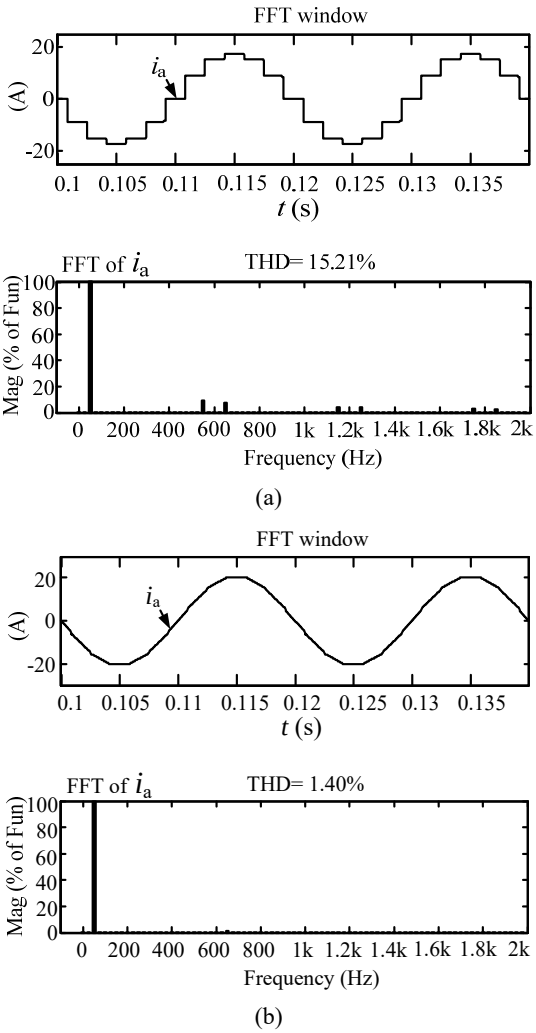


Fig. 21. Comparison of the input line current and its spectrum: (a) before modulation; (b) after modulation.

scheme. Table I shows the parameters for the simulations and experiments.

Fig. 19 shows the voltage and current of the primary winding of the AIPR. Both the voltage u_p and the current i_p are $6*f_L$ symmetrical triangular waves and in phase. In addition, the current amplitude is 0.5 I_d. The simulation results show good agreement with the theoretical analysis.

The circulating current i_p affects the input and output currents of RecI and RecII. Fig. 20 shows a current comparison on both sides of the rectifier bridge before and after current modulation. It is obvious that the two bridge rectifiers operate under the critical conduction mode after current modulation.

Eventually the circulating current i_p leads to a difference in the input line current. Fig. 21 shows a current comparison of input line current and its spectrum before and after the current modulation. Obviously the circulating current realizes suppression of the system input current harmonics. Through the spectrum analysis of the input line current, when compared with the conventional 12 pulse system, the proposed system completely eliminates the 5th and 7th

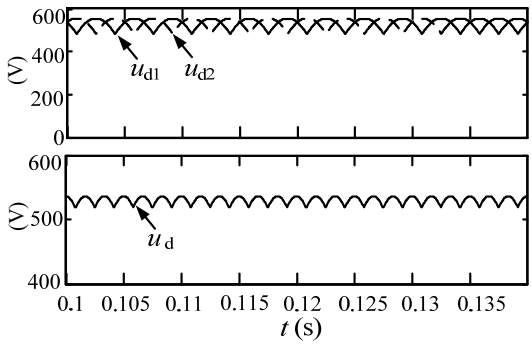


Fig. 22. Output voltages of the rectifier bridge and system.

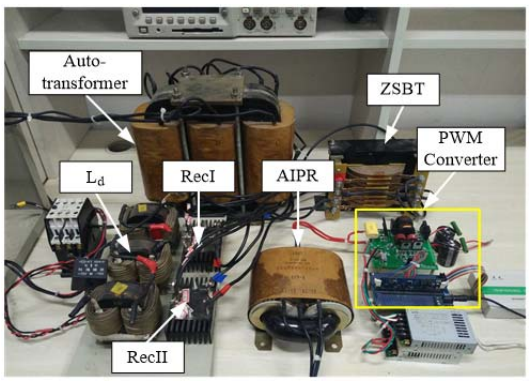


Fig. 23. Experimental setup of a 12-pulse rectifier based on an interleaved Boost PFC type AIPR.

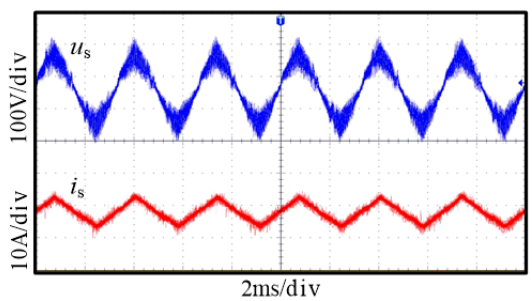


Fig. 24. Voltage and current of the secondary winding of the AIPR.

harmonics of the input current, and effectively reduces the 11th and 13th harmonics content. The THD of the input line current is reduced to about 1.4%. The correctness of the theoretical analysis is verified by simulation results.

Fig. 22 illustrates the output voltages of RecI and RecII, and the load voltage. Simulation results show that the voltage characteristic is not affected by the PWM Converter, which is in consistent with the theoretical analysis.

In order to verify the validity of the above analysis, an experimental setup was built. Fig. 23 is a photograph of the proposed 12-pulse rectifier based on an interleaved converter.

Fig. 24 illustrates the output characteristic of the AIPR secondary winding. It can be seen from the experimental waveform that good tracking performance is achieved. Voltage and current waveforms are symmetrical triangular waves with $6*f_L$, and they are in phase. The experimental

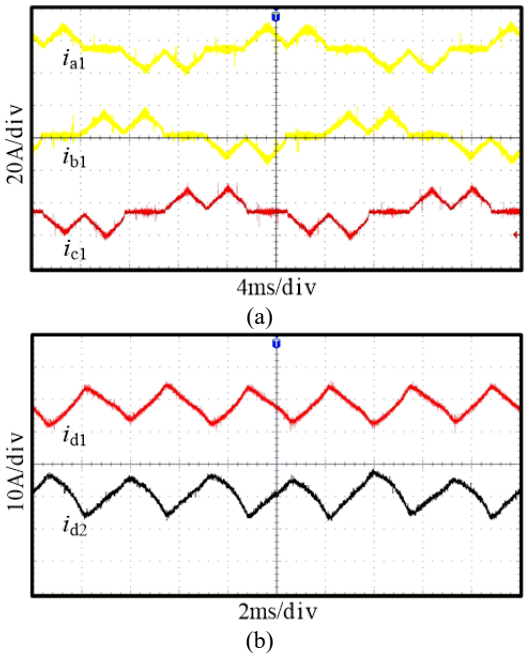


Fig. 25. Current characteristic: (a) input currents of RecI; (b) output currents of RecI and RecII.

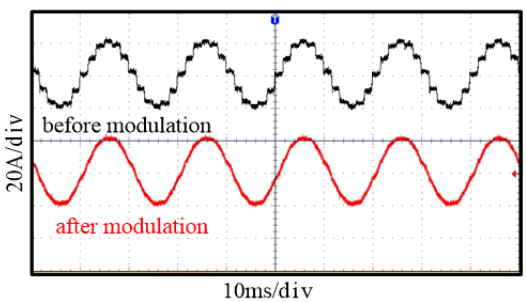


Fig. 26. Comparison of the input line current before and after modulation.

results are in agreement with the theoretical analysis and simulation results.

Fig. 25 illustrates the input and output current characteristic of a three-phase bridge. Fig. 25(a) shows the input currents of RecI. It is obvious that the input currents are symmetrical periodic waves with equal amplitudes and that they have a 120° phase shift between each other. Fig. 25(b) shows the output currents of RecI and RecII. The output currents of the two three-phase bridge are critical continuous symmetrical triangular waves due to the circulating current, and their phase shift is 180°.

The aim of the current modulation is to reduce the current harmonics of the input line currents. Fig. 26 illustrates a comparison of the input line current before and after modulation. It can be seen that the waveform has been changed from the original 12 step into a sine wave, and that the input current quality has been significantly improved.

Fig. 27 illustrates the voltage and current waveforms of the load resistance R_d.

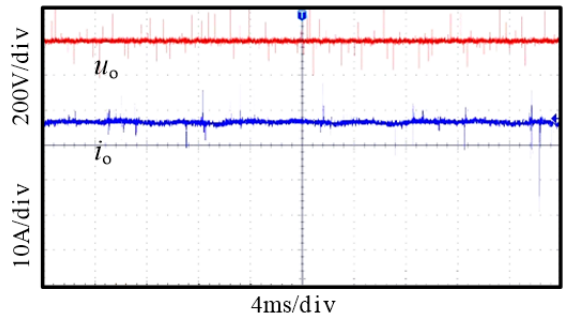
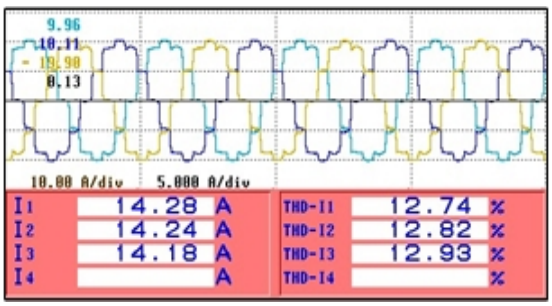
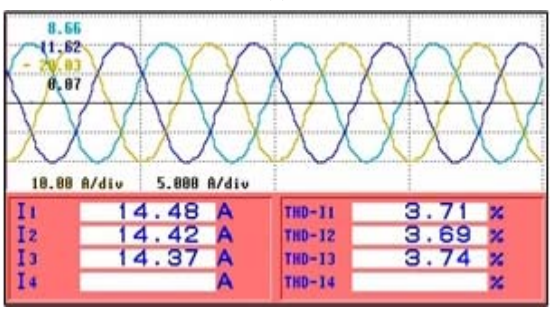


Fig. 27. The voltage and current of the load resistance R_d.



(a)



(b)

Fig. 28. Comparison of the input line current and its quality; (a) before modulation; (b) after modulation.

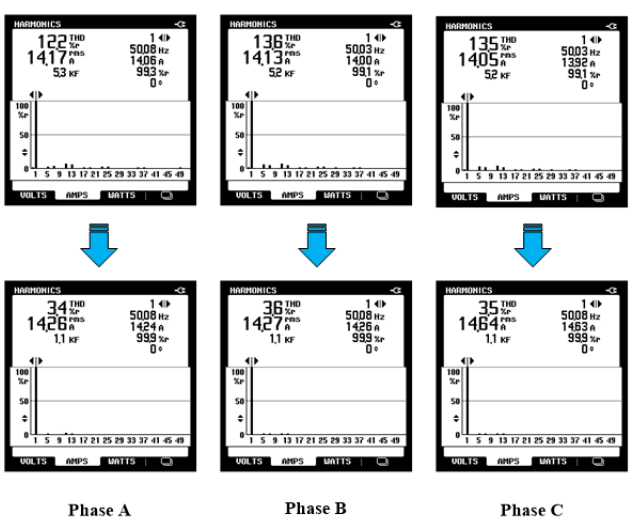


Fig. 29. Comparison of the THD levels and harmonic distribution before (upper Figs.) and after (lower Figs.) the proposed method is implemented.

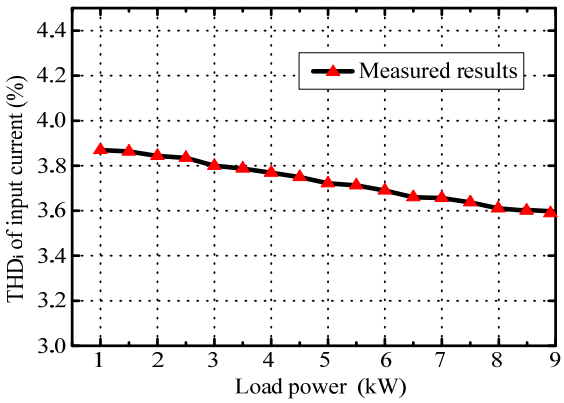


Fig. 30. THD_i curve under different load powers.

In order to compare the effects of the harmonic suppression, the THD values are measured by a three phase power quality analyzer. Fig. 28 illustrates the measurement results. Fig. 28(a) shows the input current waves and their THD values before modulation. It is obtained that the whole system operates as a 12-pulse ac-dc converter. Fig. 28(b) shows the input current waves and their THD values after modulation. It is obtained that the input current is close to a sine wave. The harmonic suppression effect is remarkable.

To better highlight the performance of the proposed technique, the obtained harmonic levels and harmonic distribution for each of the phases are compared in Fig. 29. This further proves the effectiveness of the harmonic suppression.

Fig. 30 shows the THD curve under different load powers. It is obvious that the THD values of the proposed 12-pulse rectifier are reduced significantly when the load power varies on a large scale.

From the aforementioned simulation and experimental results, the method proposed in this paper can effectively overcome the selection inconvenience and aging of the passive elements discussed in [6]. Moreover, since the AIPR and the main circuit are in parallel in this system, it avoids the drawbacks of the Tapped IPR technique mentioned in [7]. Compared with other dc bus modulation techniques, the AIPR in this paper is not in series with the DC side of the main circuit. This decreases the power level of the elements in the AIPR and increases the reliability of the circuit. Even if the AIPR is damaged, the main circuit can still work in the conventional 12-pulse mode. In addition, both simulation and experimental results show that the method proposed in this paper can effectively suppress the current harmonics of the AC grid side. In further investigations, the authors of this paper will focus on the research on the following: the case of a higher power level, when the problem of unequal sharing of the load between the two boost converter stages exists, the influence on system performance, and how to solve it. In addition, a loss analysis of the AIPR will be discussed in depth.

VI. CONCLUSIONS

In this paper, an active circuit is utilized to reduce the harmonic of the input line current in a 12-pulse rectifier. Theoretical analyses show that the system input current harmonics can be effectively eliminated by extracting an appropriate current waveform from the dc side of the system. A double interleaved parallel Boost APFC circuit is designed as the active circuit. Simulation and experimental results show that the proposed circuit can guarantee the current tracking effect, which can ensure the effects of harmonic suppression. The kVA rating of the active circuit is only 2% of the output power. Compared with the traditional 12-pulse rectifier, the proposed method is effective and efficient in high power applications.

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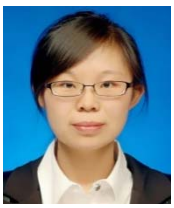

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