JPE 17-5-11

https://doi.org/10.6113/JPE.2017.17.5.1231
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Design of a High-performance High-pass Generalized Integrator Based Single-phase PLL

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Abstract

Grid-interactive power converters are normally synchronized with the grid using phase-locked loops (PLLs). The performance of the PLLs is affected by the non-ideal conditions in the sensed grid voltage such as harmonics, frequency deviations and the dc offsets in single-phase systems. In this paper, a single-phase PLL is presented to mitigate the effects of these non-idealities. This PLL is based on the popular second order generalized integrator (SOGI) structure. The SOGI structure is modified to eliminate the effects of input dc offsets. The resulting SOGI structure has a high-pass filtering property. Hence, this PLL is termed as a high-pass generalized integrator based PLL (HGI-PLL). It has fixed parameters which reduces the implementation complexity and aids in the implementation in low-end digital controllers. The HGI-PLL is shown to have the lowest resource utilization among the SOGI based PLLs with dc cancelling capability. Systematic design methods are evolved leading to a design that limits the unit vector THD to within 1% for given non-ideal input conditions in terms of frequency deviation and harmonic distortion. The proposed designs achieve the fastest transient response. The performance of this PLL has been verified experimentally. The results agree with the theoretical prediction.

Key words: Current control, DC offsets, Distributed generation, Harmonic distortion, Phase-locked loops

NOMENCLATURE

PLL	Phase-locked loop.
SOGI	Second-order generalized integrator.
SRF	Synchronous reference frame.
HGI	High-pass generalized integrator.
k	Gain in HGI transfer functions.
ω_0	Nominal grid frequency ($2\pi 50$ *rad/s*).
v_g	Sensed grid voltage.
v_α, v_β	In-phase and quadrature-phase outputs of a HGI with v_g as the input.
v_d, v_q	Rotating reference frame voltages corresponding to the SRF transformation of v_α, v_β.
k_p, k_i	Proportional and integral gains of a PI controller.
ω_e	Estimated frequency of the HGI-PLL in rad/s.
θ_e	Estimated phase of the HGI-PLL in rad.
$t_{s,srf}$	Settling time due to the embedded SRF-PLL in the HGI-PLL.
$t_{s,hgi}$	Settling time due to the HGI block.
t_{sd}	Additive worst case settling time ($t_{sd} = t_{s,srf} + t_{s,hgi}$).
ω_{bw}	Design bandwidth of the embedded SRF-PLL in rad/s.
f_{bw}	Design bandwidth of the embedded SRF-PLL in Hz.
$k_{opt,h}$	Optimum value of k in a HGI that gives the fastest settling time.
U	Design limit on the unit vector THD in %.
Δf	Maximum frequency deviation considered in a grid ($\Delta f = \pm 8\%$).
u_{thd}	Unit vector THD in %.
$\boldsymbol{K_u}$	Set of k satisfying $u_{thd} \leq 1\%$ for any given f_{bw}.

Manuscript received Sep. 18, 2016; accepted May 15, 2017
Recommended for publication by Associate Editor Sung-Jin Choi.
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I. INTRODUCTION

Phase-locked loops (PLLs) are used in multiple applications ranging from miniature system on chips (SOCs) to large grid-connected power converters. In SOCs, the PLLs are used

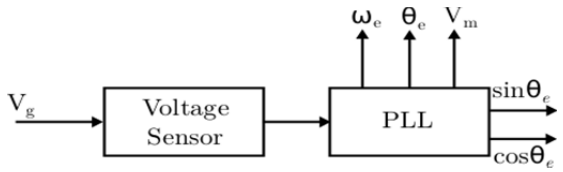


Fig. 1. General structure of a PLL used in grid-connected power converters.

for functions such as clock generation [1]. In grid-connected power converters such as distributed generation (DG) systems and static compensators (STATCOMs), the PLLs are used for synchronization with the grid voltage [2]-[7]. In this paper, the design and implementation aspects for the PLL in single-phase grid connected power converters are discussed.

The PLLs estimate the frequency, phase and amplitude of the grid voltage. They are used to generate unit amplitude sine and cosine signals synchronized with the grid voltage. These signals are called unit vectors [8]. They are used for reference signal generation in the closed-loop control of power converters. The PLLs are also used to monitor disturbances in the grid voltage [4], [9]-[11]. Fig. 1 shows a general schematic of a PLL used in the grid-synchronization of a single-phase power converter. In Fig. 1, V_g is the grid voltage. ω_e, θ_e and V_m are the frequency, phase and amplitude of the grid voltage estimated by the PLL. $sin\theta_e$ and $cos\theta_e$ are unit vectors.

The performance of single-phase PLLs is affected by non-ideal conditions in the grid voltage. These include frequency deviation, harmonic distortion and dc offsets. In the case of three-phase systems, there will be an additional non-ideality of unbalance in the three-phase voltages. It should be noted that under ideal conditions, the grid voltage has a fixed frequency of either 50/60Hz, no harmonic distortion, no dc offsets and no unbalance in the three-phase case.

A. Literature Survey of Existing PLL Structures

Among the various PLLs proposed in the literature, the synchronous reference frame PLL (SRF-PLL) is a popular PLL [8], [12] used in three-phase systems. It is very simple from the design and implementation point of view. The SRF-PLL forms the building block of many PLLs for both three-phase and single-phase applications [13]-[19]. The second-order generalized-integrator (SOGI) based single-phase PLLs [16]-[19] are low-complexity single-phase PLLs that use an embedded SRF-PLL. The basic SOGI-PLL was first introduced in [16]. This PLL has sinusoidal ripple errors in the estimated frequency when the input contains harmonics and dc offsets. These ripple errors can also occur when the input frequency changes from the nominal value [16]. The adaptation of the SOGI parameters is suggested to overcome the problem due to input frequency deviation [16], [17], [19], [20]. However, the adaptive SOGI-PLLs have a higher design and implementation complexity.

The input to single-phase SOGI based PLLs can have a dc offset due to factors such as sensor dc offsets, dc offsets from the analog-to-digital controllers (ADC) and mismatch in the semiconductor device switching in practical power converters. Since the basic SOGI structure cannot eliminate dc offsets, the embedded SRF-PLL has a dc offset in its input. This can result in a serious problem of dc injection to the grid [21]. DC injection to the grid is undesirable [22] and it is to be limited to be less than 0.5% of the rated current of the power converter as per the grid interconnection standard IEEE 1547-2003 [23]. The problem of dc offsets in the basic SOGI-PLL is mitigated in [17], where the design method is based on a heuristic approach. However, the effect of input harmonics is not quantified in that study. A multiple cascaded SOGI based frequency locked loop (FLL) is proposed in [24]. This is proposed for three-phase systems. However, design optimizations considering the response time have not been analyzed. The cascading of SOGI blocks increases the implementation complexity in terms of increased computation time or digital resource utilization. In [25], a modified high-pass based SOGI structure is studied for a robust adaptive PLL. This PLL contains additional non-linear functions when compared to other SOGI based PLLs such as [16]–[19]. In addition, the response to transients is slow in the order of tens of fundamental cycles. The work in [26] estimates the grid frequency and amplitude correctly when the input contains dc offsets. However, the phase estimation is affected by input dc offsets.

B. Present Work

In this paper, a modified SOGI-PLL is presented. The modified SOGI has full dc offset rejection capability and includes a high-pass based filter structure. Hence, this PLL is termed a high-pass generalized integrator based PLL (HGI-PLL). The outputs of the HGI are given as inputs to the embedded SRF-PLL block.

The structure of the HGI-PLL is shown in Fig. 2. This is a fixed parameter or non-adaptive PLL which helps to keep its implementation simple. Its performance is affected by frequency deviations as well as harmonics in the input voltage. These non-ideal conditions of frequency deviations and harmonics result in unit vector harmonic distortions [18]. This is undesirable since the unit vectors are used for reference generation and are expected to have a minimal harmonic distortion. Hence, the HGI-PLL must be designed so that the unit vector distortion is minimal for the non-ideal grid conditions of frequency deviation and harmonic distortion. Another desirable performance parameter is a fast settling time. The HGI-PLL design must consider the factors of a minimal unit vector distortion and fast response time for given worst case non-idealities in the grid voltage.

Novel systematic designs are derived for the HGI-PLL in this paper. For a given worst case frequency deviation in the input, a design approach is proposed which results in the fastest response for a given constraint on the unit vector THD. For example, for the worst case setting of a ±8% frequency

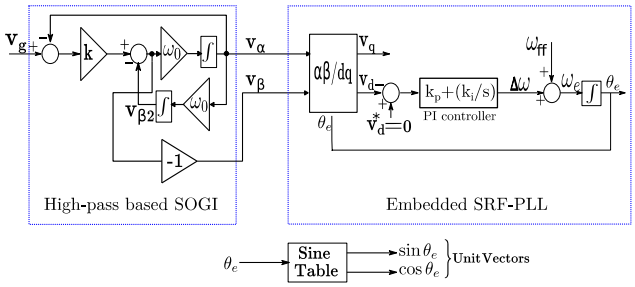


Fig. 2. Structure of a high-pass generalized integrator based PLL (HGI-PLL).

deviation, the HGI-PLL is designed to have the fastest response while limiting the unit vector THD to be less than 1%. This design is evolved into a design procedure considering two constraints, the worst case frequency deviations and harmonic distortions in the input. The worst-case harmonic THD for the input is considered to be 5%. This design achieves the fastest response for the HGI-PLL while limiting the unit vector THD to be within 1% for the given worst-case input conditions.

A HGI-PLL with the proposed designs achieves very good transient and steady-state performance. The practical settling time is shown to be less than 30ms. This PLL has the least resource utilization in terms of digital implementation among the SOGI based PLLs with dc cancelling capability. The performance of this PLL has been compared with analysis and simulation and has been validated by experimental results for various steady-state and transient operating conditions.

II. Structure and Design Considerations of the HGI-PLL

A. Structure

The HGI-PLL produces two quadrature signals v_α and v_β from the input sensed grid voltage v_g. The HGI is a modified SOGI filter structure which generates v_α and v_β. The transfer functions realized by the HGI are as follows:

$$G_{\alpha,h}(s) = \frac{v_\alpha}{v_g} = \frac{ks\omega_0}{s^2+ks\omega_0+\omega_0^2} \quad (1)$$

$$G_{\beta,h}(s) = \frac{v_\beta}{v_g} = -\frac{ks^2}{s^2+ks\omega_0+\omega_0^2} \quad (2)$$

It can be verified that the transfer functions in (1) and (2) have zero gain at dc. When the input voltage is sinusoidal with a frequency of ω_0, it can be seen that v_α and v_β are balanced quadrature signals. This is evident from the bode plots of the two transfer functions in Fig. 3.

As can be seen from Fig. 3, the transfer function in (2) is a high-pass filter. In the basic SOGI-PLL [16], the transfer function to generate v_β is a low-pass filter. Hence, it does not block any of the dc offset in the input voltage. As a result, the embedded SRF-PLL has dc offsets in its input which in turn lead to dc offsets in the PLL unit vectors [21]. In the HGI PLL, this is mitigated by making use of a dc blocking high-pass filter as shown in Fig. 2.

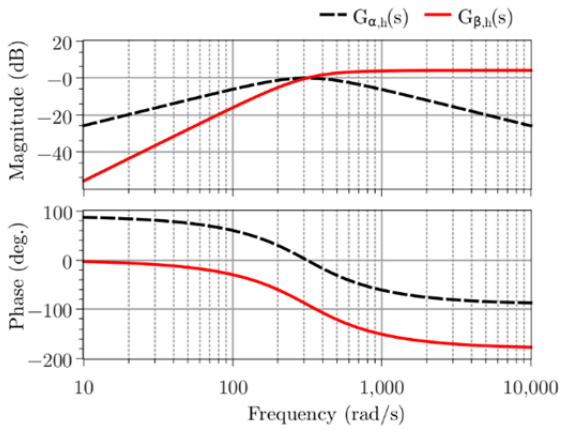


Fig. 3. Bode plot of the transfer functions of the HGI-PLL, when $k = 1.6$.

B. Design Considerations

The HGI-PLL has three design parameters. These parameters are the gain k in the HGI transfer functions, and k_p and k_i of the PI controller transfer function as shown in Fig. 2. In adaptive SOGI based PLLs, the term ω_0, which is used in the transfer functions, is replaced by the estimated frequency ω_e of the PLL [20]. In the present implementation, ω_0 is constant and equal to the nominal grid frequency in rad/s. By keeping ω_0 fixed, the implementation is simplified. The use of fixed parameters helps in arriving at a systematic design method. Hence, the response time can be optimized. The main disadvantage of fixed parameter SOGI based PLLs is the fact that frequency deviations in the input voltage cause unequal amplitudes in v_α and v_β. This is also clear from Fig. 3. Unequal amplitudes result in the application of a negative sequence component to the embedded SRF-PLL [18]. This results in a double harmonic ripple in the estimated frequency [12]. This in turn results in harmonic distortion in the unit vectors [8]. Harmonic distortion in the unit vectors is highly undesirable because the current references generated using them also become distorted. Since the current controllers normally used have low-pass filtering characteristics with a high bandwidth [27], the resulting grid current becomes distorted. Grid interconnection standards such as IEEE 1547-2003 [23] have defined limits on harmonic injection to the grid. The PLL design should ensure that these limits are not exceeded. This can be achieved by carefully selecting the bandwidth of the embedded SRF-PLL. The lower the bandwidth, the better the harmonic attenuation for the unit vectors when the input has frequency deviations [18]. The response time of the embedded SRF-PLL is inversely related to its bandwidth. The relation between the settling time $t_{s,srf}$ and its bandwidth ω_{bw} in rad/s can be approximated as [21]:

$$t_{s,srf} = \frac{4}{\omega_{bw}} \quad (3)$$

There is a tradeoff between the response time and the harmonic attenuation. Hence, it is important to arrive at a design bandwidth of the embedded SRF-PLL such that the

response time is fastest for a given constraint on the unit vector harmonic distortion or THD. This approach of the PLL parameter design follows from the basic SOGI-PLL in [18].

When the grid voltage has a transient amplitude or phase jumps, the filters used in the HGI take a known amount of time to settle. The transients in the HGI output affect the inputs v_α and v_β to the embedded SRF-PLL. This results in temporary errors in the estimation of the frequency and phase till the HGI outputs settle to correct values. Hence, the overall settling time is also dependent on the design parameter k of the HGI block. It must be designed to have a fast response during transient changes in the grid voltage.

Let the overall settling time due to the HGI transfer functions be defined as:

$$t_{s,hgi} = \max\left(t_{s\alpha}(k), t_{s\beta}(k)\right) \quad (4)$$

In (4), $t_{s\alpha}(k)$ and $t_{s\beta}(k)$ are the settling times of the transfer functions in (1) and (2) for a step change. These settling time values depend on the parameter k.

Since the HGI-PLL has a cascade of the HGI block and the embedded SRF-PLL block, the worst-case additive settling time is given by the sum of the settling times of the HGI blocks and the embedded SRF-PLL. This worst-case additive settling time is termed as t_{sd}, and is given by:

$$t_{sd} = t_{s,hgi} + t_{s,srf} \quad (5)$$

The grid voltage at the point of common coupling (PCC) normally contains lower order harmonics due to the presence of non-linear loads in the system and a finite grid impedance [28], [29]. The transfer function in (1) has a bandpass configuration centered around the nominal fundamental frequency ω_0. Hence, there is attenuation of harmonics by this transfer function. However, as can be seen from Fig. 3, the transfer function (2) has a high-pass characteristic. Hence, it cannot attenuate any of the harmonics in the input. The embedded SRF-PLL has a low-pass characteristic and can attenuate harmonics. Hence, to sufficiently attenuate the input harmonics, both the k and PI controller parameters of the embedded SRFPLL have to be selected carefully as proposed in Section III of this paper. This also influences the overall settling time, which is to be minimized as explained in Section III.

III. Design of the HGI-PLL

The design of the HGI-PLL discussed in the following subsections III-A is referred to as minimum t_{sd} design (MTSD design). Note that t_{sd} is the additive settling time defined in (5), which is the sum of the settling time of the HGI block and the settling time of the embedded SRF-PLL block. This design selects the values of k and the bandwidth considering only the expected range of the frequency deviations. The objective of this design is to select PLL parameters that lead to the shortest additive settling time for a specified limit on the unit vector THD considering worst case frequency deviations in the input. This design is analyzed for its harmonic attenuation capability and the resulting limitations are then explained. The MTSD design forms the basis of the complete design method proposed in Section III-B. This is called the harmonic constrained minimum t_{sd} design (HC-MTSD design), because the design parameters are selected to achieve a limit on the unit vector THD when the input contains both frequency deviations and harmonic distortions. In other words, this design optimizes the response time of the HGI-PLL without exceeding the THD limit on the unit vectors when the input voltage contains both frequency deviations and harmonic distortions.

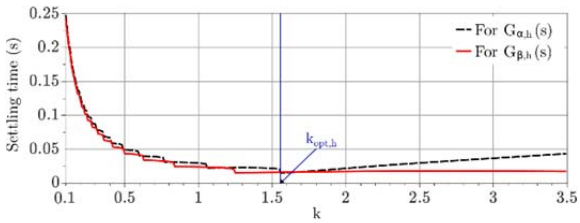


Fig. 4. Variation of the settling time of the HGI transfer functions versus k for the MTSD design.

A. MTSD Design for the HGI-PLL

1) Selection of the Parameter k *for MTSD Design:* The parameter k is selected so that the transfer functions of the HGI-PLL give the fastest settling time. The step response settling time of the transfer functions (1) and (2) as a function of k is determined using a simulation. The variation of k with a 2% step response settling time [30] for the HGI-PLL is shown in Fig. 4. As can be observed, there is a value of k that gives the fastest response, which corresponds to the minimum settling time of the SOGI block in Fig. 2.

From Fig. 4, the optimal value of k is determined to be:

$$k_{opt,h} = 1.56 \quad (6)$$

For this value of $k_{opt,h}$, the settling times for v_α and v_β are 14.91ms and 15.97ms for a 50Hz system. Hence, the combined worst-case settling time ($t_{s,hgi}$) is the maximum of the two settling times, that is:

$$t_{s,hgi} = 15.97ms \approx 16ms \quad (7)$$

Thus, the worst case settling time of 16ms is less than one fundamental cycle.

The selection of $k = k_{opt,h}$ results in the fastest response of the HGI blocks for any changes in the input. The harmonic attenuation is fixed based on the selected value of k. The remaining design parameter is the bandwidth of the embedded SRF-PLL.

2) Selection of the Bandwidth of the Embedded SRF-PLL for the MTSD Design: As explained in Section II-B, the frequency deviations in the input result in a unit vector

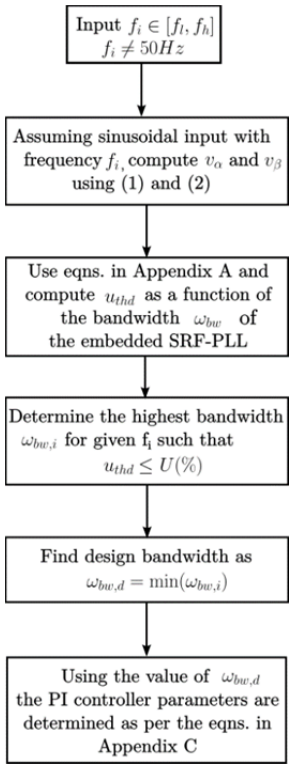


Fig. 5. Flowchart to determine the design bandwidth of the embedded SRF-PLL for different levels of frequency deviations in the input.

distortion. To minimize the unit vector THD, the bandwidth of the SRF-PLL should be adjusted to attenuate the resulting ripple in v_d and the estimated frequency. Let the limit on the unit vector THD be U = 1%. Hence, for a given frequency deviation of Δf, the SRF-PLL bandwidth must be chosen to so that the unit vector THD is $u_{THD} \leq U$ (%).

The analytical expressions derived in [8] are used to determine the unit vector THD as a function of the bandwidth of the embedded SRF-PLL for any frequency deviations in the input. The relevant expressions derived in [8] are included in Appendix A for quick reference. The procedure to determine the design bandwidth is given in the flowchart in Fig. 5. The frequency range is swept from $f_i = [f_l, f_h]$. For a frequency deviation of Δf = ±8%, the frequency is swept between f_l = 46Hz and f_u = 54Hz in a 50Hz system. A step size of 2Hz has been used to sweep this range.

This method is illustrated in Fig. 6. Consider the input frequency to be 46*Hz*. The equations (21)–(23) in Appendix A are used, and the unit vector THD versus the bandwidth are plotted in Fig. 6. The highest bandwidth is chosen for this case as per the flowchart to give a unit vector THD of at most U = 1%. This corresponds to the design bandwidth of 55*Hz*. Similarly, the bandwidth is determined for the remaining three cases in Fig. 6. It can be observed from Fig. 6 that the bandwidth must be chosen to be 55*Hz* so that the unit vector THD is less than 1% for the entire range of frequency deviations from 46*Hz* to 54*Hz*.

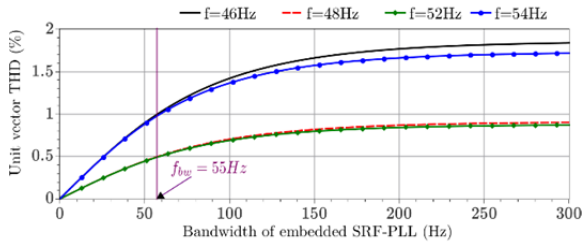


Fig. 6. Variation of the unit vector THD with the bandwidth for various grid frequency values assuming a sinusoidal grid voltage for the HGI-PLL.

Thus, the bandwidth $\omega_{bw,d}$ = 2π55 rad/s will limit the unit vector THD to be less than 1%. This is true even for a frequency deviation of up to ±8% in the input voltage. Once the design bandwidth is known, the PI controller parameters of the embedded SRFPLL can be determined using the design equations given in studies such as [12], [21]. The final expressions (33) and (34) used to compute these PI controller parameters are provided in Appendix C. The settling time of the embedded SRF-PLL for this design bandwidth is given by:

$$t_{s,srf} = \frac{4}{\omega_{bw,d}} = 11.6ms \quad (8)$$

3) Summary of the MTSD Design: The k in the HGI transfer function is selected to achieve the fastest response. The bandwidth of the embedded SRF-PLL is the highest for the given frequency deviation and constraint on the unit vector THD. Hence, for the given constraints, the embedded SRF-PLL also has the fastest response. The net worst-case additive settling time using (7) and (8) is given by:

$$t_{sd} = t_{s,hgi} + t_{s,srf} = 16ms + 11.6ms = 27.6ms \quad (9)$$

Thus, the proposed design results in a worst-case settling time of less than 1.5 fundamental cycles. The actual settling time is less than this value since the transients in the HGI and the embedded SRF-PLL occur simultaneously. This is shown in Section V with experimental results.

4) Effect of Input Harmonics on the MTSD Design: The effect of the input harmonics is quantified analytically for this design since it does not include input harmonic distortion during the design process. A known amount of input THD is considered. The individual harmonics considered are the low order odd harmonics up to the ninth harmonic. The harmonic amplitude is considered to be inversely proportional to its harmonic order. That is:

$$\frac{v_{h,i}}{v_{h,j}} = \frac{j}{i} \quad (10)$$

Hence, the fifth harmonic has an amplitude of 3/5 times the third harmonic, the seventh harmonic is 3/7 times the third harmonic and the ninth harmonic is 3/9 times the third harmonic. Based on this, the individual harmonics are calculated for a given THD.

For each input THD, the resulting harmonics in the outputs of the transfer functions in (1) and (2) are determined analytically. The resulting distorted v_α and v_β are input to the

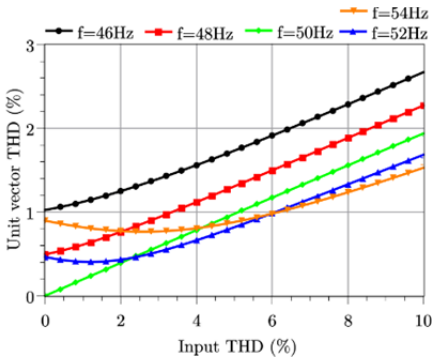


Fig. 7. Variation of the unit vector THD with the input THD for up to a ±8% frequency deviation in the input for the MTSD design of the HGI-PLL.

embedded SRF-PLL. Hence, using the analytical expressions derived in [8], the unit vector THD is determined as a function of the input THD and frequency deviations. The unit vector THD can be evaluated from the phasor sum of the individual unit vector harmonic distortion given by (30)-(32) in Appendix B. The resulting variation between the unit vector THD and the input THD for the MTSD design of the HGI-PLL is given in Fig. 7.

As can be seen from Fig. 7, when the input has a THD of 5%, the unit vector THD is equal to 1.7% when the input has a frequency of 46Hz. Thus, when the input THD is assumed to have a worst-case value of 5% [29], [31], the unit vector THD can exceed the 1% limit. To meet the objective of limiting the unit vector THD when the input contains both frequency deviations and harmonics, an enhanced design procedure is evolved for the HGI-PLL. This is termed as the HC-MTSD design. This design limits the unit vector THD to within a limit of U = 1%, and achieves the fastest additive settling time while considering both frequency deviations and the input THD. This design method is explained in the following subsection.

B. HC-MTSD Design for the HGI-PLL

The objectives of this design can be defined as follows:

$$Minimize\ t_{sd} = g(f_{bw}, k) \tag{11}$$

Such that:

$$u_{thd} \leq 1\% \tag{12}$$

given that the frequency deviation is Δf (%) and the input THD is H (%).

The additive settling time t_{sd} is a function of the HGI-PLL parameters f_{bw} and k. This function is labelled as $g(f_{bw},k)$ in (11). The unit vector THD u_{thd} is affected by both f_{bw} and k. The upper limit on the bandwidth for the solution of (11) is considered to be 55Hz based on the MTSD design. This is due to the fact that from a fundamental frequency deviation point of view, any higher f_{bw} would result in a unit vector THD that is higher than 1%, as indicated in Fig. 6, for up to a ±8% deviation in the grid fundamental frequency. The lower limit is considered to be 20Hz. Theoretically, the lower limit on the bandwidth can be close to zero.

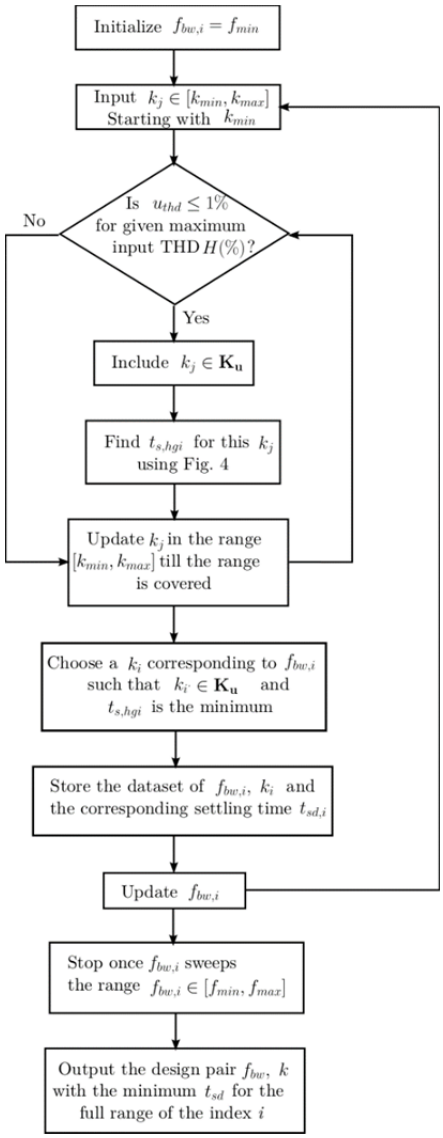


Fig. 8. Flowchart showing the steps in the HC-MTSD design of the HGI-PLL.

The optimum solution for (11), considering the constraint in (12) and the inputs of Δf = ±8% and H = 5% is, determined within the bandwidth range of [f_{min}, f_{max}]. The range of k to be considered is [k_{min}, k_{max}]. These are listed as follows:

$$f_{min} = 20Hz\ and\ f_{max} = 55Hz$$
$$k_{min} = 0.1\ and\ k_{max} = 4 \tag{13}$$

The range of k considers a wide possible design selection range as shown in Fig. 4. This range includes $k_{opt,h}$ for the MTSD design specified in (6).

The procedure for the HC-MTSD design is explained using the flowchart in Fig. 8. This is qualitatively explained as follows. For every bandwidth value in the considered range, the set of k satisfying the unit vector THD so that it is less than 1% is determined. This set is designated as $\boldsymbol{K_u}$ in the flowchart in Fig. 8. In $\boldsymbol{K_u}$, the value of k that gives fastest response time for the HGI is determined. This is done using a procedure similar to the plot in Fig. 4. This value of k is

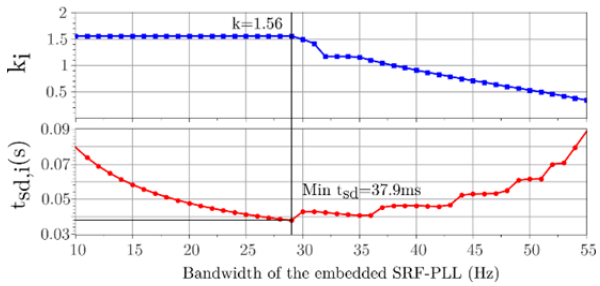


Fig. 9. HC-MTSD design for the HGI-PLL. Variation of k_i with respect to the bandwidth (top trace), and variation of the additive settling time $t_{sd,i}$ with respect to the bandwidth (bottom trace).

selected as the corresponding value to the chosen bandwidth. The additive settling time of the HGI-PLL is computed for this pair of bandwidth and *k*. This is repeated for a large number of bandwidth values in the range specified in (13). For each bandwidth, a corresponding *k* and settling time are determined. The pair with least additive settling time is selected as the design value based on the objective in (11).

The solution to this method is graphically illustrated as follows. The valid solution points contain three components which are $f_{bw,i}$, k_i and the corresponding $t_{sd,i}$. In the top trace in Fig. 9, k_i is plotted versus $f_{bw,i}$. In the bottom trace, $t_{sd,i}$ is plotted versus $f_{bw,i}$. It can be observed that the minimum t_{sd} is obtained for $f_{bw} = 29Hz$ in the bottom trace. The corresponding $k = 1.56$. This is the optimal pair of f_{bw} and k and it gives a settling time of *37.9ms*, which is less than two fundamental cycles in a 50Hz system. The plot in Fig. 9 is for a worst-case input THD of $H = 5\%$ and a frequency deviation of $\Delta f = \pm 8\%$.

The variations of the unit vector THD versus the input THD and the input frequency deviations are shown in Fig. 10 for the HC-MTSD design. Fig. 10 can be compared with Fig. 7. It can be seen that with the HC-MTSD design, the unit vector THD stays within 1% for the worst-case condition of an input THD of up to 5% with a frequency deviation of up to ±8%.

IV. Design Summary

In the proposed design method, the parameter *k* and the bandwidth of the embedded SRF-PLL are selected. These parameters are general and not system specific. This is due to the fact that in the HGI, the transfer functions in (1) and (2) are fixed. Hence, the value of k remains as per the proposed design in any system. Similarly, the SRF-PLL bandwidth is a general parameter. The PI controller parameters, which are calculated using the bandwidth value using (33)-(34), are system specific and their values depend on discretization methods and the sampling frequency. However, the bandwidth value is the same as per the proposed designs. Hence, the overall design summary applies to any general single-phase system. It is given as follows.

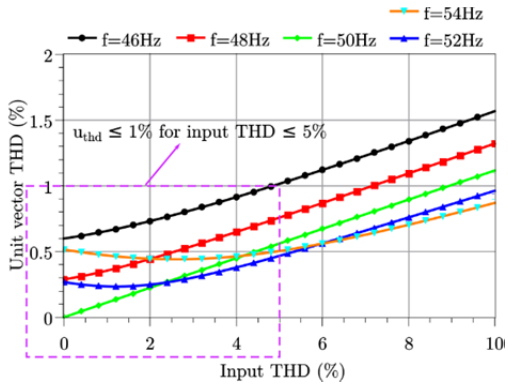


Fig. 10. Variation of the unit vector THD with an input THD of up to a ±8% frequency deviation in the input for the proposed HC-MTSD design.

1) *Minimum t_{sd} design (MTSD design)*: This design selects the HGI-PLL design parameters considering a worst case input frequency deviation and a limit on the unit vector THD. For these conditions, this design obtains the fastest response. The design parameters determined for a frequency deviation of ±8% and a unit vector THD limit of 1% are:

$$k = 1.56, f_{bw} = 55Hz, t_{sd} = 27.6ms \quad (14)$$

2) *Harmonic constrained Minimum t_{sd} design (HC-MTSD design)*: This design is an extension of the MTSD design. It selects the HGI-PLL design parameters considering a worst case input frequency deviation, a worst case input THD and a constraint on the unit vector THD. For these conditions, this design obtains the fastest response. The design parameters determined for a frequency deviation of ±8%, an input voltage THD of 5% with the constraint of (10) and a unit vector THD limit of 1% are:

$$k = 1.56, f_{bw} = 29Hz, t_{sd} = 37.9ms \quad (15)$$

Note that the proposed HC-MTSD design approach uses a worst-case maximum harmonic distortion in the grid voltage. There is no online computation of either the THD of the grid voltage or the THD of v_α and v_β. The PLL design parameters are computed offline and implemented in a digital controller for the worst-case condition. Hence, when the grid voltage conditions are closer to the ideal-case, the performance of the HGI-PLL improves further.

The performance of the HGI-PLL is compared with the popular SOGI based single-phase PLLs. The comparison is given in Table I. The resource utilization mentioned in Table I is computed using a forward Euler implementation. Trapezoidal or other discretization methods can also be used [16]. However, the Euler method gives the least resources which is important when the implementation is done using a low-end digital controller. It can be seen from Table I that the HGI-PLL uses considerably less resources when compared to other dc cancelling SOGI based PLLs. It also has systematic design methods for the selection of the PLL parameters.

TABLE I
COMPARISON OF THE HGI-PLL WITH THE POPULAR SOGI BASED SINGLE-PHASE PLLS

PLL Type	DC cancelling capability	Design Parameters	Design Method	Resource Utilization* (Multiplications - M and additions - A)
Basic fixed SOGI-PLL [18]	No	2	Systematic	3M, 4A
Basic adaptive SOGI-PLL [16], [19]	No	2	Heuristic	5M, 4A
Modified adaptive SOGI-PLL [17]	Yes	3	Heuristic	7M, 8A
HGI-PLL (Present work)	Yes	2	Systematic	4M, 6A

*The resource utilization in the embedded SRF-PLL is 7M, 6A for all the SOGI based PLLs.

V. EXPERIMENTAL RESULTS

The simulation and experimental results in this section validate the steady-state and transient performance of the HGI-PLL for the following cases.

1. Validating the offset rejection performance.
2. Validating the transient response.
3. Validating the unit vector THD when the input contains a THD of 5% along with a −8% frequency deviation.

The experimental implementation of the HGI-PLL is done on an Altera Cyclone EP1C12Q240C8 FPGA controller board using a fixed point 16 bit arithmetic. In any FPGA, the PLL is realized using the digital logic elements within the FPGA. Since the individual blocks such as HGI, the *αβ/dq* conversion, and the PLL loop are implemented in parallel in the FPGA, the execution time is very small. It can be in the order of a few clock cycles. In the experimental system, the FPGA uses a clock of 50 MHz. Hence, the execution time is in the order of a few tens of nanoseconds.

Fig. 11(a) shows the effect of the presence of a 10% dc offset in the input voltage of the basic SOGI-PLL [16], [18]. A large amount dc offset is considered to clearly show the presence of the dc offset in the input voltage. As can be observed from Fig. 11(a), the estimated frequency f_e contains a ripple error at the fundamental frequency. This results in the presence of dc offsets and even harmonics in the unit vector.

The performance of the HGI-PLL for the same 10% input dc offset condition is shown in Fig. 11(b). The estimated frequency is a purely dc quantity for the HGI-PLL indicating that the input dc has been rejected by the modified SOGI structure in the HGI-PLL.

The transient response of the HGI-PLL is verified by introducing a step-phase-change in the input voltage. Fig. 12(a) shows the result for the MTSD design of the HGI-PLL. Fig. 12(b) shows the result for the HC-MTSD design of the HGI-PLL. As can be observed, the HC-MTSD design has a slightly slower response. The settling time for the MTSD design is observed to be 20ms whereas for the HC-MTSD design it is observed to be about 30ms. As expected, these values are lower than the respective worst case

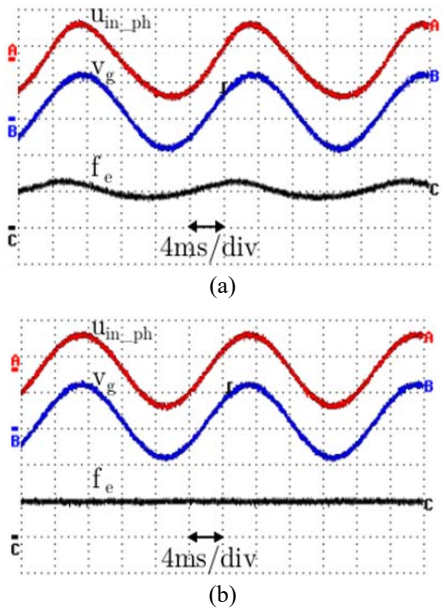


Fig. 11. Effect of a 10% dc offset on: (a) the basic SOGI-PLL; (b) the HGI-PLL. Ch. A = the in-phase unit vector u_{in_ph} (1pu/div); Ch. B = the input voltage v_g (5V/div); Ch. C = the estimated frequency f_e(50Hz/div).

additive-settling-times (t_{sd}), which were 27.6ms and 37.9ms, respectively.

The effect of a frequency jump from the nominal 50 Hz to 54 Hz, on the performance of the HGI-PLL is shown in Fig. 13(a), for the MTSD case. It can be observed that the frequency is tracked within 20ms. The corresponding result for the HC-MTSD case is shown in Fig. 13(b). It can be seen that the HC-MTSD gives practically the same result, with a relatively higher settling time, for the frequency jump. When the frequency increases to 54 Hz, it can be observed from the figure that there is a second harmonic ripple in the estimated frequency. This is as per the theoretical expectation and the unit vector THD is maintained to be within 1% by the proposed designs.

The effect of harmonics and frequency deviations in the input voltage is verified next. The input voltage has a fundamental frequency of 46Hz which corresponds to a −8% frequency deviation. The input voltage also has a 5% THD.

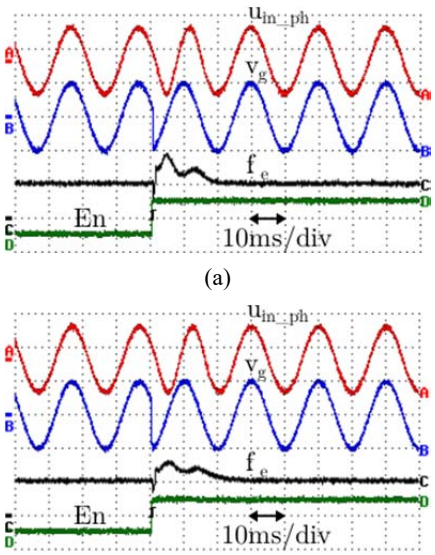


Fig. 12. Transient response of the HGI-PLL to step-phase-changes in the input in: (a) the MTSD design; (b) HC-MTSD design. Ch. A = the in-phase unit vector u_{in_ph} (1pu/div); Ch. B = the input voltage v_g (5V/div); Ch. C = the estimated frequency f_e (50Hz/div); Ch. D = the enable (En) signal.

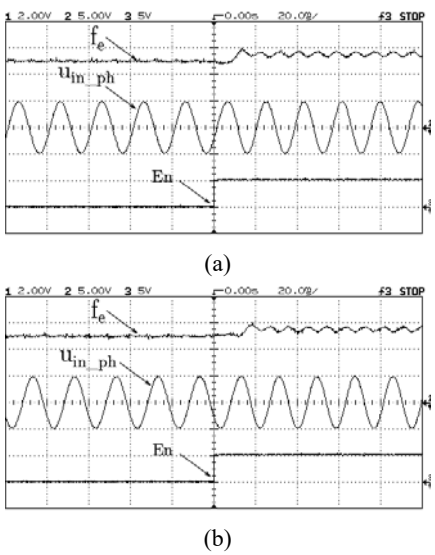


Fig. 13. Transient response of the HGI-PLL to a step frequency change in the input: (a) the MTSD design; (b) the HC-MTSD design. Ch. 1 = the estimated frequency f_e(20Hz/div); Ch. 2 = the in-phase unit vector u_{in_ph} (1pu/div); Ch. 3 = the enable (En) signal.

The performance of the HGI-PLL with the MTSD design for this input voltage is shown in Fig. 14(a). The response of the HGI-PLL for the same input condition with the HC-MTSD design is shown in Fig. 14(b).

The time domain waveforms of the in-phase unit vector do not show a significant difference in terms of distortion. However, the spectrum of the unit vectors was obtained from

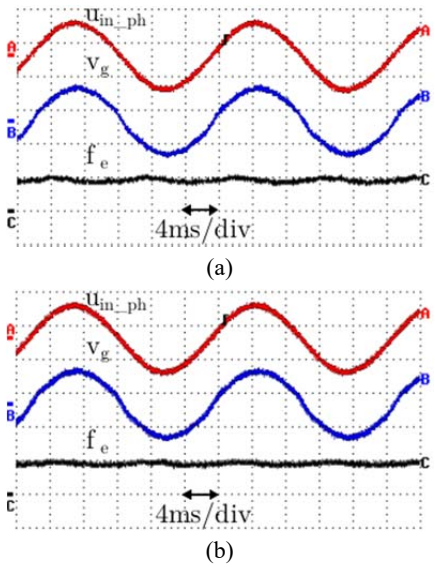


Fig. 14. Effect of a −8% frequency deviation in the input voltage with a 5% THD on the HGI-PLL for: (a) the MTSD design; (b) the HC-MTSD design. Ch. A = the in-phase unit vector u_{in_ph} (1pu/div); Ch. B = the input voltage v_g (5V/div); Ch. C = the estimated frequency f_e (50Hz/div).

TABLE II

COMPARISON OF THE ANALYTICAL, SIMULATION AND EXPERIMENTALLY OBSERVED UNIT VECTOR THD OF THE HGI-PLL FOR THE MTSD DESIGN AND THE HC-MTSD DESIGN

*Input THD is 5% with a Fundamental Frequency Variation of Up to ±8%

MTSD design

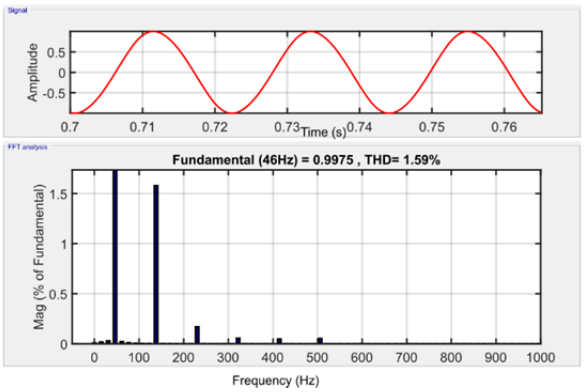
Fundamental Frequency (Hz)	Unit vector THD (%)		
	Analytical	Simulation	Experimental
46	1.7	1.6	1.5
48	1.3	1.3	1.3
50	1.0	1.0	1.0
52	0.8	0.8	0.8
54	0.9	0.7	0.7

HC-MTSD design

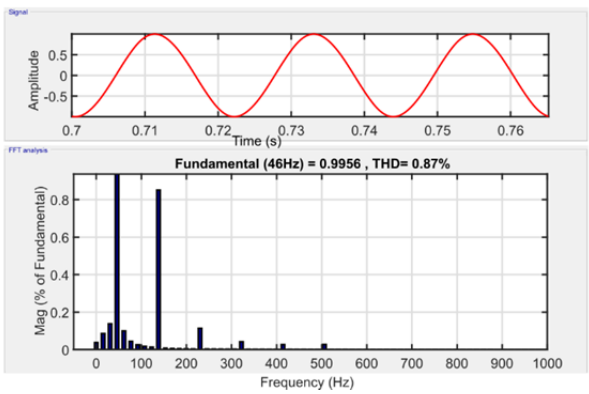
Fundamental Frequency (Hz)	Unit vector THD (%)		
	Analytical	Simulation	Experimental
46	1.0	0.9	0.9
48	0.8	0.7	0.8
50	0.6	0.6	0.5
52	0.5	0.4	0.4
54	0.5	0.4	0.4

experimental waveforms. The unit vector THD corresponding to Fig. 14(a) and (b) is compared with the unit vector THD from the analytical results and simulation result in Table II(a) and (b).

Fig. 15(a) shows simulation result when the input frequency is 46 Hz for the MTSD design. The corresponding result for the HC-MTSD design is shown in Fig. 15(b). Similarly, simulation result for an extreme frequency deviation of 54 Hz is shown in Fig. 16. For frequency deviations between 46 Hz to 54 Hz in steps of 2 Hz,

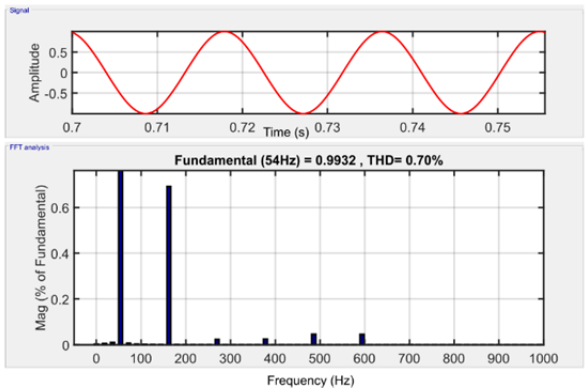


(a)

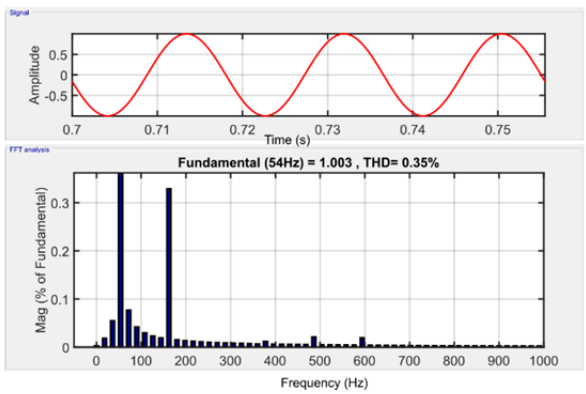


(b)

Fig. 15. Simulation result showing the unit vector and its spectrum when the input voltage frequency is 46 Hz with a THD of 5%: (a) the MTSD design; (b) the HC-MTSD design. The resulting unit vector THD is mentioned in Table II.



(a)



(b)

Fig. 16. Simulation results showing the unit vector and its spectrum when the input voltage frequency is 54 Hz with a THD of 5%: (a) the MTSD design; (b) the HC-MTSD design. The resulting unit vector THD is mentioned in Table II.

simulations are performed and the obtained results are summarized in Table II. It can be seen from Table II that the analytical, simulation, and experimental results are in close agreement. This validates the analysis and effectiveness of the proposed design when the sensed grid voltage contains a frequency deviation and harmonic distortion. The HC-MTSD design gives better results when the input contains both harmonics and frequency deviation, as shown in Table II.

VI. Conclusions

In this paper, systematic designs are proposed for a high-pass generalized integrator based PLL (HGI-PLL) for single-phase grid-connected power converter applications. This is a modified fixed-parameter SOGI-PLL with input dc offset rejection capability. This property of dc rejection is important since the basic SOGI-PLLs do not have this capability which can result in dc injection to the grid when the input contains dc offsets. The performance of the HGI-PLL is affected by the non-ideal input conditions of frequency deviations as well as harmonic distortions. These non-idealities result in harmonic distortion of the PLL unit vectors. This is undesirable since the unit vectors are used for reference generation in the closed-loop control of grid-connected power converters.

Systematic design methods are proposed in this paper for the HGI-PLL. Firstly, the HGI-PLL parameters are selected considering a worst-case input frequency deviation. For a constraint on the unit vector THD of 1%, this design achieves the fastest response of the HGI-PLLs. This method can exceed the limit on the unit vector THD when the input contains considerable harmonic distortion. Hence, to mitigate this problem, this design is developed to include the non-ideality of input voltage harmonic distortion. This is an extension of the first design and it selects the HGI-PLL parameters considering the worst case frequency deviations as well as THD in the input voltage. The design parameters are selected so that for the given worst case conditions, the HGI-PLL has the fastest response without exceeding the unit vector THD limit of 1%.

The proposed designs have been experimentally validated and are found to agree with the analysis. The HGI-PLL uses considerably less resources while being able to provide good steady-state and transient performances. The proposed design method can be extended to arbitrary single-phase systems. The HGI-PLL with the proposed designs is a suitable PLL scheme when low-end digital controllers are used in the control of grid-connected power converter systems, since it

has a low implementation complexity.

APPENDIX A
QUANTIFYING THE EFFECTS OF FREQUENCY DEVIATION ON THE UNIT VECTOR HARMONIC DISTORTION

When there is a frequency deviation in the input, the amplitudes of v_α and v_β become unequal as can be seen from the Bode plot in Fig. 3. Let these voltages be defined as follows:

$$v_\alpha = V_1 \sin(\omega t + \varphi_1) \quad (16)$$

$$v_\beta = V_2 \sin(\omega t + \varphi_2) \quad (17)$$

From the Bode plot in Fig. 3, it can be deduced that $V_1 \neq V_2$ in (16) and (17). Similarly, $\varphi_1 \neq \varphi_2$ and $\varphi_1 - \varphi_2 = \pi/2$. These parameters are known from the transfer functions of the HGI for any given input frequency.

Due to their unequal amplitudes, the two-phase equivalent voltages v_α and v_β contain an unbalance and hence a negative sequence component. This causes the well-known problem of double fundamental frequency ripples in v_d, v_q and the estimated frequency ω_e. Since the estimated phase θ_e is an integral of ω_e, it has the following form:

$$\theta_e = \omega_e t + f \quad (18)$$

In (18), f is a second harmonic ripple error. This is defined below in (19). The aim is to determine the parameters a and φ in the equation below:

$$f = \text{asin}(2\omega t + \varphi) \quad (19)$$

In (19), ω is the fundamental frequency whose nominal value is $\omega = \omega_0 = 2\pi 50$ rad/s. It is assumed that the fundamental frequency can vary by up to ±8% in this paper. For a given f, it is shown in [8] that the unit vector has a third harmonic amplitude equal to:

$$u_3 = \frac{a}{2} \quad (20)$$

The detailed derivation steps to determine a and φ are provided in [8]. Only the final expressions are reproduced here:

$$a = \frac{m\left[\left(\frac{V_1}{2}\right)\cos(\varphi_1 + x) + \left(\frac{V_2}{2}\right)\sin(\varphi_2 + x)\right]}{cos\varphi - mcos(\varphi + x)[-\frac{cos\varphi_1 V_1}{2} + \frac{sin\varphi_2 V_2}{2}]}$$

$$\varphi = \arctan\left[\frac{\alpha + \beta\vartheta}{\alpha\vartheta - \beta}\right] - x \quad (21)$$

Where:

$$\alpha = cosx + \left[\left(\frac{V_1}{2}\right)cos\varphi_1 - \left(\frac{V_2}{2}\right)sin\varphi_2\right]m$$

$$\beta = \sin(x)$$

$$\vartheta = \frac{\left(\frac{V_1}{2}\right)\cos(\varphi_1 + x) + \left(\frac{V_2}{2}\right)\sin(\varphi_2 + x)}{\left(\frac{V_1}{2}\right)\sin(\varphi_1 + x) - \left(\frac{V_2}{2}\right)\cos(\varphi_2 + x)} \quad (22)$$

In (21) and (22), m and x are the overall magnitude gain and phase shift at the second harmonic frequency given by the summer, PI controller and integrator in the embedded SRFPLL in Fig. 2. They are expressed as follows:

$$m = \left| -\frac{\left(k_p + \frac{k_i}{s}\right)1}{s} \right|_{s=j2\omega}$$

$$x = angle(m) \quad (23)$$

Thus, for a given frequency deviation, it is possible to determine the output of the HGI v_α and v_β. Then the above equations can be used to determine a, which is equal to twice the amplitude of the third harmonic in the unit vector [8].

APPENDIX B
QUANTIFYING THE EFFECTS OF GRID VOLTAGE HARMONICS ON THE UNIT VECTOR HARMONIC DISTORTION

Assume that the sensed grid voltage contains a harmonic of the order h. Depending on the transfer functions of the HGI, the voltages v_α and v_β also contain a harmonic of the order h, whose magnitude and phase can be calculated. Let these harmonic voltages be defined in phasor form as follows:

$$\boldsymbol{v_{h\alpha}} = V_{h\alpha}\angle\varphi_h$$

$$\boldsymbol{v_{h\beta}} = V_{h\beta}\angle\psi_h \quad (24)$$

The phasors in (24) rotate at a harmonic frequency that is h times the fundamental. These harmonic voltages can be split into positive and negative sequence voltages in two-phase systems as follows:

$$\boldsymbol{v_{h\alpha p}} = \frac{\boldsymbol{v_{h\alpha}} + j\boldsymbol{v_{h\beta}}}{2}$$

$$\boldsymbol{v_{h\alpha n}} = \frac{v_{h\alpha} - jv_{h\beta}}{2} \quad (25)$$

In (25), the voltages $\boldsymbol{v_{h\alpha p}}$ and $\boldsymbol{v_{h\alpha n}}$ are the α axis positive and negative sequence voltages. The corresponding β axis voltages are given by:

$$\boldsymbol{v_{h\beta p}} = -j\boldsymbol{v_{h\alpha p}}$$

$$\boldsymbol{v_{h\beta n}} = j\boldsymbol{v_{h\alpha n}} \quad (26)$$

The expressions in (26) are obtained based on the fact that the β axis voltage lags the α axis voltage by 90° in the positive sequence while it leads by 90° in the negative sequence. By adding up the positive and negative sequence voltages, the original voltages in (24) can be obtained.

In [8], the unit vector harmonic distortion is determined analytically when the input contains a harmonic of any given sequence. A harmonic with order h occurring as a positive sequence gives rise to $(h-2)$ and h order harmonics in the unit vectors. Similarly, a harmonic with order h occurring as a negative sequence gives rise to h and $(h+2)$ order harmonics in the unit vectors.

The expressions in [8] are reproduced here for computing the distortion due to positive sequence harmonics. Let these voltages be:

$$v_{h\alpha p} = V_h \sin(h\omega t + \gamma)$$

$$v_{h\beta p} = -V_h \cos(h\omega t + \gamma) \quad (27)$$

The expressions in (27) are general time domain expressions of the corresponding phasors specified in (25) and (26). The sensed grid voltage has a positive sequence fundamental voltage given in the following general form:

$$v_{1+(\alpha)} = V_{1+}\sin(\omega t + \delta)$$

$$v_{1+(\beta)} = -V_{1+}\cos(\omega t + \delta) \quad (28)$$

For the input conditions, as in (28) and (27), the analytical

expressions are derived in [8] to compute the *(h − 2)* and *h* order harmonics in the unit vector. The sine unit vector has the following form for these harmonics:

$$u_{h-2} = a_h \sin((h-2)\omega t + \varphi_h)$$
$$u_h = a_h \sin(h\omega t + \varphi_h) \quad (29)$$

The final expressions for the amplitude and phase in (29) are as follows:

$$\varphi_h = \arctan\left[\frac{\alpha_h - \beta_h \cot(x_{h-1}+\gamma)}{\beta_h + \alpha_h \cot(x_{h-1}+\gamma)}\right]$$
$$a_h = \frac{0.5 V_h m_{h-1} \cos(x_{h-1}+\gamma)}{\cos(\varphi_h) + m_{h-1} V_{1+} \cos(\delta)\cos(\varphi_h + x_{h-1})} \quad (30)$$

Where:

$$\alpha_h = 1 + m_{h-1} V_{1+} \cos(\delta)\cos(x_{h-1})$$
$$\beta_h = m_{h-1} V_{1+} \cos(\delta)\sin(x_{h-1}) \quad (31)$$

In (30) and (31), m_{h-1} and x_{h-1} are the overall magnitude gain and phase shift at the second harmonic frequency given by the summer, PI controller and integrator in the embedded SRF-PLL in Fig. 2. They are expressed as follows:

$$m_{h-1} = \left| -\frac{\left(k_p + \frac{k_i}{s}\right)1}{s} \right|_{s=j(h-1)\omega}$$
$$x_{h-1} = angle(m_{h-1}) \quad (32)$$

For the negative sequence harmonics, the same expressions (30)–(32) can be used by replacing *h − 1* with *h + 1*. The overall THD is determined by performing a phasor sum of the harmonics in the unit vector that appear due to all of the positive sequence and negative sequence harmonics in the input voltage to the embedded SRF-PLL.

APPENDIX C
EXPRESSIONS FOR THE PI CONTROLLER PARAMETERS

For any given design bandwidth of the embedded SRFPLL (ω_{bw}), the PI controller parameters k_p and k_i can be uniquely determined. The corresponding equations are as follows [12], [21]:

$$k_p = \frac{\omega_{bw}}{V_m} \quad (33)$$
$$k_i = k_p T_s \omega_{bw}^2 \quad (34)$$

In (34), the parameter T_s is the sampling time used in the digital implementation of the SRF-PLL. In (33), V_m is the nominal sensed grid voltage peak.

ACKNOWLEDGMENT

This work was supported by CPRI, Ministry of Power, Government of India, under the project "Power conversion, control, and protection technologies for microgrid."

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