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Analysis and Design Considerations for a High Power Buck Derived LED Driver with Extended Output Voltage and Low Total Harmonic Distortion

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Abstract

In order to reduce the cost, improve the efficiency and simplify the complicated control of existing isolated LED drivers, an improved boundary conduction mode (BCM) Buck ac-dc light emitting diode (LED) driver with extended output voltage and low total harmonic distortion is proposed. With a coupled inductor winding and a stacked output, its output voltage can be elevated to a much higher value when compared to that of the conventional Buck ac-dc converter, without sacrificing the input harmonics and power factor. Therefore, the proposed Buck LED driver can meet the IEC61000-3-2 (Class C) limitation and has a low THD. The operating principle of the topology and the design methodology of the ac-dc LED driver are presented. A 150 W ac-dc prototype was built in the laboratory and it shows that the input current harmonics meet the lighting standard. In addition, the THD is less than 16% at a typical ac input. The peak efficiency is higher than 96.5% at a full load and a normal input.

Key words: AC-DC, BCM Buck, LED driver, Low THD, Non-isolated

I. INTRODUCTION

With the significant luminous efficiency improvement of the High Brightness Light Emitting Diode (HB-LED), it has been regarded as the next generation of "green" light source due to its virtues of high efficacy, ultra-long lifetime, no mercury inside and flexible control [1]. In general lighting applications, an ac-dc converter is needed to drive a LED lamp. To prevent interference from the input current harmonics of the ac-dc converter on grids, many countries and regions have imposed restrictions on the input power factor and current harmonics for different power level lighting systems, such as the Energy Star [2], IEC61000-3-2 [3], etc. For high power ac-dc LED drivers, the harmonic content of the line current must comply with the IEC-61000-3-2 Class C standard.

Many non-isolated dc-dc topologies can be used as ac-dc LED drivers, such as conventional boundary conduction mode (BCM) Boost, Buck [4], [5], Buck-boost, Cuk, Sepic and Zeta topologies and their derivatives. Boost converters can achieve a high power factor (PF) and a low total harmonics distortion (THD). However, they output a relatively high voltage, especially at 220Vac and higher inputs. Therefore, the minimum voltage range of a LED strings is limited for non-isolated LED drivers. Buck converters can achieve a relatively high efficiency, particularly at a low input voltage due to the large duty cycle and low rms current. However, they make it difficult to meet the harmonics limitations of lighting applications when their output voltage is higher than 150V. Sepic [7], [8], Cuk [6] and Zeta[9] converters can achieve a low THD, a high PF, and a flexible output voltage. However, the voltage stresses of the switches are pretty high, which results in a high conduction loss and a low efficiency especially in high power LED lighting applications. Non-isolated two-stage solutions can also achieve a high PF, a low THD and a flexible output voltage. They also have good performance for LED driving applications. However, they are not competitive when compared to isolated two-stage solutions in terms of cost and performance. Hence, integrated two-stage converters [10]-[14] are more attractive because their component count is reduced. In [10], a double-buck single switch converter, which integrates a power factor correction (PFC) cell and a dc-dc cell, was presented. Its power factor is always kept constant even when the line and load-conditions vary and its input current can meet the harmonics limitations of IEC21000-3-2 (Class C).

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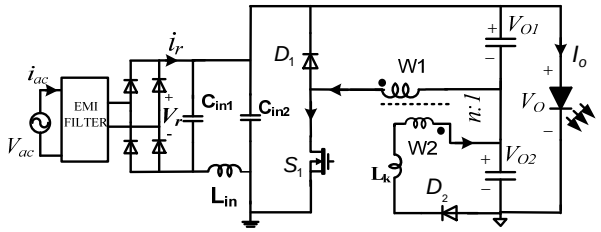


Fig. 1. Improved Buck converter with additionally coupled inductor winding and stacked outputs [23].

This converter is suitable for low-voltage low-power applications. The authors of [11] presented a single switch ac-dc topology integrating Buck and Buck-boost converters, which eliminates the input line current idle time. It can achieve a high PF and low harmonics. In [12], [13] two integrated double-Buck ac-dc converters with a single switch were discussed, which integrate the PFC cell and the dc-dc cell. The integrated topology is still complicated, which may result in a higher cost and a lower efficiency. An integrated Buck PFC converter with two switches and an auxiliary network for achieving a high PF, a low THD and high output voltages was presented in [15], [16]. However, two switches and some other components are needed to compensate the idle time of the conventional Buck ac-dc converter, which leads to an increased cost. With improved control strategies [17]-[21] for Buck ac-dc converters, the THD and PF can be improved. However, it is still difficult for a high output voltage LED lamp to match the harmonics and THD limitations of lighting applications.

A high power Buck derived ac-dc LED driver with extended output voltage and low total harmonic distortion has been presented in Fig. 1. Though, a conventional Buck converter with a coupled winding in the inductor can build the second independent output, namely a flybuck converter [22]. When the two outputs are stacked into one output, it brings largely different operating principles when compared to the flybuck converter, especially for ac-dc conversions [23] and [25]. The rectifier output V_{O2} of the coupled winding is stacked onto the Buck's first output V_{O1}. Therefore, the total output voltage is elevated when compared to the conventional Buck PFC converter without sacrificing the harmonics and PF. With respect to the above mentioned non-isolated topologies mentioned above, the proposed converter has advantages in terms of more adaptive output, lower cost, higher efficiency and simpler control. The steady state operating principle has been briefly presented in [23]. This paper emphasizes the detailed operating principle in the ac-dc conversion and the design methodology for LED driving applications.

II. Operating Principle of the Improved Buck AC-DC Led Driver

A. Steady State Operation of the Proposed Buck Converter

Since the switching frequency is much higher than the line frequency, the input and output capacitors can be assumed to be constant voltage sources V_{in}, V_{O1} and V_{O2} during a switching cycle. In order to simplify the analysis, the ac-dc converter in Fig. 1 can be simplified into a dc-dc converter by neglecting the input rectifier, as shown in Fig. 2. The Buck switch S_1 is connected to the ground of the input. Therefore, it can be easily driven without floating drivers. The coupled inductor can be equalized to a transformer with the magnetizing inductance L_m. The turns ratio is n ($n=n_{W2}:n_{W1}$) and the leakage inductance is equalized into the secondary side L_k, which is shown in Fig. 1. The magnetizing current of L_m is defined as i_{Lm}. In addition, the secondary winding current is i_P. The intrinsic capacitor of the switch is C_S. The parasitic capacitors of the diodes are C_{D1} and C_{D2}, respectively. These capacitors are assumed to be linear devices.

The operation in a switching cycle of the converter in Fig. 2 can be divided into 5 modes according to the key waveforms in Fig. 3. The simplified equivalent circuits for all of the modes are given in Fig. 4.

Mode 1 (t_0-t_1): At t_0, S_1 is on and the magnetizing inductance L_m is charged by the voltage (V_{in}-V_{O1}). Then the primary current i_L increases linearly with a slope of (V_{in}-V_{O1})/L_m. The current i_{S1} in switch S_1 is equal to i_L during this mode. When S_1 turns off at t_1, this mode ends. The equivalent circuit of this mode is shown in Fig. 4(a). The peak current value I_{LM} can be calculated in (1). During this mode, the charging current i_L is calculated in (2).

$$I_{LM} = i_{Lm}(t_1) = \frac{(V_{in}-V_{O1})}{L_m}(t_1 - t_0) \quad (1)$$

$$i_L(t) = \frac{(V_{in}-V_{O1})}{L_m}(t - t_0),\ (t_0 \le t \le t_1) \quad (2)$$

Mode 2 (t_1-t_2): After t_1, the intrinsic capacitor C_S is charged and the intrinsic capacitors C_{D1} and C_{D2} are discharged by the magnetizing current i_{Lm} at the same time. The voltage v_{ds} across S_1 increases linearly, and the voltages across the diodes D_1 and D_2 decrease linearly. The equivalent circuit of this mode is shown in Fig.4(b). The leakage inductance L_k is very small, with a value of less than 5uH. Hence, the resonance between the parasitic capacitors and the leakage inductance L_k can be neglected during this mode. Therefore, the charging (or discharging) currents for the capacitors are almost in proportion to their capacity. The sum of the charging and discharging current values for the three capacitors is I_{Lm}. When v_{ds} is charged to V_{in}, namely the voltages across the diodes D_1 and D_2 decrease to zero, they begin conducting. Then during this mode, the currents i_{S1}, i_P and i_L are calculated in (3), (4) and (5), respectively.

$$i_{S1}(t) = I_{Lm} \cdot \left(\frac{C_S}{C_S+C_{D1}+n^2C_{D2}}\right),\ (t_1 \le t \le t_2) \quad (3)$$

$$i_P(t) = \frac{1}{n} \cdot I_{Lm} \cdot \left(\frac{n^2C_{D2}}{C_S+C_{D1}+n^2C_{D2}}\right), (t_1 \le t \le t_2) \quad (4)$$

$$i_L(t) = I_{Lm} \cdot \left(\frac{C_S+C_{D1}}{C_S+C_{D1}+n^2C_{D2}}\right), (t_1 \le t \le t_2) \quad (5)$$

Mode 3 (t_2-t_3): After the conducting of D_1 and D_2, i_P increases and i_L decreases. The current commutation between

the inductor windings W_1 and W_2 begins. The equivalent circuit of this mode is shown in Fig. 4(c). Since the diodes D_1 and D_2 are nearly conducting at the same time, the voltage difference (V_{O1}-V_{O2}/n) between the two windings is applied across the leakage inductance L_k. Hence, the current commutation time is determined by L_k and (V_{O1}-V_{O2}/n). The current decreasing slope of i_L is (V_{O1}-V_{O2}/n)/(L_k/n^2). The current increasing slope of i_P is (V_{O1}-V_{O2}/n)/(L_k/n^2)-V_{O1}/L_m. This mode ends when the current i_L decreases to zero. Although the voltage difference (V_{O1}-V_{O2}/n) is pretty low when compared to V_{O1}, the current slope is still large because L_k is low. During this mode, the magnetizing inductance L_m charges both of the output capacitors, C_{O1} and C_{O2}. During this mode, the charging currents i_P and i_L are calculated in (6) and (7), respectively.

$$i_L(t) = i_L(t_2) - \frac{V_{o1}-\frac{V_{o2}}{n}}{\frac{L_k}{n^2}} \cdot (t - t_2),\ (t_2 \le t \le t_3) \quad (6)$$

$$i_P(t) = i_P(t_2) + \frac{(\frac{V_{o1}-\frac{V_{o2}}{n}}{L_k/n^2} - \frac{V_{o1}}{L_m})(t-t_2)}{n},\ (t_2 \le t \le t_3) \quad (7)$$

Mode 4 (t_3-t_4): After i_L decreases to zero at t_3, D_1 is turned off naturally. The voltage v_{ds} across the switch S_1 becomes V_{in}-(V_{O1}-V_{O2}/n). The equivalent circuit of this mode is shown in Fig.4(d). Fortunately, because the voltage difference (V_{O1}-V_{O2}/n) is fairly small in steady state operation, the voltage variation across S_1 during this mode is negligible. Since the magnetizing current charges C_{O2}, i_P decreases with a slope of (V_{O2}/(n^2L_m)). This mode ends when the current i_P decreases to zero at t_4. During this mode, the charging current i_P is calculated in (8).

$$i_P(t) = i_P(t_3) - \frac{V_{o2}}{n^2 L_m}(t - t_3), (t_3 \le t \le t_4) \quad (8)$$

Mode 5 (t_4-t_5): At t_4, when i_{Lm} decreases to zero, the inductor L_m begins to resonate with the intrinsic capacitors. The equivalent circuit of this mode is shown in Fig. 4(e). The resonant circuits can be equalized as a simple resonant circuit between the two resonant components L_m and C, where C is equal to (C_S+C_{D1}+n^2C_{D2}). The circuit derivation of this mode is shown in Fig.5. The current i_{Lm} and the voltage v_{ds} can be derived in (9) and (10) according to the equivalent resonant circuit. The leakage inductance L_k is omitted since its value is much less than L_m.

$$i_{Lm}(t) = \frac{-V_{O1}\cdot\sin(\omega_r(t-t_4))}{Z_r} \quad (9)$$

$$v_{ds}(t) = V_{in} - V_{O1} + V_{O1}\cos(\omega_r(t - t_4)) \quad (10)$$

where $\omega_r = 1/\sqrt{L_m \cdot (C_S + C_{D1} + n^2 C_{D2})}$, $Z_r = \sqrt{L_m/(C_S + C_{D1} + n^2 C_{D2})}$.

Due to the resonance between the intrinsic capacitors and the inductance L_m, the voltage v_{ds} drops from V_{in} to 0 (or valley) at t_5. After that, S_1 can be switched on with zero voltage switching (ZVS) or valley switching. From the equivalent resonant circuit, although the output voltage is extended, the ZVS condition is still determined by the first output V_{O1}, which is similar to that of the conventional BCM

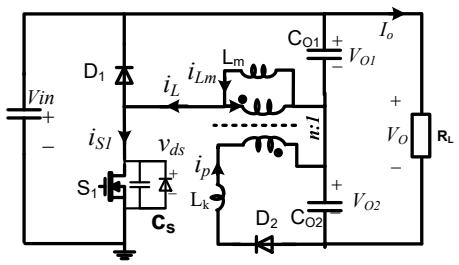


Fig. 2. Equivalent dc-dc converter of the proposed Buck converter.

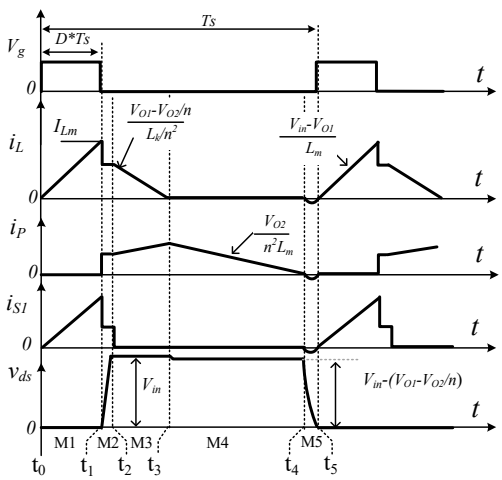


Fig. 3. Key waveforms of the steady state operation in one switching cycle.

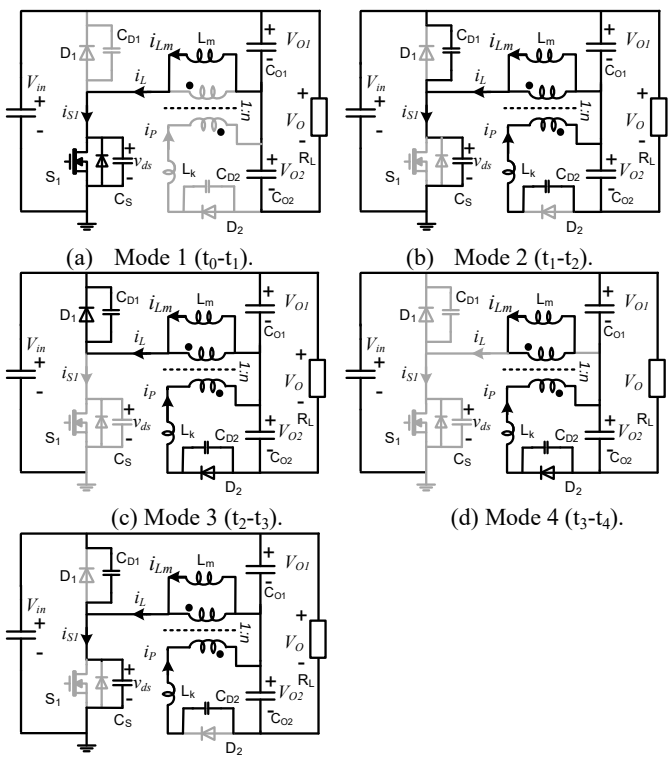


Fig. 4. Equivalent circuits of the operating modes during one switching cycle: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode 5.

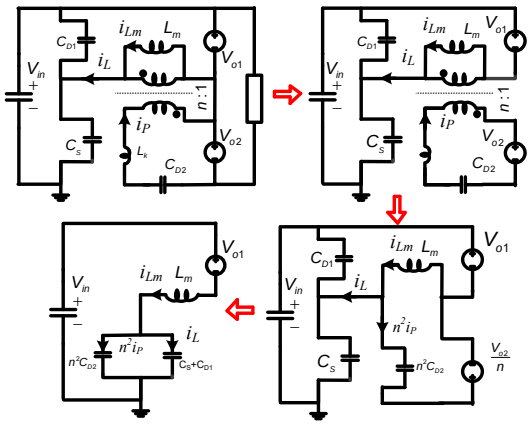


Fig. 5. Equivalent resonant circuit derivation of Mode 5.

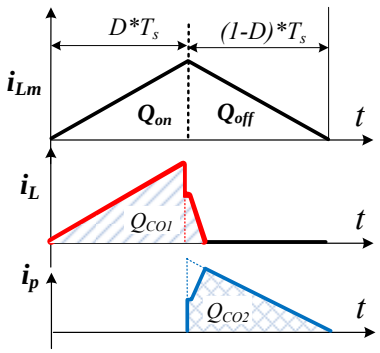


Fig. 6. Simplified current waveforms of i_{Lm}, i_L and i_p.

Buck converter [4].

After t_5, the switching cycle finishes and another cycle begins.

B. The Maximum Output Voltage of the Proposed Buck Converter

Since the capacitors C_{O1} and C_{O2} are in series, the output currents of the two capacitors are the same. In order to keep the steady state operating, the charge into the two output capacitors should be equal during a switching cycle. Fig.6 shows simplified current waveforms of i_{Lm}, i_L and i_p by neglecting the transition modes 2 and 5. From the switching mode analysis under steady state operation, the charge into C_{O2} appears during modes 3 and 4 as Q_{CO2}; and the charge into C_{O1} appears as Q_{CO1}, as shown in Fig.6. The charge provided from the inductor during the conducting mode and off mode of S_1 is divided into two parts, Q_{on} and Q_{off}. The capacitor C_{O2} can be charged by L_m during modes 3 and 4. Meanwhile, for C_{O1}, it can be charged during modes 1 and 3. For this reason, the maximum charge into C_{O2} is Q_{off}/n. In addition, the minimum charge into C_{O1} is Q_{on}. Hence, $Q_{CO1} \geq Q_{on}$ and $Q_{CO2} \leq Q_{off}/n$. Because the charge into the two output capacitors, Q_{CO1} and Q_{CO2}, should be equal during one switching cycle, an inequality (11) can describe the relationship between Q_{on} and Q_{off}.

$$Q_{on} \leq Q_{CO1} = Q_{CO2} \leq Q_{ff}/n \tag{11}$$

In one simplified switching period (neglecting modes 2 and 5), L_m is charged by (V_{in}-V_{O1}) when S_1 is on and it is discharged by V_{O1} (in mode 3) and by (V_{O2}/n) (in mode 4), as shown in Fig. 3. If (V_{O1}-V_{O2}/n) is fairly low, namely $V_{O1} \approx V_{O2}$/n, the voltage across L_m is approximately V_{O2}/n. If (V_{O1}-V_{O2}/n) is high, $(t_3 - t_2)$ is a lot less than $(t_4 - t_3)$ because the duration of mode 3 is inversely proportional to the voltage difference (V_{O1}-V_{O2}/n). Then the voltage across L_m is approximate V_{O2}/n, which is mostly determined by circuit mode 4. In conclusion, during the discharging period, the voltage across L_m is approximately V_{O2}/n. Then the expressions of Q_{on} and Q_{off}/n can be derived as (12) and (13).

$$Q_{off}/n \approx \int_0^{(1-D)*Ts} \frac{V_{O2}}{n^2 L_m} tdt \tag{12}$$

$$Q_{on} = \int_0^{D*Ts} \frac{V_{in}-V_{O1}}{L_m} tdt \tag{13}$$

where *Ts* is the switching period, and *D* is the duty cycle.

Meanwhile, under the steady state operation condition, by the volt-second balance of the inductor, the relationship between the voltages V_{O1} and V_{O2} can be roughly obtained in (14).

$$(V_{in} - V_{O1}) * D \approx \frac{V_{O2}}{n} * (1 - D) \tag{14}$$

In addition, the steady state voltage gain of the converter can be deduced in (15).

$$D = \frac{V_{O2}}{n(V_{in}-V_{O1})+V_{O2}} = \frac{V_O-V_{O1}}{n(V_{in}-V_{O1})+V_O-V_{O1}} \tag{15}$$

By substituting equations (12), (13) and (15) into $Q_{on} \leq \frac{Q_{ff}}{n}$, which is from equation (11), an inequality for the duty cycle can be obtained in (16).

$$(1 + \mathrm{n})D^2 - (2 + \mathrm{n})D + 1 \geq 0 \tag{16}$$

Then from the critical condition of (16), the maximum duty cycle D_{max} can be derived in equation (17).

$$(1 + \mathrm{n})D_{max}^2 - (2 + \mathrm{n})D_{max} + 1 = 0 \tag{17}$$

Therefore, D_{max} can be solved in (18).

$$D_{max} = \frac{(n+2)\pm\sqrt{(n+2)2-4(n+1)}}{2(n+1)} = \frac{n+2\pm n}{2(n+1)} \tag{18}$$

Because one of the solutions (unity gain) must be abandoned, the real solution is:

$$D_{max} = \frac{1}{(n+1)} \tag{19}$$

When the duty cycle of the converter is less than D_{max}, the converter can work in the steady state because the charge balance condition (11) is matched. When the duty cycle is higher than D_{max} in (19), the output regulation capability is lost for the dc-dc converter.

When the maximum duty cycle is determined, the total output voltage V_O can be derived in (20) according to equation (15).

$$\mathrm{V}_O = \mathrm{V}_{O1} + \mathrm{V}_{O2} = (n + 1)V_{O1} - nV_{in} + \frac{n(V_{in}-V_{O1})}{1-D} \tag{20}$$

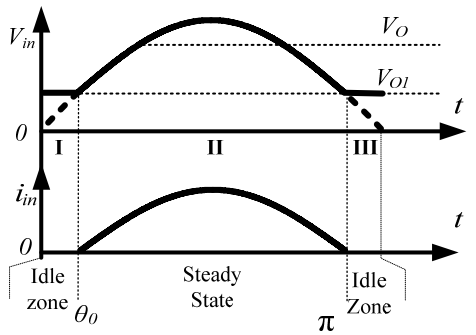


Fig. 7. Interval division in half of a line cycle.

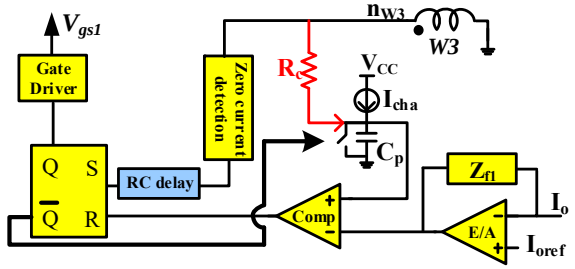


Fig. 8. Simplified VOT control scheme for the proposed ac-dc converter.

Finally, the output voltage limitation V_{O_max} in the steady state condition can be obtained by substituting (19) into (20).

$$V_{O\_max} = (n+1)V_{O1} - nV_{in} + \frac{n(V_{in}-V_{O1})}{1-D_{max}} = V_{in} \quad (21)$$

This limitation shows that the proposed converter is a step-down converter. It should be noted that although the maximum output voltage is derived from a dc-dc conversion, this voltage limitation also exists in ac-dc conversions.

III. Design Considerations of the Improved Buck AC-DC LED Driver

A. Operating Intervals of the AC-DC Converter

After the maximum voltage of the converter is determined, the line cycle operating intervals can be analyzed for the ac-dc converter. Since the maximum dc output voltage should be lower than the input voltage, the maximum V_{O_max} is limited by the peak value of the ac input voltage. At the same time, when the input is higher than V_{O1}, the converter begins working. Therefore, the ac-dc converter can be divided into three intervals during a half line cycle, as shown in Fig.7. Interval I and III are both idle states because the converter does not work when the input V_{in} is lower than V_{O1}. In interval II, the converter is under the steady state of the operating condition. It is obvious that V_{OI} determines the dead time of the input current, which dominates the low order harmonics.

For the ac-dc converter, in order to keep the dc output stable in half of a line cycle, a charge balance between C_{O1} and C_{O2} is required. Before analyzing the charge balance, more assumptions are made. Because the capacity of C_{O1} and C_{O2} is large enough, V_{O1} and V_{O2} are almost constant during half of a line cycle. In order to simplify the expression of the duty cycle, it is assumed that L_m is charged by the voltage (V_{in}-V_{OI}) when S_1 is on, and discharged by the voltage (V_{O2}/n). Then the duty cycle of the converter with boundary conduction mode (BCM) operation in half of a line cycle can be obtained in (22).

$$D(\theta,n) \approx \frac{V_{O2}}{n(\sqrt{2}V_{inrms}\sin(\theta)-V_{O1})+V_{O2}} = \frac{V_O-V_{O1}}{n(\sqrt{2}V_{inrms}\sin(\theta)-V_{O1})+V_O-V_{O1}} \quad (22)$$

where V_{inrms} is the rms value of the input voltage, and θ is the line angle of the input.

In order to further reduce the harmonics, the variable on time (VOT) control [24] is applied in the proposed ac-dc converter. The on-time T_{on} and switching cycle T_S can be derived as well as the derivation in [24], which can be given in (23) and (24).

$$T_{on} = \frac{\frac{\pi P_o L_m}{\eta}/(1-\frac{k\sqrt{2}V_{inrms}}{V_{norm}}(sin\theta - sin\theta_0))}{\int_{\theta_0}^{\pi/2}\frac{\sqrt{2}V_{inrms}\sin\theta\,(\sqrt{2}V_{inrms}\sin\theta - V_{O1})V_{O2}}{(n(\sqrt{2}V_{inrms}sin\theta - V_{O1})+V_{O2})\left(1-\frac{k\sqrt{2}V_{inrms}}{V_{norm}}(sin\theta - sin\theta_0)\right)}d\theta} \quad (23)$$

$$T_s(\theta) = \frac{T_{on}}{D(\theta)} \quad (24)$$

where $\theta_0 = arcsin\left(\frac{V_{O1}}{\sqrt{2}V_{inrms}}\right), k = n_{w3}V_{norm}/(n_{W1}R_cI_{CHA})$ is referred to as the modulation index and V_{norm} is defined as 220V. In addition, n_{W3} is the turns count of the auxiliary winding of the inductor, I_{cha} is a constant current source of the on-time control and the resistance R_c is used for generating a variable on-time.

B. Input Current Analysis for the AC-DC Application

According to the operating principle of the proposed Buck ac-dc converter and the VOT control strategy, the input average current at given input and output voltages is derived in (25).

$$i_{avg}(\theta) = \begin{cases} \frac{(\sqrt{2}V_{inrms}\sin(\theta)-V_{O1})\cdot T_{on}}{2L_m}\frac{T_{on}}{T_s(\theta)} & \theta \in (\theta_0, \pi-\theta_0) \\ 0, \ Otherwise \end{cases} \quad (25)$$

Using a Fourier analysis, the rms value I_N of the N^{th} harmonic of the average input current i_{avg} is obtained as:

$$I_N = \frac{2\sqrt{2}}{\pi}\int_{\theta_0}^{\frac{\pi}{2}}\frac{(\sqrt{2}V_{inrms}\sin(\theta)-V_{O1})\cdot T_{on}}{2L_m}\frac{T_{on}}{T_s(\theta)}\sin(N\theta)d\theta \quad (26)$$

where N =1,2,3…

The normalized harmonics of the input current are defined as:

$$H(N) = \frac{I_N}{I_1} \quad (27)$$

C. Relationship between VO1 and the Turns Ratio n

Since V_{OI} determines both the input current idle zone and

the harmonics, the selection of V_{O1} is very important. However, in the proposed converter V_{O1} is determined by the turns ratio n and the specified output voltage V_O for a detailed ac-dc application. Therefore, the relationship between n and V_{O1} should be investigated.

In order to demonstrate the design procedure of the key parameters for the proposed ac-dc converter, the input of the ac-dc prototype is chosen at 220Vac (+/-20%), that is 176Vac~264Vac. Therefore, the maximum output voltage must be lower than the peak value of the minimum ac input. For a minimum 176Vac input, the maximum dc output is about 250V.

Based on the switching mode analysis, the charge of C_{O2} during half of a line cycle is calculated in (28) by neglecting the charge in mode 2 and mode 5.

$$Q_{CO2} = \int_{\theta_0}^{\pi-\theta_0} \frac{\int_{t_1}^{t_5} i_P(t)\,dt}{T_s(\theta)} d\theta \approx \int_{\theta_0}^{\pi-\theta_0} \frac{\int_{t_2}^{t_4} i_P(t)\,dt}{T_s(\theta)} d\theta \quad (28)$$

In addition, the charge of C_{O1} is calculated in (29).

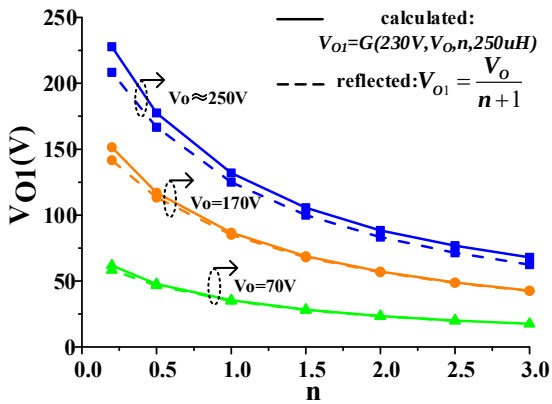
$$Q_{CO1} = \int_{\theta_0}^{\pi-\theta_0} \frac{\int_{t_0}^{t_3} i_L(t)\,dt}{T_s(\theta)} d\theta \approx \int_{\theta_0}^{\pi-\theta_0} \frac{\int_{t_0}^{t_1} i_L(t)\,dt + \int_{t_2}^{t_3} i_L(t)\,dt}{T_s(\theta)} d\theta \quad (29)$$

In order to keep the output voltage stable during half of a line cycle, the charge between C_{O1} and C_{O2} has to be balanced, that is, $Q_{CO1} = Q_{CO2}$. Then the implicit function (30) can be derived by substituting (2), (4), (5), (6), (7) and (8) into (28) and (29). In addition, the explicit expression of V_{O1} can be derived as (31) from (30).

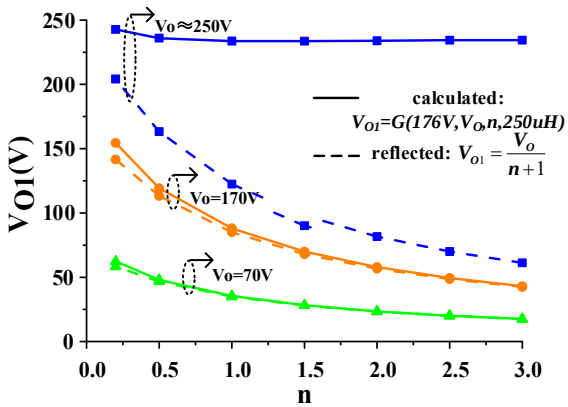
$$F(V_{inrms}, V_O, V_{O1}, n, L_m) = 0 \quad (30)$$

$$V_{O1} = G(V_{inrms}, V_O, n, L_m) \quad (31)$$

Because the implicit function (31) is a transcendental function, the mathematical expression of V_{O1} cannot be derived. However, by using $Q_{CO1} - Q_{CO2} = 0$ and by substituting certain values for the variables V_O, n, L_m and V_{inrms} into (30), V_{O1} can be calculated with a given value for these variables. For example, with V_{inrms}=230V, V_O=214V, L_m=250uH and n=1, V_{O1} can be calculated as 110V. Hence, these detailed results of V_{O1} are depicted by the different points of solid lines at 230Vac in Fig. 9(a) and at 176Vac in Fig. 9(b), where the vertical axis is V_{O1} and the horizontal axis is n. The points of solid lines are calculated with certain V_O, L_m (250uH). The dash lines are the virtual voltage V_O/(n+1) reflected from V_O according to the turns ratio of the windings. These curves show the relationship between V_{O1} and n at different values of V_O. It can be observed that for a given V_O, a larger n results in a lower V_{O1}, which leads to a low THD because of the narrow idle zone of the input current. Furthermore, it can be concluded that V_{O1} is closer to V_O/(n+1) with a lower V_O. Since V_{O1} directly determines the input harmonics, it seems that V_{O1} can be selected according



(a)



(b)

Fig. 9. Relationship between V_{O1} and n with different values of V_O: (a) at a 230 V_{ac} input; (b) at a 176Vac input.

to Fig. 9(a) by the turns ratio n of the coupled inductor at a given V_O. It should be mentioned that when V_O increases, the V_{O1} begins to deviate from V_O/(n+1) because the charge balance condition is changed with an increase of V_O, which is the principle of the derivation of equation (30). Unfortunately, the value of V_{O1} deviates greatly from V_O/(n+1) when the peak of the input voltage is closer to V_O, as shown in Fig. 9(b). Therefore, the design considerations of the proposed ac-dc converter are quite different than those of the VOT Buck [24], Buck and flybuck [22] dc-dc converters. In addition, a modified design procedure for the proposed Buck ac-dc converter is needed.

D. Selection Criteria for Turns Ratio n

Compared to the conventional Buck converter in [24], the output of the proposed ac-dc converter is composed of two stacked dc voltages. For a certain input voltage, V_{O1} can be expressed by certain values of V_O and n in (31). Since V_{O1} directly determines the input harmonics, it can be concluded that V_O and n also determine the input harmonics. With the same high output voltage V_O, the proposed converter can decrease the dead time of the input current by regulating the turns ratio of the inductors, which means a better power

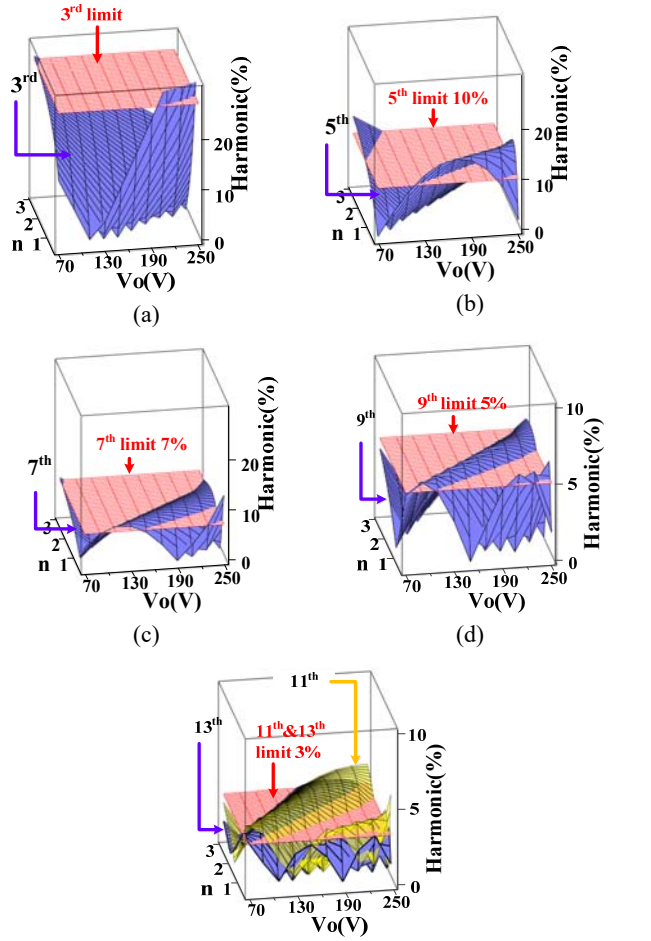


Fig. 10. Harmonics in the function of n and V_O with k=0 at 230Vac and the harmonics limitation (Class C): (a) 3rd; (b) 5th; (c) 7th; (d) 9th; (e) 11th; and 13th.

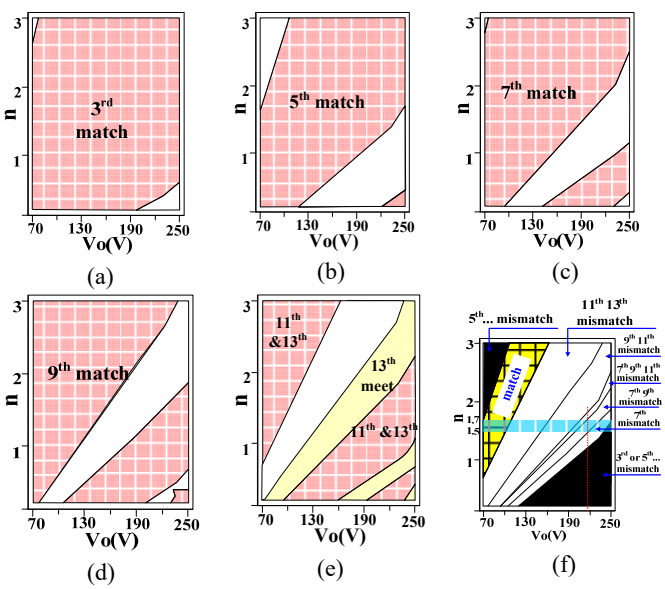


Fig. 11. Match and mismatch region of the harmonics limitation in the function of n and V_O with k=0 at 230Vac: (a) 3rd; (b) 5th; (c) 7th; (d) 9th; (e) 11th and 13th; (f) the 3rd~13th.

quality (THD, PF). Although a higher n results in a lower V_{OI} and a better THD, it may reduce the efficiency because of the small duty cycle of the switch. Therefore, the selection of *n* should pay more attention to the trade-off between the harmonic limitations and high efficiency.

According to the harmonics limitation of the Class C standards (IEC61000-3-2), the harmonics effect of V_O and n is analyzed at 230Vac input. In the formula of the input current harmonics, the difference when compared to the conventional Buck ac-dc converter is that turns ratio n and T_{on} (23) are in the duty cycle (22). In Fig.10, the curve surfaces of the different order harmonic contents of the input current vs. n and V_O with k=0 are plotted according to (27), including 3rd, 5th, 7th, 9th, 11th and 13th. For further analysis, these curve surfaces are projected to the n-V_O plane in Fig.11. Fig. 11(a)-(e) plot the matching regions (shadow areas) for each order harmonic from the 3rd to 13th in the function of n and V_O with k=0 at 230Vac. Fig.11(f) shows the low order harmonics contents (from the 3rd to 13th). In addition, they can match the Class C limitation only in the second region from the left side (yellow region) with k=0. It can be seen that in this narrow region it is difficult to meet the Class C limitation when the output voltage is higher than 150V. However, in many practical high power LED lighting applications, an output voltage higher than 200V is widely used. Fortunately, harmonics higher than the 7th can be depressed by selecting an appropriate modulation index k. Therefore, in order to avoid the 3rd and 5th order contents (dark regions) during a wide output voltage range, the turns ratio n is suggested to be between 1.3 and 1.7 when the output voltage is higher than 200V. In addition, the other high order harmonics can be reduced by k in high output voltage applications.

After the range of the turns ratio n is determined according to the input harmonics, the inductance should be selected according to the detailed output specifications. For a design example, a 150W LED string is chosen as the load and the forward current is 0.7A. In addition, considering the tolerance of the voltage drop of the LED string, the output voltage range is from 107V to 214V. Then, from Fig.11(f), n is chosen as 1.55 in order to have enough of a margin and avoid the peak value of the 7th order harmonics shown in Fig. 10(c) and Fig. 11(c).

E. Selection of the Inductance Lm

The value of the magnetizing inductance L_m significantly affects the switching frequency. The lowest frequency of the VOT Buck converter appears at the peak value of the minimum input due to its BCM operating mode. Because the influence of k is much less than that of the other variables, in

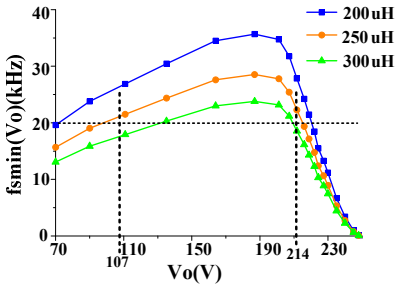


Fig. 12. Minimum switching frequencies in the function of V_O at different inductances.

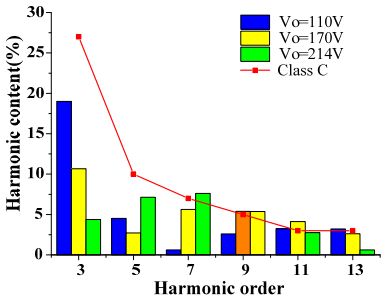


Fig. 13. Calculated harmonics at different output voltages with n=1.55 (k=0).

order to simplify the selection of the inductance, the minimum switching frequency can still be determined according to k=0, which is similar to [23].

When the input voltage is higher than V_{OI}, the expression of the switching frequency is obtained in (32).

$$f_s \approx \frac{\mathrm{D}(\theta)}{T_{on}(\theta)} \tag{32}$$

The minimum switching frequency can still be determined by the following equation (32) at $\theta = \frac{\pi}{2}$ and the minimum input voltage [23].

$$f_{s\_min}\left(V_{inrms\_min}, \frac{\pi}{2}, V_O\right) = D\left(V_{inrms\_min}, \frac{\pi}{2}, V_O\right) \times \frac{\int_{\theta_0}^{\frac{\pi}{2}} \sqrt{2}V_{inrms\_min} sin\theta\left(\sqrt{2}V_{inrms\_min} - V_{O1}\right) D(V_{inrms\_min}, \theta, V_O) d\theta}{\pi V_O I_O L_m / \eta} \tag{33}$$

where $V_{inrms\_min} = 176V, I_o = 0.7A$.

According to (33), the switching frequencies at different output voltages are plotted in Fig.12. Then the value of L_m is obtained as:

$$L_m = D\left(V_{inrms\_min}, \frac{\pi}{2}, V_O\right) \times \frac{\int_{\theta_0}^{\frac{\pi}{2}} \sqrt{2}V_{inrms\_min} sin\theta\left(\sqrt{2}V_{inrms\_min} sin\theta - V_{O1}\right) D(V_{inrms\_min}, \theta, V_O) d\theta}{\pi V_O I_O f_{s\_min} / \eta} \tag{34}$$

If the expected minimum switching frequency f_{s_min} is assumed to be 20 kHz, L_m can be chosen as 250uH for the expected V_O range from Fig. 12.

F. Selection of Modulation Index k

According to the input harmonic analysis mentioned in the above paragraphs, the harmonics when compared to the Class C limitations at different output voltages and selected values of n without an additional modulation control can be plotted in Fig.13. It is clear that the 7th, 9th, 11th and 13th harmonics exceed the limitation at different output voltages. The VOT control strategy [23] can reduce these low order harmonics. After the inductance value L_m and the turns ratio n are both determined, the modulation index k can be selected. Fig. 14 plots the curve surfaces of the harmonic contents of the input current vs. k and V_O with n=1.55. For further analysis, these

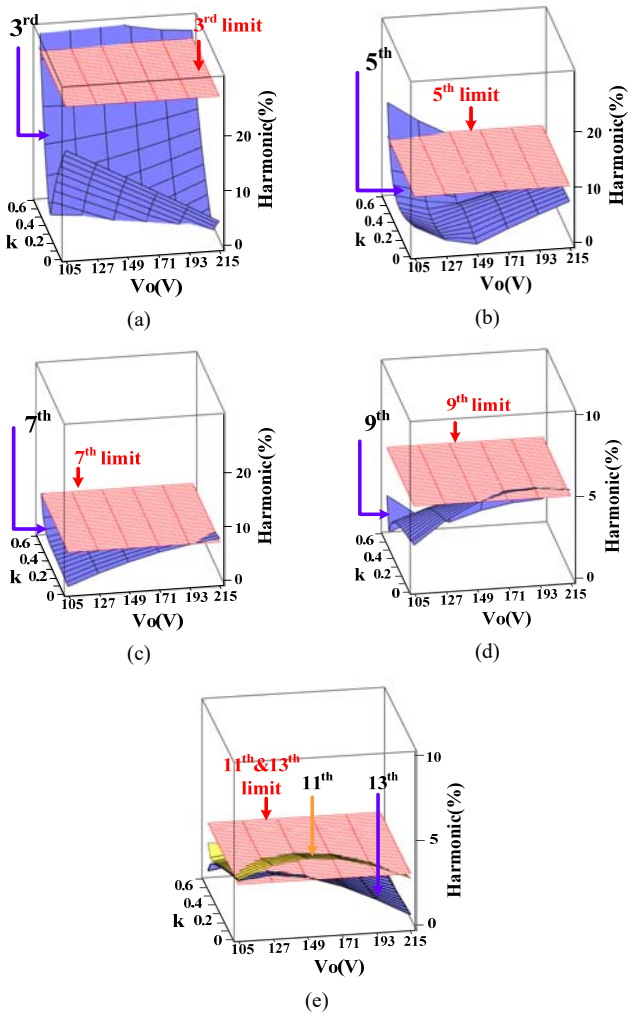


Fig. 14. Harmonics in the function of n and V_O with n=1.55 at 230Vac and harmonics limitations (Class C): (a) 3rd; (b) 5th; (c) 7th; (d) 9th; (e) 11th and 13th.

surfaces are also projected to the k-V_O plane in Fig.15(a)-(e).

The range of the matching region for the output voltage is greatly extended when compared to that in Fig.11, especially for the 7th, 9th, 11th and 13th. In Fig.15(f), it can be concluded that the Class C limitations can be met in the shaded region for all of the harmonics during the whole output voltage range when k is between 0.32 and 0.65.

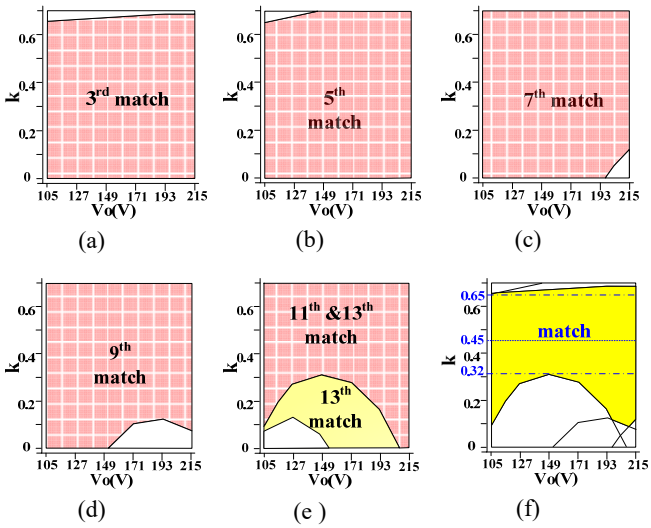


Fig. 15. Match and mismatch regions of the harmonics limitation in the function of n and V_O with k=0 at 230Vac: (a) 3rd; (b) 5th; (c) 7th; (d) 9th; (e) 11th and 13th; (f) the 3rd~13th.

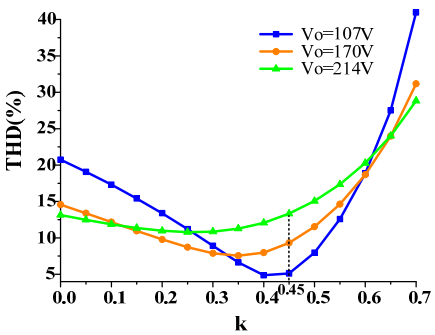


Fig. 16. THD in the function of k at different values of V_O with n=1.55 at 230Vac.

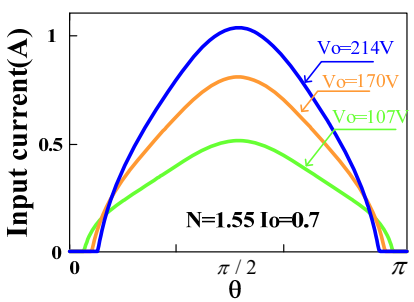


Fig. 17. Calculated input current waveforms of the proposed Buck converter with k=0.45 at different output voltages.

Both the low order harmonics and the THD should be considered in selecting k. Fig.16 shows the calculated THD in the function of k at different values of V_O with n=1.55 at 230Vac. When k=0.45, the THD is less than 15% at different values of V_O. Fig.17 shows the calculated input current waveforms of the proposed Buck converter with k=0.45 at different output voltages. Fig.18 shows the calculated harmonics at different output voltages with k=0.45. All of the harmonics can meet the harmonics requirements (Class C standard) with at least a 23% margin.

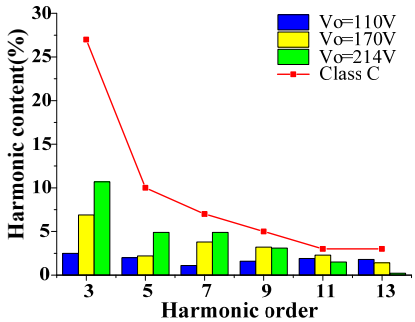


Fig. 18. Calculated harmonics without an input filter (k=0.45) at different output voltages.

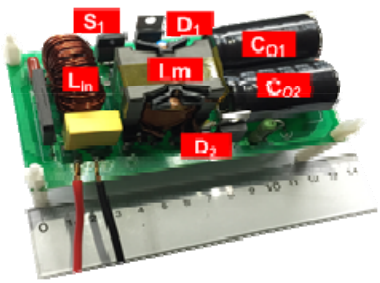


Fig. 19. Photo of the ac-dc LED driver prototype.

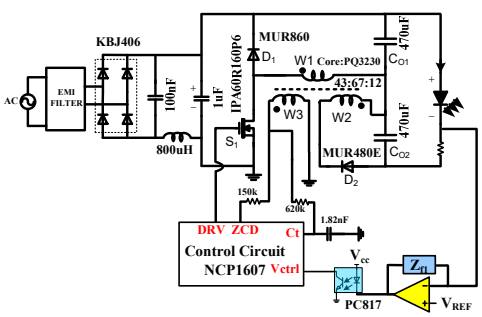


Fig. 20. Schematics and key parameters of the prototype.

IV. Experimental Verifications

In order to verify the theoretical analysis and the performance of the proposed ac-dc Buck converter, a 150W ac-dc LED driver has been built according to the design guidelines in the last section. The input voltage range is 176Vac~264Vac (the rated input voltage is 220Vac). The forward current of the LED module is chosen as 700mA, which is the mainstream specification of LED products. Considering that the forward voltage of a LED module varies at different junction temperatures and different forward currents, the output voltage range is chosen from 107V to 214V with a 50% tolerance (rated output voltage 214V). A photo of the prototype is given in Fig.19. The schematics of the prototype are shown in Fig. 20. All of the key parameters are marked in the schematics. The output current is controlled

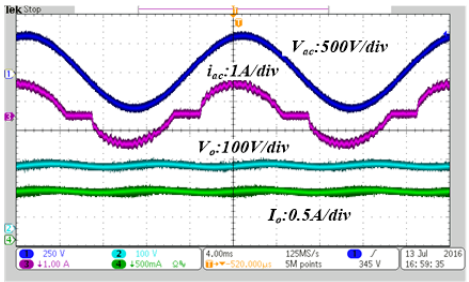
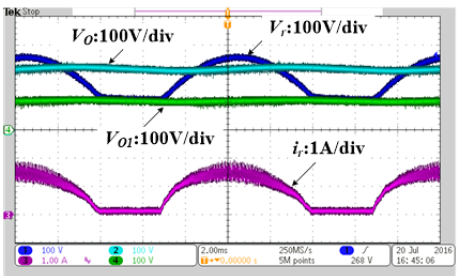
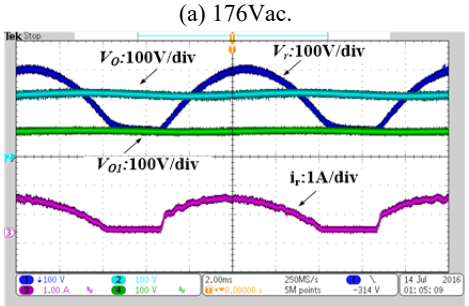


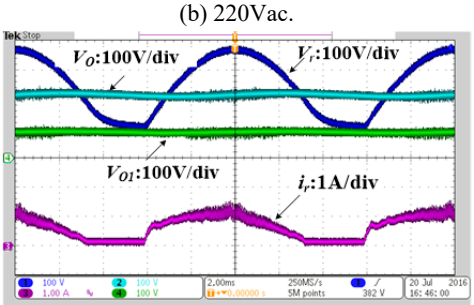
Fig. 21. Measured ac input and dc output waveforms at a 220Vac input and the rated output power.



(a) 176Vac.



(b) 220Vac.



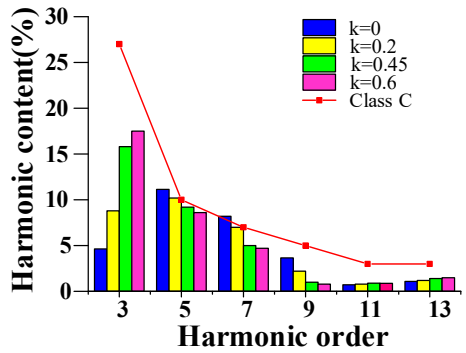
(c) 264Vac.

Fig. 22. Measured rectified input and dc output waveforms at different input voltages and rated output powers.

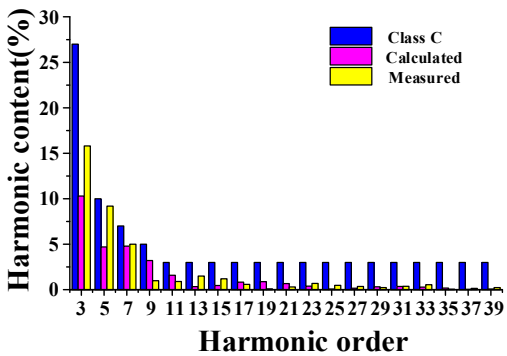
as a current source (700mA in average) to drive the LEDs by a current loop feedback, which is also shown in Fig. 20.

Measured waveforms of the ac input and output voltages along with the currents at a 220Vac input are shown in Fig. 21. With a 214V dc output for a Buck converter, the idle zone of the input current is small.

The measured rectified input voltage V_r and current i_r with V_{OI} and V_O, which are defined in Fig. 1, are provided in Fig. 22. These figures verify that the input idle zone is determined by V_{OI}. When the input voltage increases, the input current's idle zone decreases.

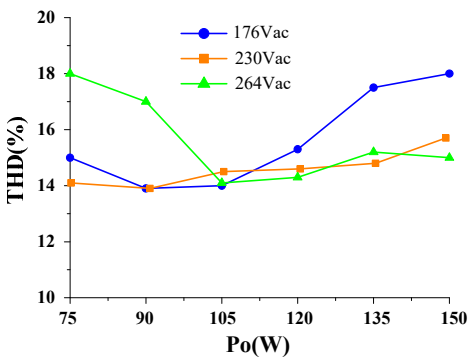


(a)

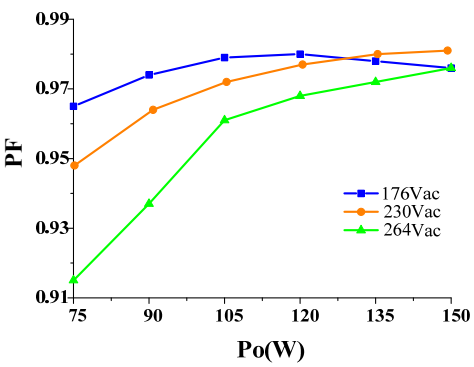


(b)

Fig. 23. (a) Measured harmonic contents of the line current at different values of k with the limits of the Class C standard; (b) measured harmonic contents with the calculated results and the limits of the Class C standard at k=0.45 (V_{in}=230Vac).

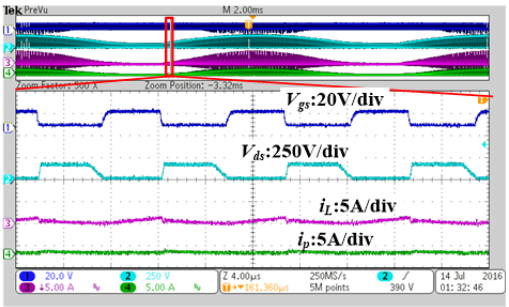


(a) Measured THD at different input voltages.

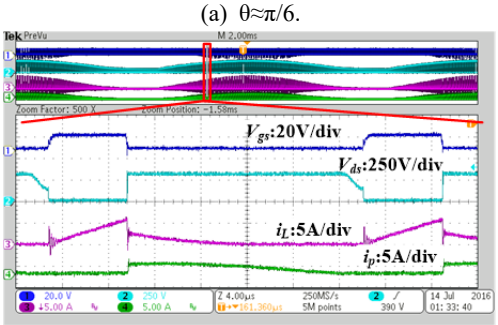


(b) Measured PF at different input voltages.

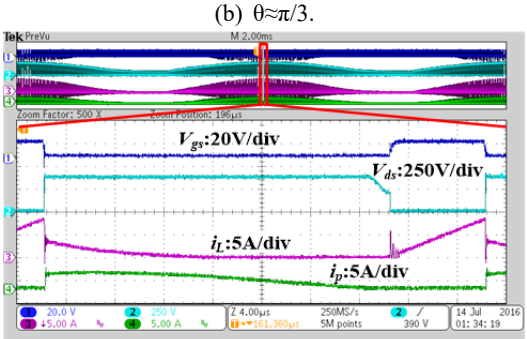
Fig. 24. Measured THD and PF at different operating conditions.



(a) θ≈π/6.



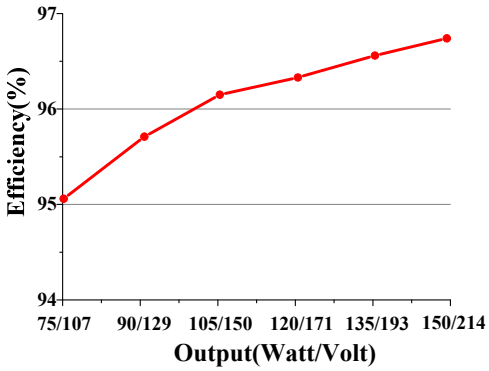
(b) θ≈π/3.



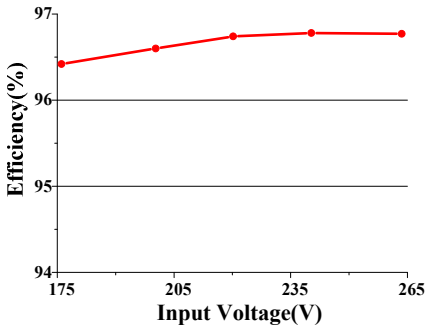
(c) θ≈π/2.

Fig. 25. Measured v_{ds}, V_{gs}, i_L, and i_p waveforms at different line angles in half of a line cycle.

Measured high order harmonics at a 230V_{ac} input with different values of k and measured harmonics with the calculated results at k=0.45 are given in Fig. 23(a) and Fig. 23(b). Because the other high order harmonics can meet the Class C standard very well, Fig. 23(a) only gives the measured odd harmonics from the 3rd to 13th. The harmonic results cannot meet the Class C standard at k=0 or k=0.2 in Fig. 23(a). Although the harmonic results match the Class C standards at k=0.6, the third component of k=0.6 is higher than that of k=0.45, which leads to a higher THD. Therefore, it is reasonable to choose k=0.45. Fig. 23(b) shows that the measured harmonic contents of the line current match the calculating results at k=0.45 and that all of the harmonics are below the limitation of the Class C standard. The measured harmonic contents at k=0.45 verify the theoretical expectations very well except for the third component, whose prediction is much less than the measurement. This is caused by the input differential mode filter capacitor, which causes an additional phase shift and distortion.



(a)



(b)

Fig. 26. Measured efficiencies under a full load as a function of the input voltage and the output power.

Fig. 24 shows the measured THD and power factor (PF) at different input voltages and different output powers. The peak PF is over 0.91 and the THD is less than 20% during the 50%~100% output power range.

Fig. 25 shows the measured primary inductor current i_L and secondary current i_p waveforms at different angles for half of a line cycle at a 264 V_{ac} input. Fig. 25(a) shows that ZVS is achieved when θ is π/6, where the instantaneous input voltage V_{in} is about 140V, which is less than double V_{OI}. Fig. 25(b) and (c) show that the ZVS is lost when the instantaneous input voltage is more than double V_{OI}. Fortunately, the switching on loss is still low in the valley where switching on is achieved. The measured current waveforms in the windings are almost consistent with the analysis in Fig.3, especially at a high input voltage.

The efficiency of the proposed ac-dc LED prototype is measured at different output powers and input voltages. Fig. 26(a) shows the measured efficiency at different output powers, namely at different output voltages because the output current is a constant 0.7A. The efficiency over the load range is above 95%, and the peak efficiency reaches 96.7% at a 220Vac input. Fig. 26(b) shows the measured efficiency under a full load as a function of the input voltage. The peak efficiency almost reaches 96.8%.

V. CONCLUSIONS

This paper proposes an improved BCM Buck ac-dc LED driver with extended output voltage range and low THD. With the coupled winding and stacked output, the output voltage of the proposed Buck converter is decoupled from the power factor and harmonics. Hence, the low THD and extended output voltage are compatible in the proposed ac-dc LED driver. Therefore, the proposed converter has the advantages of the Buck's high efficiency, simple control and low cost, in addition to a flexible output voltage and a low harmonic current. The theoretical analysis and design considerations are verified with a 150W improved BCM Buck ac-dc LED driver prototype.

ACKNOWLEDGMENT

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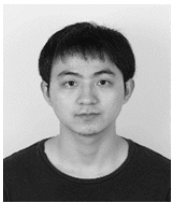

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