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A 4-Channel 6.25-Gb/s/ch VCSEL Driver for HDMI 2.0 Active Optical Cables

Chaerin Hong and Sung Min Park

Abstract—**This paper presents a 4-channel common-cathode VCSEL driver array operating up to 6.25 Gb/s per channel for the applications of HDMI 2.0 active optical cables. The proposed VCSEL driver consists of an input buffer, a modified Cherry-Hooper amplifier as a pre-driver, and a main driver with pre-emphasis to drive a common-cathode VCSEL diode at high-speed full switching operations. Particularly, the input buffer merges a linear equalizer not only to broaden the bandwidth, but to reduce power consumption simultaneously. Measured results of the proposed 4-channel VCSEL driver array implemented in a 0.13-μm CMOS process demonstrate wide and clean eye-diagrams for up to 6.25-Gb/s operation speed with the bias current 2.0 mA and the modulation currents of 3.1 mA_{PP}. Chip core occupies the area of 0.15 x 0.1 μm^2 and dissipate 22.8 mW per channel.**

Index Terms—**AOC, cherry-hooper, CMOS, driver, HDMI, VCSEL**

I. INTRODUCTION

Data transmission rate has been dramatically growing for the past decades. This trend leads to corresponding increase of system bandwidth particularly in the area of high-performance integrated circuits. So far, copper cable- based electric interconnections have been popular as a transmission medium. However, enormous signal attenuation or distortion occurs in the copper cables because of its detrimental skin effect and frequency-dependent dielectric losses. These phenomena become more severe at higher data rate, which vividly limits not only the data rates but also the transmission distance of electrical interconnections. In order to overcome these issues, loss-compensation techniques can be exploited. Yet, it inevitably consumes considerable power and increases chip area [1], thereby mandating its better replacement.

Optical interconnection, on the contrary, enables to provide more attractive, beneficial, and promising solutions for high-speed long-distance transmission over copper-based interconnects. Signal loss is significantly reduced due to the negligibly low-loss and distortion characteristics of optical fibers [2]. Also, it is cost-effective, and is easy to setup and maintain, thereby proliferating a number of applications as shown in Fig. 1.

Many studies have shown that vertical-cavity surface-emitting laser(VCSEL) diodes are suitable for parallel optical interconnects as a transmitting device because directly modulated and emitted lights allow easy fabrication and their low bias and modulation currents can be translated into low power consumption, thereby mitigating thermal issues of dense arrays [3]. Nonetheless, the resulting optical waveforms from VCSELs can be seriously degenerated due to its large parasitic capacitance and inductance in a high-density assembling array [4].

Therefore, we propose a couple of circuit techniques for VCSEL driver arrays to suppress the performance degradation by exploiting equalization and feedforward functions in the circuitry. Especially, a pre-amplifier with Cherry-Hooper configuration is inserted to guarantee

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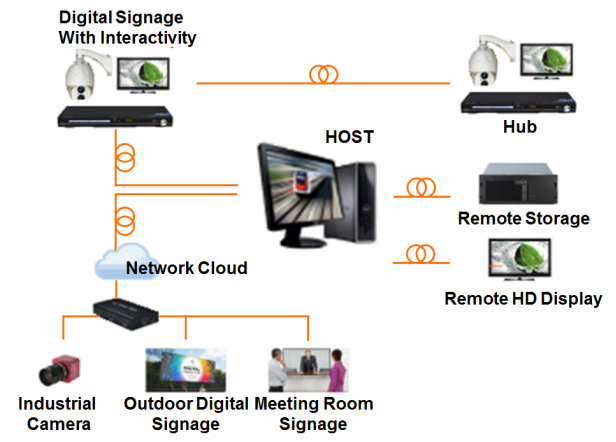

Fig. 1. HDMI applications using active optical cables.

high gain and wide bandwidth characteristics so that the VCSEL driver can operate with full switching for up to 6.25 Gb/s speed.

This paper starts by discussing the requirements of VCSEL drivers in an optical transmitter. Then, circuit techniques for the proposed main driver is described, including feedforward scheme as pre-emphasis, modified Cherry-Hooper amplifier, and input buffer with equalization. Circuit analysis and post-layout simulations are followed. Finally, measured data of the fabricated VCSEL driver chip are discussed to prove the validity of the proposed VCSEL driver.

II. Proposed VCSEL Driver

The advances of multimedia applications such as HDMI active optical cables demand high-speed low-power CMOS VCSEL driver arrays. However, a typical issue arises in a VCSEL driver array, i.e., the output signal path is single-ended for low-cost although each channel has fully differential inputs. Therefore, serious impedance mismatch may occur at the output of VCSEL driver. In order to circumvent this problem, an additional ground-pad should be placed adjacently to provide low-inductance return path for modulation currents, which however leads to large chip area due to its I/O pad configuration of an array.

Fig. 2 shows the block diagram of an optical transmitter which drives a common-cathode VCSEL diode with bias currents and modulation currents. First, low-freqeuncy differential digital signals are multiplexed to high-frequency differential signals by clocking with a

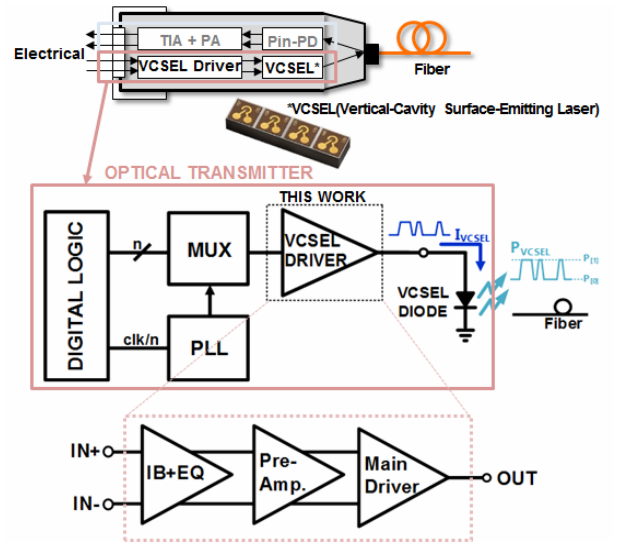

Fig. 2. Block diagram of an optical transmitter with a common-cathode VCSEL diode.

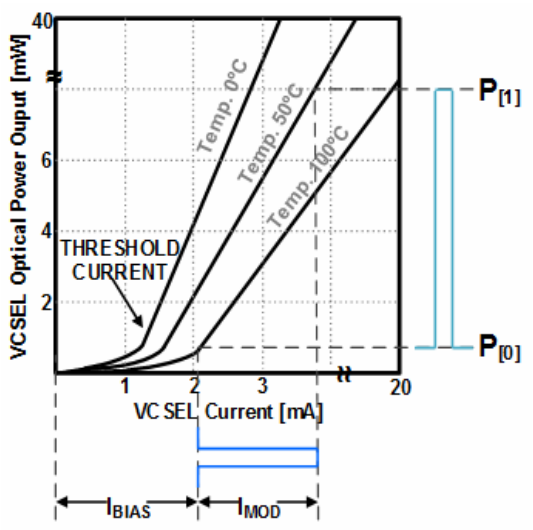

Fig. 3. VCSEL diode characteristics: current vs. optical power.

PLL. Then, VCSEL driver emits modulation currents through a VCSEL diode to transmit optical power over fiber. In this situation, DC bias currents larger than the threshold current of VCSEL diodes must be supplied to the VCSEL diode to avoid relaxation oscillation particularly when transmitting logic '1' signals. Fig. 3 depicts the relationship between the VCSEL optical power and the VCSEL currents, where it is clearly seen that the optical power P[1] is almost linearly emitted with the magnitude of the modulation current(I_{MOD}), and that the bias current(I_{BIAS}) corresponds to transmitting zeros, i.e., P[0].

I_{MOD} is a data-dependent AC current and is added to

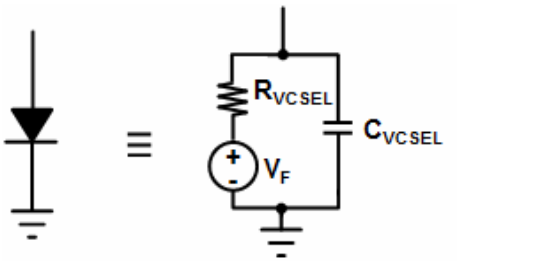

Fig. 4. VCSEL diode equivalent circuit for SPICE modeling.

I_{BIAS} when transmitting P[1] [5]. Namely, the current outputs of the VCSEL driver swing between I_{BIAS} and $I_{BIAS}+I_{MOD}$.

Typically, the modulation current range is large enough to reach the desired optical output power even with a low-efficiency VCSEL diode under high-temperature conditions (corresponding to low slope efficiency). Similarly, the bias current range must be large enough to cover the threshold current under high-temperature conditions (corresponding to high-threshold voltage).

In this work, the bias current of 2.0 mA and the modulation current of 3.1 mA_{PP} are selected.

One of the critical steps to design VCSEL drivers is to model the VCSEL diode as an electrical equivalent circuit so that its transient behavior can be accurately estimated and simulated using SPICE. Fig. 4 shows an example, where the VCSEL diode requires a turn-on forward voltage(V_F), and gives rise to the pad and aperture capacitance(C_{VCSEL}) and the aperture resistance(R_{VCSEL}) [6]. In this work, it is given that V_F = 2.2 V, C_{VCSEL} = 0.85 pF, R_{VCSEL} = 60 Ω .

1. Main Driver with Pre-emphasis

VCSEL diode emits lights perpendicular to the wafer surface, and as described above, the output light power(P_{VCSEL}) grows in an approximately linear fashion with the driving VCSEL modulation currents(I_{MOD}). The quantity(P_{VCSEL}/I_{MOD}) is well known as the slope efficiency which becomes lower at the conditions of higher temperature and longer life. Therefore, the main driver must always provide I_{BIAS} over the threshold current to maintain stable operation of VCSEL diodes. Otherwise, relaxation oscillation may occur when VCSEL diodes are turned on. Also, I_{MOD} should be controlled to provide large extinction ratio (defined by P_1/P_0) even under low-efficiency conditions.

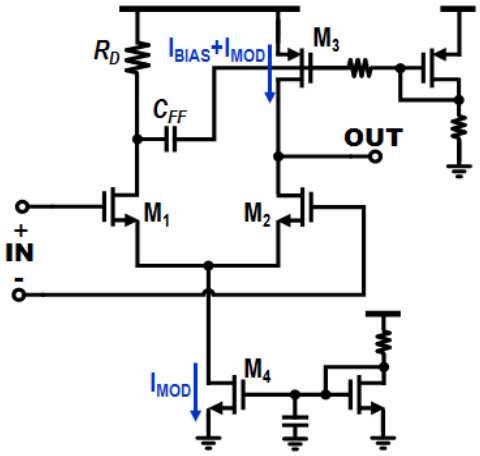

Fig. 5. Schematic diagram of the proposed pre-emphasis main driver.

Fig. 5 depicts the schematic diagram of the proposed main driver which is based on current steering circuit. The sum of the bias and modulation currents, i.e., $I_{BIAS}+I_{MOD}$, is supplied by a PMOS current-source(M_3), whereas I_{MOD} is controlled by the tail-current source(M_4). Therefore, when a logic '1' data is inputted on M_1, a logic '0' at the gate of M_2 turns itself off. Then, the output current of the main driver maintains $I_{BIAS}+I_{MOD}$. When M_1 is off with a '0' input, M_2 is turned on and the output current becomes I_{BIAS} only.

In the design of high-speed VCSEL drivers, the switching speed of the current-steering circuit is significantly important. Hence, the gate-width of driving MOSFETs must be chosen large enough to ensure full switching at the given input voltage swings.

Yet, not too large size should be selected to keep the parasitic capacitances small. As a result, the driving transistors(M_1 and M_2) are designed with the aspect ratio(W/L) of (108 μm / 0.25 μm). Even in this case, switching speed of VCSEL drivers can be limited by the parasitic capacitance and inductance of interconnect components including I/O pads or metal-lines. Therefore, a feedforward technique is further exploited to improve the rising time of the output signals by utilizing a MIM capacitor(C_{FF} = 3 pF). Namely, the drain voltage of M_1 changes when the input rises low to high. Then, C_{FF} passes through the HF components, rendering the gate voltage of M_3 lower accordingly. This will effectively increase the modulation currents, thereby improving the rising time.

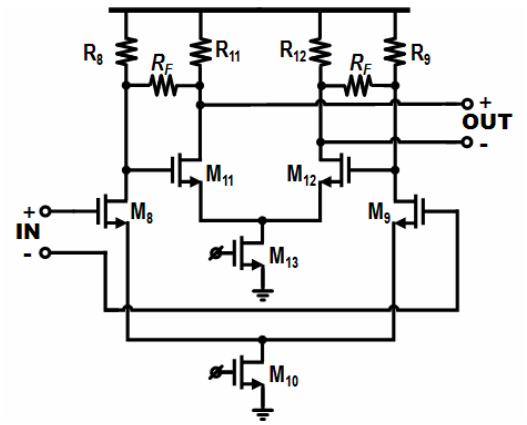

Fig. 6. Schematic diagram of the modified Cherry-Hooper amplifier as a pre-amplifier.

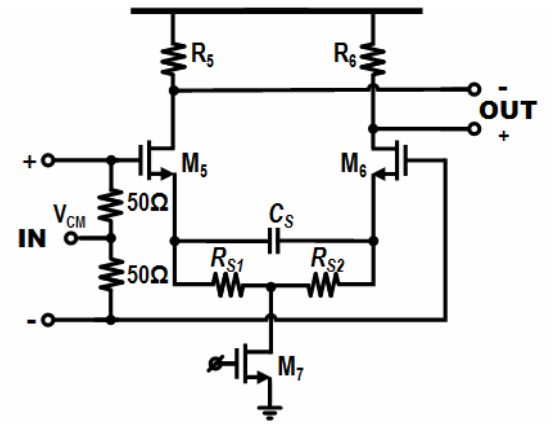

Fig. 7. Schematic diagram of the input buffer merged with a continuous-time linear equalizer.

2. Cherry-Hooper Pre-Amp.

Since the transistors in the main driver must be large to switch large currents, they cannot avoid large input parasitic capacitance. Hence, a critical design tradeoff between switching speed and driving currents occurs because high-speed switching demands small devices. In order to facilitate this issue, a pre-driver is inserted in advance of the main driver as a gain-scaling stage, so that the combination of the pre-driver and the main driver can drive a large capacitive load with high-switching speed and ensure full switching of output voltages by providing sufficient gain. As a pre-driver, we incorporate a modified Cherry-Hooper amplifier (as shown in Fig. 6), which is inserted as an inter-stage between the input buffer and the main driver. It guarantees not only wide bandwidth but also high voltage gain.

The differential pair(M_{11} and M_{12}) with shunt-feedback resistors(R_F) is a transimpedance amplifier which functions as a load for the transconductance stage(M_8 and M_9), hence providing excellent high-frequency performance [7]. The voltage gain of this modified Cherry-Hooper stage is equal to that of a simple common-source amplifier with a load resistance R_F., i.e., $-g_{m8}R_F$. Also, the resistance appeared at the drain nodes of M_8 and M_9 is small, i.e., $R_F/(1+g_{m11}R_{11})$, so that wide bandwidth charactersitics can be achieved. Thereby, the bandwidth is only dependent upon load capacitance, which indicates that higher gain is no longer related to lower bandwidth.

3. Input Equalization Buffer

Although a current-mode logic(CML) is conventionally utilized as an input butter, it consumes large currents. Also, equalization can be exploited in between the amplifier stages to extend bandwidth of the overall system. However, since the cascaded circuits dissipate huge power consumption, we merged the CML input buffer with a continuous-time linear equalizer(CTLE) as depicted in Fig. 7, not only to guarantee 50 Ω input impedance matching, but also to reduce DC power consumption simultaneously. Source degeneration resistors and a capacitor render the gain-boosting by one zero and two poles in the frequency domain, so as to extend the bandwidth [8]. In this work, the values of the degenerated capacitance and resistance are selected to 600 fF and 100 Ω , respectively.

4. Post-layout Simulation Results

Fig. 8 depicts the layout of the proposed 4-channel VCSEL driver array, where the chip core of a single channel occupies the area of 0.027 mm^2. In order to driver the main driver with the designated current levels for the off-chip VCSEL diode, contact areas for interconnects were designed to be wide enough to satisfy the electro-migration rules of the utilized 0.13-μm CMOS technology.

For post-layout simulations, all the feasible parasitic components occurred from bond-wires, ESD protection diode, and I/O pads were considered. As input data, 2^{31}-1 PRBS with an input-common mode level of 0.8 V are

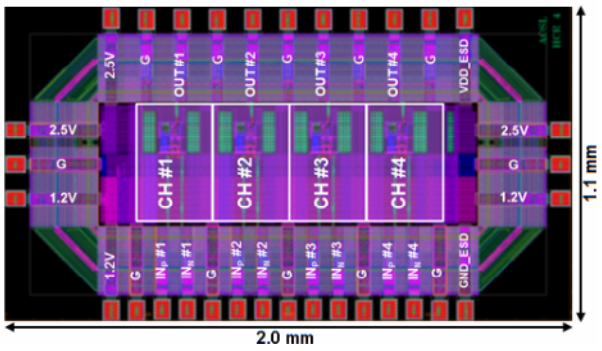

Fig. 8. Layout of the proposed 4-channel VCSEL driver array.

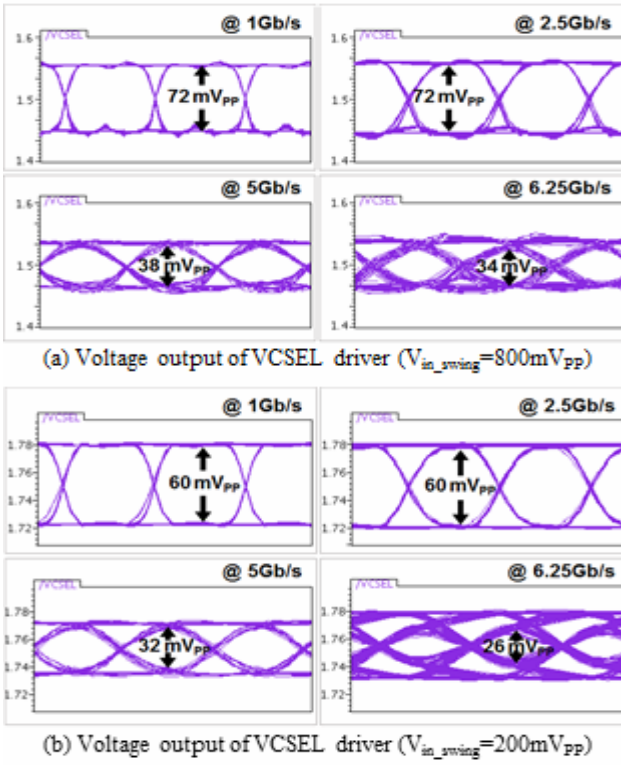

Fig. 9. Simulated voltage eye-diagrams for different input swings of (a) 800 mV_{pp}, (b) 200 mV_{pp} at various data rates of 1 Gb/s, 2.5 Gb/s, 5 Gb/s, and 6.25 Gb/s, respectively.

applied to the proposed VCSEL driver array. Then, the single-ended voltage and current eye-diagrams are obtained at the 2nd channel with 50 Ω impedance termination.

Fig. 9 illustrates the simualted voltage eye-diagrams for two different input voltage swings of 800 mV_{pp} and 200 mV_{pp} at various data rates of 1 Gb/s, 2.5 Gb/s, 5 Gb/s, and 6.25 Gb/s, respectively, where the eye-height of the single-ended output voltages becomes 72 mV_{pp} at lower data rates and decreases at over 5 Gb/s due to the paracitic capacitace. However, the simulated modulation

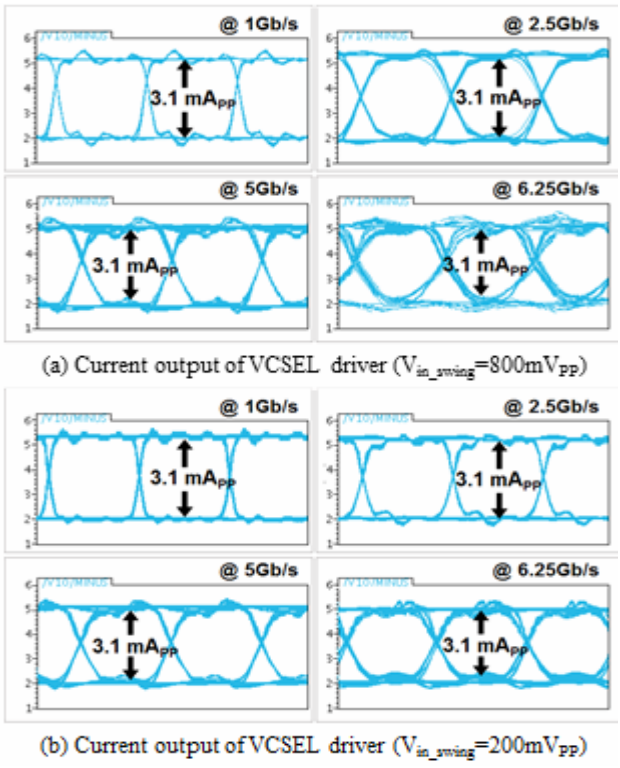

Fig. 10. Simulated current eye-diagrams for different input swings of (a) 800 mV_{pp}, (b) 200 mV_{pp} at various data rates of 1 Gb/s, 2.5 Gb/s, 5 Gb/s, and 6.25 Gb/s, respectively.

currents maintain 3.1 mA_{pp} for the different input voltage swings at various data rates.

III. Chip Fabrication And Measurements

Test chips of the 4-channel VCSEL driver array were realized in a 0.13-μm CMOS technology. Fig. 11 shows the chip microphotograph, where the 4-channel array occupies the area of 2.0 x 1.1 mm^2. Also, Fig. 11 depicts the test setup where a 4-channel common-cathode VCSEL diode array is bond-wired to the driver chip upon a FR-4 PCB. Here, two supplies of 1.2 V and 2.5 V are utilized. DC measurements reveal that the input buffer and the pre-driver dissipate 9.1 mW from 1.2 V, while the main driver consumes 13.7 mW from 2.5 V.

Output voltage eye-diagrams of the proposed 4-channel VCSEL driver array were measured by using Agilent DCA-X 86100D and Anritsu MP1763C pulse-pattern generator. Fig. 12 demonstrates the measured eye-diagrams with a 50 Ω single-ended termination for 2^{31}-1 PRBS differential input swings of (a) 800 mV_{pp} and (b) 200 mV_{pp} at various operation speeds of 1 Gb/s, 2.5

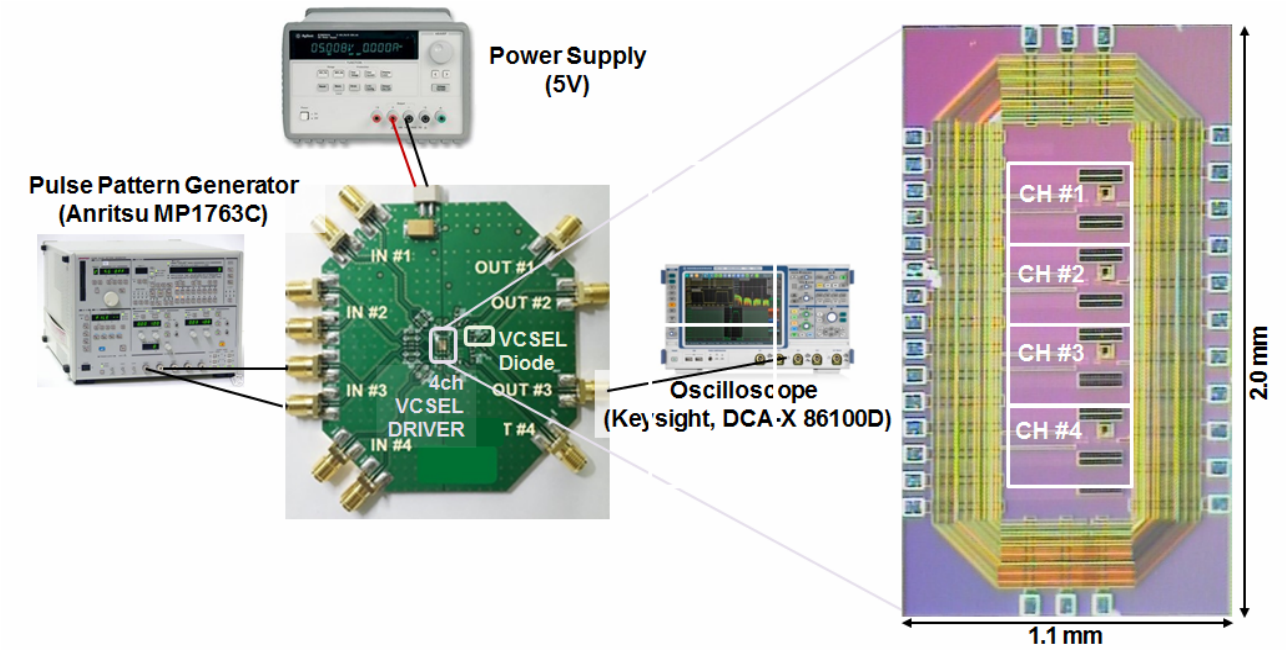

Fig. 11. Chip microphotograph of the proposed 4-channel VCSEL driver array and test setup with PCB module.

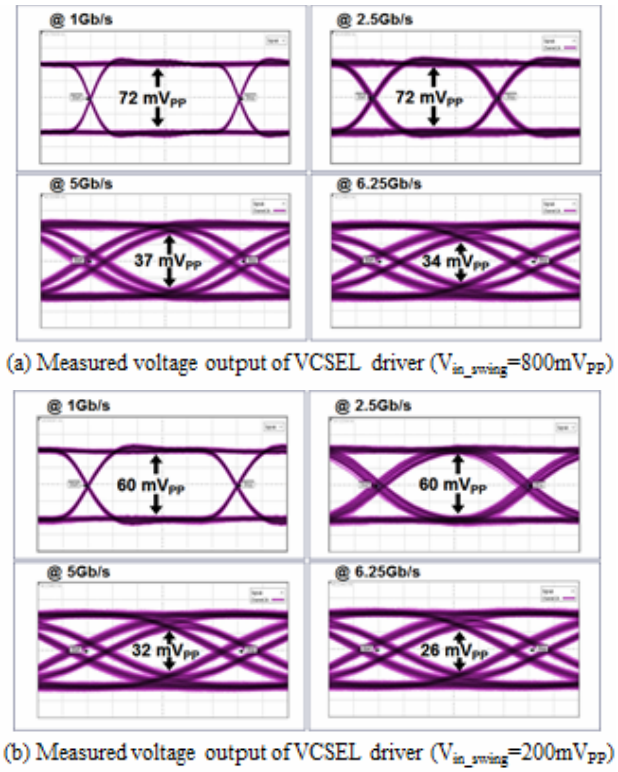

Fig. 12. Measured voltage eye-diagrams for different input swings of (a) 800 mV_{pp}, (b) 200 mV_{pp} at various data rates of 1 Gb/s, 2.5 Gb/s, 5 Gb/s, and 6.25 Gb/s, respectively.

Gb/s, 5 Gb/s, and 6.25 Gb/s, respectively.

The amplitudes of the measured output voltage levels confirm the post-layout simulation results. Table 1 summarizes and compares the performance of the proposed 4-channel VCSEL driver array with recently published prior arts. It is clearly seen that this work consumes smallest power and chip area with lowest jitter characteristics for comparable modulatoin currents and output voltage swings even at higher data rates up to 6. 25 Gb/s per channel.

Table 1. Performance summary and comparison of the proposed 4-channel VCSEL drvier with prior arts

parameters	VCSEL Driver array		
	[9]	[10]	**This work**
Technology	0.13-µm CMOS	0.13-µm CMOS	**0.13-µm CMOS**
Supply	1.5/ 1.2/ 3.0 V	2.5 V	**1.2 V / 2.5V**
Channel no. x Data rate	4 x 5.0 Gb/s	1 x 5.0 Gb/s	**4 x 6.25 Gb/s**
VCSEL Forward Bias	1 ~ 2 V	N/A	**2.2 V**
VCSEL Capacitance	200 fF	N/A	**850 fF**
Modulation Current	13 mA	12 mA	**3.1 mA**
Output signal amplitude	N/A	max. 41 mV_{PP}	**max. 72 mV_{pp} min. 26 mV_{pp}**
Jitter	N/A	< 25 ps,rms	**9 ps,rms**
Power dissipation per channel	26 mW	N/A	**22.8 mW**
Core area per channel	N/A	0.2 mm^2	**0.027 mm^2**

IV. CONCLUSIONS

This paper demonstrates a 4-channel 6.25-Gb/s/ch VCSEL driver array implemented in a 0.13-μm CMOS technology, which employs feedforward techniques for the main driver with a common-cathode VCSEL diode to achieve 6.25 Gb/s operations, merges equalization function into the input buffer to save power consumption, and incorporates Cherry-Hooper amplifier to extend the bandwidth and increase voltage gain for full switching. It can be concluded that the proposed VCSEL driver array provides a low-cost low-power solution for the applications of HDMI 2.0 active optical cables.

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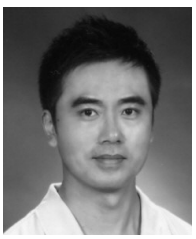

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